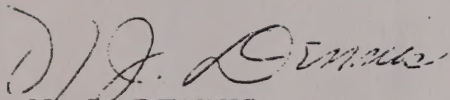


DEPARTMENT OF THE NAVY
Headquarters U.S. Marine Corps
Washington, D. C. 20380

30 September 1968

1. This Manual is effective upon receipt and contains information on the operation and maintenance of the Radio Receiving Set, AN/GRR-17.
2. Notice of discrepancies and suggested changes to this Manual should be forwarded to the Commandant of the Marine Corps (Code CSY).

BY DIRECTION OF THE COMMANDANT OF THE MARINE CORPS

OFFICIAL

N. J. DENNIS
Colonel, U.S. Marine Corps
Director, Technical Division
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[illegible]

SAFETY SUMMARY

LISTED BELOW IS EVERY "WARNING" CONTAINED IN THIS MANUAL AND THE PAGE ON WHICH THE "WARNING" IS LOCATED. ALL PERSONNEL INVOLVED IN THE OPERATION AND MAINTENANCE OF THIS EQUIPMENT MUST FULLY UNDERSTAND THE "WARNING" AND THE PROCEDURE BY WHICH THE HAZARD IS TO BE REDUCED OR ELIMINATED. PERSONNEL SHALL BECOME THOROUGHLY FAMILIAR WITH ALL ASPECTS OF SAFETY OF PERSONNEL AND EQUIPMENT PRIOR TO THE OPERATION AND MAINTENANCE OF THE EQUIPMENT.

1. Potentials as high as 125 volts are present in the power supply circuits. Avoid contact. (Pages 4-15, 4-22, 4-141, and 4-144.)
2. Remove primary power from equipment before attempting module removal, replacement, or any repair technique. (Page 5-22.)
3. Transit Case C43611-G1 is equipped with a pressure relief valve to permit safe transportation by aircraft. Valve MUST be opened (turned fully counter-clockwise) prior to shipment, whether set is packed or unpacked. (Pages 1-5 and 2-11.)

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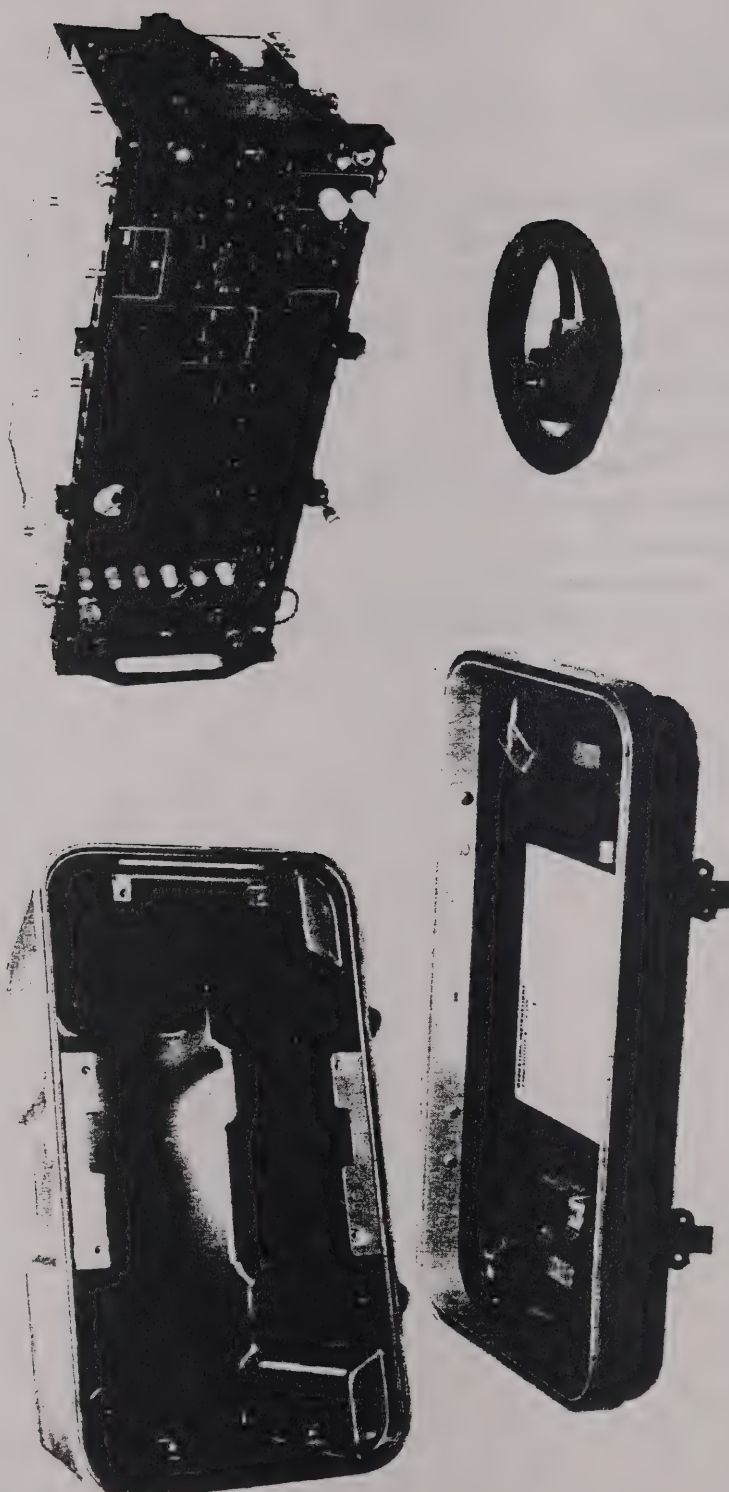


Figure 1-1. Radio Receiving Set AN/GRR-17

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION.

Radio Receiving Set AN/GRR-17 consists of Radio Receiver R-1490/GRR-17 and Transit Case D43611G1. A general view of the set appears in figure 1-1. The set is intended for ground installations and is operationally compatible with Radio Set AN/TRC-75, Radio Receiver-Transmitter RT-671/PRC-47, and Teletype-writer Set AN/TGC-14A(V). The set is operable with the transit case attached following removal of the case cover, or it can be installed in a standard relay rack when the transit case is removed. Radio Receiver R-1490/GRR-17 combines high performance and reliability characteristics with light weight, small size, solid state circuits, and low operating power requirements.

1-2. FUNCTIONAL DESCRIPTION.

Radio Receiver R-1490/GRR-17 is a high dynamic range, dual-conversion superheterodyne receiver for the frequency range from 2.0 to 30.0 mc, employing a digital synthesizer for virtually instantaneous frequency selection. Tuning, in increments of 100 cycles, is performed by setting five tuning dials to the signal frequency in megacycles. Vernier tuning of each 100 cycles step is also provided. The operating modes are for reception of upper or lower single sideband (A3j), amplitude modulated (A3), continuous wave (A1), and frequency shift teletype (F1) broadcasts. A panel mounted speaker permits signal monitoring. Output terminations are provided for the connection of external teletype equipment, and a headset or other terminal equipment. The receiver frequency stability is one part in 10^7 per day allowing extended operating periods without operator attention.

The receiver is of modular construction with hinged front panel, front deck, and rear deck sections for easy access. Circuit modules are of the plug-in type to facilitate field maintenance.

The front panel section contains all the controls, switches, meters, jacks, and terminal connections for the operation and calibration of the receiver in all reception modes. It also contains the frequency standard, bfo, notch filter, vfo, and antenna trimming circuit modules. The panel section is equipped with extension flaps for rack mounting which fold aside when the transit case is attached.

The front deck section contains the main signal path modules consisting of the vhf oscillator, i-f amplifiers, mixers, detectors, and audio amplifier circuits. The rear deck section contains the synthesizer circuit modules supplying all of the tuning injection frequencies required for signal path circuit operation. Power supply circuits are also located on the rear deck.

Receiver operation requires a primary power source of 105 to 125 volts ac, 50 to 400 cycles per second, single phase, or a nominal 24 volt dc power source. Primary power consumption, from the ac source, is a nominal 50 watts, and from a dc source is 24 watts, with the panel lamps "off" and the receiver delivering 15 milliwatts of audio output. (Speaker and noise blanker off.)

1-3. QUICK REFERENCE DATA.

a. GENERAL.

- (1) NOMENCLATURE: Radio Receiving Set AN/GRR-17
- (2) CONTRACT NUMBER: NObsr-95315
- (3) CONTRACTOR: National Radio Company, Inc., Melrose, Massachusetts, 02176, U.S.A.
- (4) DATE OF CONTRACT: 11 May, 1966
- (5) COGNIZANT INSPECTOR: DCASR, Boston, Massachusetts
- (6) NUMBER OF PACKAGES: 1

b. FUNCTIONAL CHARACTERISTICS.

- (1) PRIMARY POWER REQUIREMENTS:
 - (a) Voltage: 115 vac ($\pm 10\%$); frequency: 50 to 400 cps ($\pm 5\%$), 1-phase; or 24 vdc ($\pm 15\%$).
 - (b) Current: Nominal, 0.45 amps ac; 1.0 amps dc.
 - (c) Power: Nominal, 50 watts ac, 24 watts dc (no panel lamp, speaker, noise blanker, or internal TTY supply in use).
- (2) FREQUENCY RANGE: 2.0 to 29.9999 mc.
- (3) TYPE OF FREQUENCY CONTROL:
 - (a) Incremental tuning: Five digital-type selector switches for tuning in 100 cps increments. Controlled by 3 mc crystal oscillator frequency standard.
 - (b) Continuous tuning: Local oscillator tuning of each 100-cps increment by vernier control with ± 150 cps range.
- (4) TYPES OF RECEPTION: Upper or lower sideband ssb, am, cw, mcw, fsk.
- (5) MAXIMUM RECEIVER OUTPUT:
 - (a) Panel speaker: 1 watt (8-ohm load replacing speaker).
 - (b) Phone jack: 15 mw, 600-ohm load.

(6) FREQUENCY STANDARD:

- (a) National Radio Company identification: 42498/42384.
- (b) Frequency: 3 mc.
- (c) Output: 1 mw, 50 ohms (min.).
- (d) Input power: +18 vdc, $\pm 2\%$, no oven.
- (e) Frequency accuracy: 1 part 10^6 for 60 days.
- (f) Drift stability: 1 part 10^7 per day or 5 parts 10^7 for 30 days (ambient temperature constant, $\pm 5^\circ\text{C}$ ($\pm 41^\circ\text{F}$)).

(7) RECEIVER STABILITY AND ACCURACY:

- (a) Incremental tuning: 1 part in 10^7 per day or 5 parts in 10^7 for 30 days.
- (b) Continuous tuning: Adjustment of ± 150 cps at any main tuning increment.

(8) HETERODYNE FREQUENCY RANGE:

- (a) Vhf oscillator: 82 mc to 110 mc.
- (b) Vfo (vernier tuning) oscillator: 3 mc ± 150 cps range.

(9) I-F FREQUENCIES DEVELOPED:

- (a) First conversion: 112 mc.
- (b) Second conversion: 5 mc.

(10) RECEIVER SENSITIVITY. - Listed below are the minimum antenna input signal levels (open circuit voltage from a 50 ohm source) required to produce a receiver output level of 200 milliwatts measured at the speaker terminals, or 15 milliwatts measured at the PHONES terminals, for a signal plus noise-to-noise ratio of 10 db.

<u>Mode</u>	<u>I-F Bandwidth</u>	<u>Input (uv)</u>
A1 (cw)	0.350 kc	1.5
A1 (cw)	1.0 kc	2.5
A3 (am)	8.0 kc	3.0
A3j (ssb)	3.0 kc	1.5 (Usb-lsb)
F1 (fsk)	3.0 kc	3.0

(11) ANTENNA CHARACTERISTICS. - For optimum performance, an antenna having a 50 ohm, unbalanced termination is required. For antennas other than 50 ohms, an antenna trimming circuit is provided.

1-4. EQUIPMENT LISTS.

a. EQUIPMENT SUPPLIED. - Table 1-1 lists the names, quantities, dimensions, and weights of all equipment supplied with the receiver.

b. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Table 1-2 lists the equipment required for operation of the receiver but not supplied.

c. SHIPPING DATA. - Table 1-3 lists the contents, dimensions, volume, and weight of the receiver complement prepared for shipment. The complete equipment is packed for shipment in one box.

TABLE 1-1. EQUIPMENT SUPPLIED

QTY PER EQUIP.	NOMENCLATURE		DIMENSIONS (IN.)			VOL (CU FT)	WT (LB)
	NAME	DESIG	H	W	D		
1	Radio Receiving Set	AN/GRR-17	11-3/32	19-3/32	13-7/16	1.628	53.600
	Radio Receiver	R-1490/GRR-17	7-15/16	16-15/16	12-1/8	0.938	43.600
	Transit Case	D43611-G1	11-3/32	19-3/32	12-7/16	1.628	10.000
1	Antenna Adapter	A43787-1					
1	Power Cable (AC)	C44486-G1					
1	Power Cable (DC)	C44487-G1					
1	Connector, Coaxial, RF	UG-21H/U					

TABLE 1-2. EQUIPMENT REQUIRED BUT NOT SUPPLIED

QTY PER EQUIP.	NOMENCLATURE		USE	REQUIRED CHARACTER- ISTICS
	NAME	DESIG		
2	Technical Manual	TM-05866A-15		
1	Headset	NT-49985-A	Monitor output	600 ohms
1	Antenna	None	Supply rf signals	50 ohms
1	Cable, Coaxial	RG8A/U	Antenna cable	50 ohms
1	Card Puller	C44941G1	Remove p/c cards	
2	Card Extender	D43031G1, 2	Extend p/c cards	

TABLE 1-2. EQUIPMENT REQUIRED BUT NOT SUPPLIED (Cont)

QTY PER EQUIP.	NOMENCLATURE		USE	REQUIRED CHARACTER- ISTICS
	NAME	DESIG		
1	Cable, Module Extender	C44944G1	Extend modules	
1	Cable, Power Supply Extender	C44943G1	Extend power supply	
1	Cable, Intelli- gence Filter Extender	C44942G1	Extend intelli- gence filter	

TABLE 1-3. SHIPPING DATA

BOX NO.	CONTENTS	DIMENSIONS (IN.)			VOL (CU FT)	WT (LB)
		H	W	D		
1	RADIO RECEIVING SET AN/GRR-17 with cables and antenna adapter	16-7/8	24	17-7/8	4.2	64

WARNING

Transit Case C43611-G1 is equipped with a pressure relief valve to permit safe transportation by aircraft. Valve MUST be opened (turned fully counterclockwise) prior to shipment, whether set is packed or unpacked.

SECTION 2

INSTALLATION

2-1. UNPACKING AND HANDLING.

a. DESCRIPTION OF PACKAGING AND PACKING METHODS. - Radio Receiver R-1490/GRR-17 and accessories are packed for shipment in a cardboard box packaged as follows:

(1) The receiver and power cables assembled in the transit case are contained in a carton. End spacers in the carton contain bags of dessicant dehumidifier. A waterproof vaporproof barrier surrounds the receiver carton. This package is surrounded by an outer carton.

b. UNPACKING INSTRUCTIONS.

(1) Observe the markings on the cardboard box and place it on a flat surface with the top up.

(2) Open the outer carton.

(3) Cut open the waterproof liner.

(4) Open the inner carton and remove contents.

(5) Check the contents against the list in table 1-1.

c. HANDLING. - Normal precautions for lifting and transporting electronic equipment should be observed when handling the receiver. It may be lifted by the transit case carrying handles or the panel handles.

d. TRANSIT CASE VALVE. - The transit case is equipped with a pressure relief valve, located near the right-hand handle, to permit safe transportation by aircraft. After unpacking, for field service with case installed, close valve by turning fully clockwise to retain waterproof feature of the case.

e. MECHANICAL INSPECTION. - Directly following unpacking and before installation, inspect the receiver to detect any damage or disarrangement which may have occurred during shipment. A check of the following items may avoid much inconvenience during installation and initial equipment operation.

(1) Check for nuts, washers, or other foreign particles which may be lodged where they could cause a short circuit.

(2) Tighten any screws or nuts on mechanical assemblies which may have worked loose.

(3) Look for broken wires or loose cable connections.

(4) Operate all mechanical controls through their full range of travel to detect jammed controls, bent control shafts, or other evidence of mechanical damage.

(5) See that all plug-in modules and cable connectors are well seated in their sockets. Check that fuses AlAlF1 through AlAlF5 are in place in the fuse holders on the panel.

2-2. POWER REQUIREMENTS AND DISTRIBUTION. (See figure 2-1.)

a. REQUIREMENTS. - The receiver will operate normally from either an ac or a dc primary power source. Ac power requirements are 115 volts ac ($\pm 10\%$), 50 to 400 cps ($\pm 5\%$), single phase. Dc power requirements are 24 volts dc ($\pm 15\%$). Voltage and frequencies should not exceed the tolerances established.

b. PRIMARY POWER CONNECTIONS. - Primary power connection to the receiver requires the attachment of a 6-foot cable which is supplied with the receiver. Table 2-1 lists the cables and connectors required for all external cables not supplied with the receiver.

c. DISTRIBUTION. - The primary power distribution diagram (see figure 5-52) illustrates the distribution of the ac or dc primary power within the receiver. AC primary power from the 115 V AC connector AlAlJ3 on the receiver panel passes through fuses AlAlF1 and AlAlF2, one section of POWER switch AlAlS1, and is applied to the power transformer in the power supply module AlA3PS1. DC primary power from the 24 V AC connector AlAlJ4 on the panel passes through fuses AlAlF4 and AlAlF5, through a diode polarity gate AlAlCR2 and one section

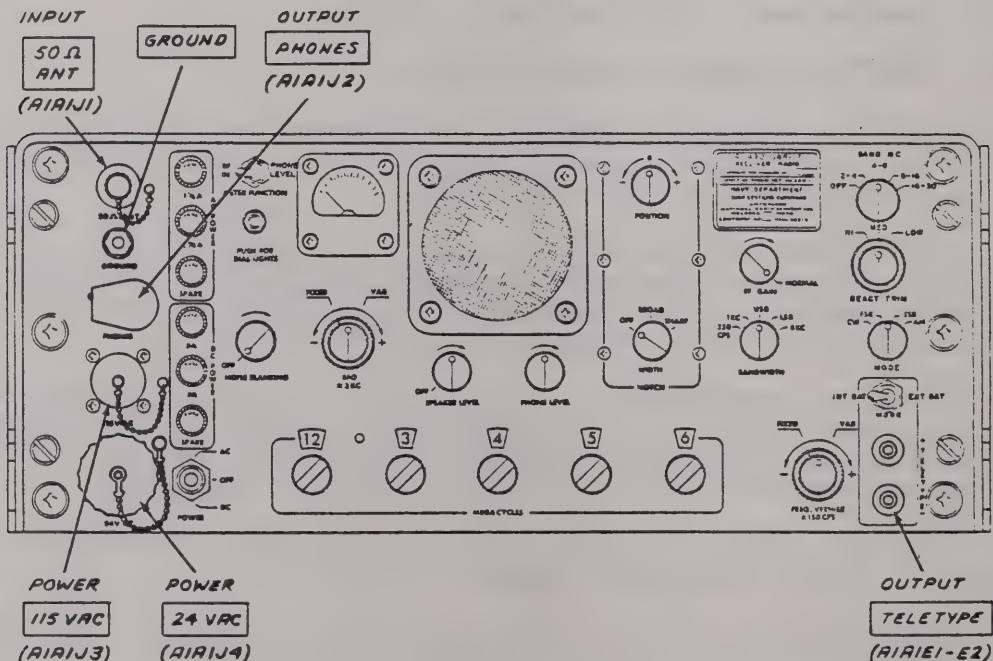


Figure 2-1. External Cable Connections

of POWER switch A1A1S1, and is applied to the output of the ac power supply circuit. The ac and dc power fuses as well as spare fuses are located on the receiver front panel.

2-3. INSTALLATION LAYOUT. (See figure 2-2.)

Radio Receiver R-1490/GRR-17 is designed for general field operation with the transit case cover only removed, or installation in a standard relay rack following removal of the entire transit case. When not installed in a relay rack, it is suggested that the transit case itself be left in place to provide maximum protection for the receiver assembly from physical damage. In selecting a suitable location for the receiver, the following factors should be considered:

a. POWER SOURCE. - The power source described in paragraph 2-2a must be available at the location.

b. CABLE LENGTHS. - Most external cable lengths to and from the receiver are not critical but the transmission line from the antenna should be as short as possible.

CAUTION

When operating from a 24 volt dc power source, note that the load current value is from 1 to 1.45 amperes. If a long power cable is required, make sure the voltage at the receiver terminals is not less than 20.4 volts dc; otherwise, receiver operation will be impaired.

c. SERVICE ACCESS. - The transit case and dust cover must be removed prior to servicing the receiver to expose the plug-in modules. Because all external cables terminate at the front panel, no special considerations are required when mounting the receiver to assure clearance for cable removal or replacement.

d. TEMPERATURE AND VENTILATION. - The receiver dissipates heat at a low rate of approximately 2.85 BTU per minute. The use of solid state circuit modules, combined with the heat conduction and dissipation ability of the chassis and panel structures, limit the receiver temperature rise to 15°C (59°F) above the ambient temperature at the receiver location. The receiver will operate normally at ambient temperatures ranging from -40°C (-40°F) to +65°C (+149°F).

e. INTERACTION WITH OTHER EQUIPMENT. - A principal feature of the receiver is its ability to operate in an environment close to transmitting facilities. Internal shielding and effective filtering reduce the possibility of interaction with other communication equipment.

f. OPERATION WITH AUXILIARY EQUIPMENT. - Installation planning should consider the relative locations of auxiliary equipment, such as teletype printers, with which the receiver will be used.

2-4. INSTALLATION REQUIREMENTS.

Field installation of Radio Receiver R-1490/GRR-17 consists of removing the transit case cover, attaching it to the rear of the transit case for storage, and making the necessary external cable connections at the front panel. Relay rack installation requires removal of the transit case, mounting the receiver in the rack,

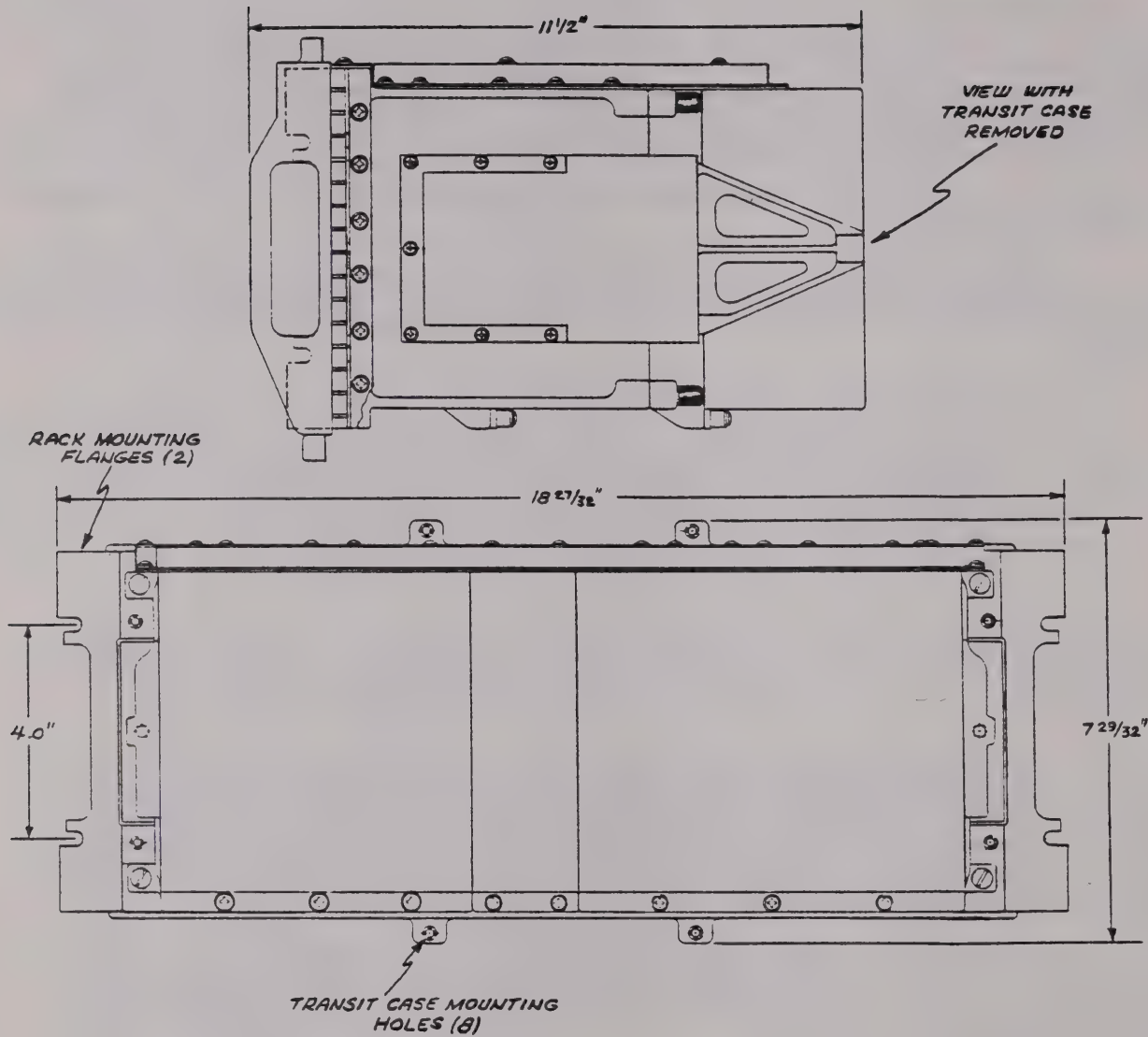


Figure 2-2. Radio Receiver R-1490/GRR-17, Outline Drawing

and the completion of all external cable connections. Initial operating tests (see paragraph 2-5) are performed immediately following an installation to establish normal receiver operation and assure optimum performance, prior to releasing the receiver to operating personnel. Power cables are stored in the transit case cover.

a. REMOVING AND REPLACING THE TRANSIT CASE. - The following procedure is used to remove the transit case, preparatory to relay rack installation, and to replace the transit case when the receiver is removed from the rack.

(1) REMOVING THE CASE. (See figure 2-2.)

(a) Release the cover fasteners and remove the cover. Store the cover at the case rear using the elastic cords provided on the cover.

(b) Release the two captive securing screws at the case rear and loosen the eight captive finger-type screws at the receiver panel.

(c) Withdraw the receiver from the transit case.

(2) REPLACING THE CASE.

(a) Insert the receiver into the case along the shelf.

(b) Tighten the panel and case retaining screws.

b. RELAY RACK INSTALLATION. - The receiver front-panel section is equipped with two hinged flanges, one at each side of the panel which when folded outward support the receiver in a standard relay rack. Preliminary to a relay rack installation, remove the transit case and its cover following the procedure described in paragraph 2-4a.

(1) Swing out the hinged flanges parallel with the receiver panel. A detent mechanism will engage when the flanges are in line with the panel.

(2) Position the receiver at the relay rack and secure the two flanges using four 1/2 inch, 10-32, fillister-head machine screws. Place a washer beneath the head of each screw.

(3) Attach an earth ground connection to the binding post directly below the 50Ω ANT connector on the front panel.

c. EXTERNAL CABLES. - External primary power cables six feet long are supplied with the receiver. Because of variations in installation requirements, the cable for the antenna connection is not supplied. However, a mating connector is supplied for this connection. Table 2-1 contains a summary of the cable types required and identifies each connector and its mating receptacle. Figure 2-3 shows the method of assembling a connector to form an external cable for the 50Ω ANT panel receptacle. Detailed instructions for the assembly of electrical connectors are contained in NAVSHIPS 900,171, Chapters 5 and 6.

d. MAKING EXTERNAL CONNECTIONS. - Figure 2-1 shows the location of all external connections at the receiver front panel. To complete the external connections, proceed as follows:

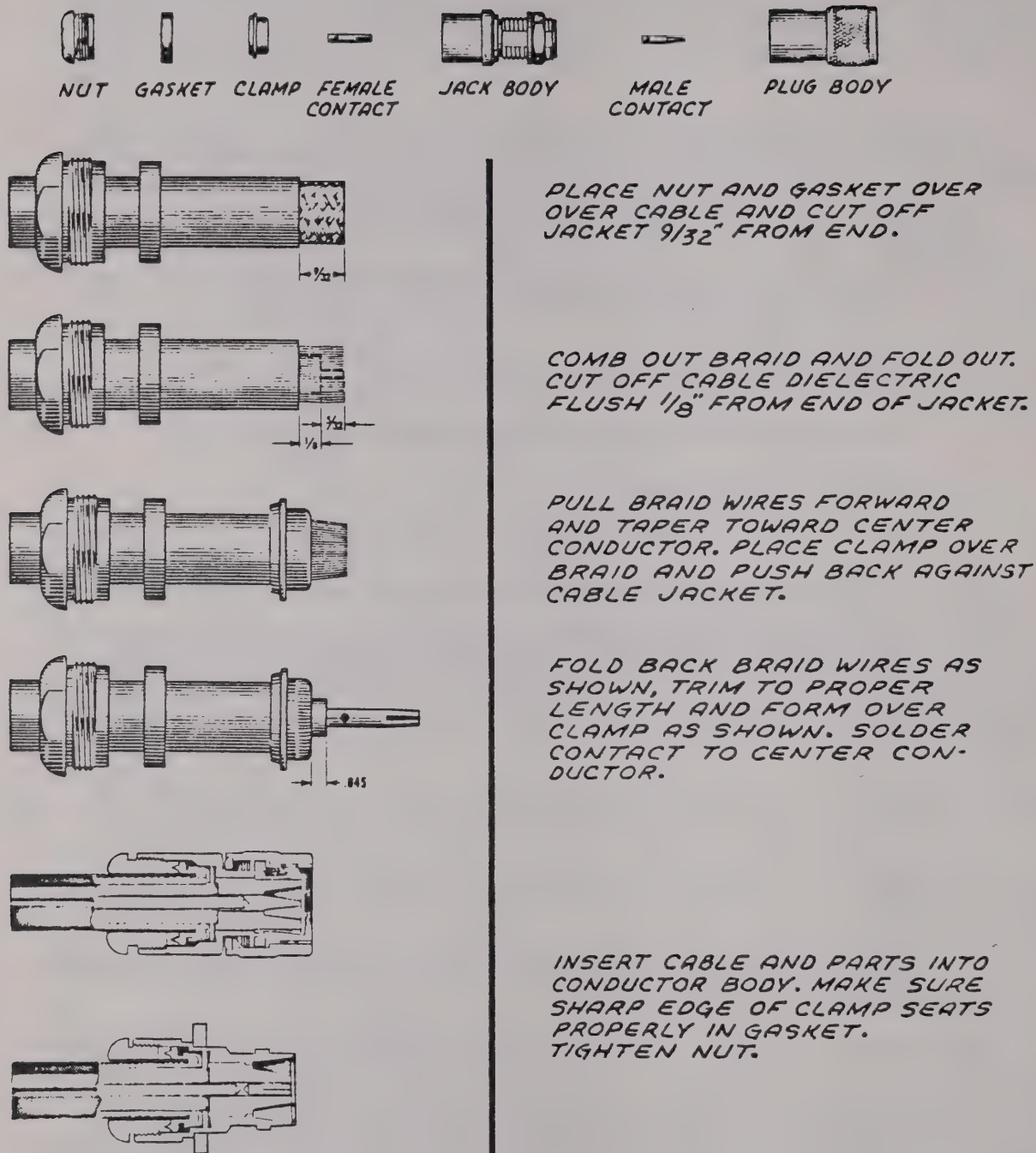


Figure 2-3. Antenna Cable, Connector Assembly

(1) For ac operation, connect one end of the ac power cable (supplied) to receptacle A1A1J3, labelled 115 V AC. Connect the other cable end to the local primary power source. (See paragraph 2-2a for the power requirements.)

TABLE 2-1. CONNECTORS SUPPLIED AND EXTERNAL
CABLE REQUIREMENTS

CIRCUIT WHERE USED	TYPE CABLE	EQUIPMENT RECEPTACLE	CABLE CONNECTOR
Antenna transmission line, 50 ohm termination.	RG-8/U	UG-556B/U	UG-21H/U
Teletype output signal line.	Not specified	FSN-5940- 351-6993	None

(2) For dc operation, connect one end of the dc power cable (supplied) to receptacle A1A1J4, labelled 24 V DC. Connect other cable end to the local dc primary power source. Observe polarity. (See paragraph 2-2a for power required.)

CAUTION

Inadvertent connection of the ac power cable to a dc primary power source, and vice versa, will cause the panel fuse to blow and may damage the equipment.

(3) Connect the antenna transmission line at receptacle A1A1J1, 50Ω ANT. (An antenna post adapter is provided for long-wire antennas.)

(4) Connect teletype equipment to the two terminals labelled TELETYPE. Observe terminal polarity. The positive lead must be attached to the upper terminal marked (+). Connect (-) lead to teletype equipment ground. If the teletype unit which is used supplies its own loop potential, place the MODE, INT BAT/EXT BAT switch at EXT BAT. In this position, the receiver teletype output provides contact closure for external loop potentials up to 120 volts, 60 ma. If the teletype unit used does not supply its own loop potential, place the MODE, INT BAT/EXT BAT switch at INT BAT. In this position, the receiver TTY power supply delivers 120 volts at 60 ma in series with the TELETYPE terminals. Refer to the applicable technical manual for the teletypewriter equipment used.

2-5. INITIAL OPERATING TESTS.

a. GENERAL. - After the receiver is installed and before turning it over to operating personnel, observe the receiver performance in detail and make any necessary circuit adjustments. All operating aspects and features of the receiver should be checked during the initial operating checks with particular attention paid to any condition noted which could lead to abnormal performance.

b. INITIALLY ENERGIZING RECEIVER. - The location of each panel control is shown in figure 3-1, and table 3-2 gives a brief description of the control

functions and indicates their preset positions. To initially energize the receiver, perform the following steps in the order presented.

- (1) Make sure that all cable connections at the panel are secure.
- (2) Verify that the receiver is connected to the correct primary power source described in paragraph 2-2a.
- (3) Preset all panel controls according to table 3-2.
- (4) Place external primary switches on at the installation site.
- (5) Set the POWER switch to AC (for an ac power source) or to DC (for a dc power source).
- (6) Press the PUSH FOR DIAL LIGHTS panel switch and observe that the MEGACYCLES dial windows are illuminated. Release the switch.
- (7) During tests, use the SPEAKER LEVEL or the PHONE LEVEL controls to adjust the speaker or headset volume levels, respectively.

c. TUNING PERFORMANCE. - To test receiver performance, use a signal generator (Signal Generator AN/URM-25 or equivalent) or actual transmitted signals. Because the tuning accuracy of the receiver exceeds that of most signal generators, use the receiver or a primary frequency standard to calibrate the generator. The receiver tuning performance is evaluated by setting the generator frequency and the MEGACYCLES tuning dials for reception of six test frequencies, selected to verify operation of the six antenna input filters (A1A2A1) as well as the operating ranges of the synthesizer circuits. It is unnecessary to test the continuous tuning (frequency vernier) circuit at more than one frequency.

(1) INCREMENTAL TUNING. - A complete tuning procedure for the receiver is described in Section 3, Operation. Main points from this procedure have been selected for the following tuning performance tests, using the SSB reception mode.

(a) Connect the signal generator to the 50 Ω ANT connector (A1A1J1). Adjust generator for a 2.5000 mc, 10 microvolt, unmodulated test signal.

(b) Set the MODE switch at SSB, and the BANDWIDTH switch at LSB.

(c) Tune the receiver to 2.5010 mc by setting the MEGACYCLES tuning dials to read 02.5010.

(d) The signal level meter on the panel should indicate and a 1000 cycle tone should be heard in the speaker.

(e) Repeat steps (b) and (c) with signal generator test frequencies 4.0000, 6.5000, 10.0000, 15.5000, and 24.5000 mc. Tune the receiver 1 kc above the generator frequency for each frequency test listed.

(2) CONTINUOUS TUNING. - To receive a signal whose frequency does not terminate in whole 100-cycle increments (for example, a frequency of 2.00005 mc), the continuous tuning method is employed using the FREQ VERNIER ± 150

CPS panel control. The dual control, with the switch knob at VAR, will provide continuous receiver tuning of more than 150 cycles above and below the MEGACYCLES dials set frequency. Refer to Section 3, Operation, for a complete description of the continuous tuning procedure.

(a) Adjust the generator for a 2.500050 mc, 10 microvolt, unmodulated test signal.

(b) Set the MODE switch at SSB, and the BANDWIDTH switch at LSB.

(c) Set the MEGACYCLES dials to read 2.5010 mc.

(d) Set the large FREQ VERNIER ± 150 CPS knob at VAR, and adjust the small knob to receive the test frequency.

(e) The panel meter should indicate presence of a signal, and a 1000 cycle note should be heard in the speaker.

d. AM MODE OPERATION. - Receiver operation for the AM mode should be verified and the agc operation checked by performing the following:

(1) Connect the signal generator to the 50 Ω ANT connector (A1A1J1). Adjust generator for a 2.0000 mc, 100 microvolts, test signal, modulated 30 per cent at 400 cycles.

(2) Set the MODE switch at AM, and the BANDWIDTH switch at 8 KC.

(3) Set the MEGACYCLES dials to 2.0000 mc.

(4) The signal level meter on the panel should indicate and a 400 cycle tone should be heard at the speaker.

(5) Set the METER FUNCTION switch at PHONES LEVEL. Adjust the PHONE LEVEL control for a reading of +5 db on the panel meter using the output level scale.

(6) Gradually increase the generator output level to 2.0 volts, noting the panel meter reading. The meter reading should change 6 db or less.

e. CW MODE OPERATION. - To check receiver operation using the CW reception mode, perform the following steps:

(1) Connect signal generator to the 50 Ω ANT connector (A1A1J1). Adjust generator for a 2.0000 mc, 10 microvolt, unmodulated test signal.

(2) Set the MODE switch at CW, and the BANDWIDTH switch at 8 KC.

(3) Set the large BFO ± 3 KC knob at VAR and adjust the small knob.

(4) Note the beat-note heard in the speaker. A zero-beat should occur at a central position of the small control knob.

f. FSK MODE OPERATION. - To verify receiver operation using the FSK mode, connect a teletype unit to the TELETYPE terminals on the receiver panel.

If Teletypewriter Set AN/TGC-14A(V), or similar equipment which supplies its own loop potential is used, place the TELETYPE MODE switch in the EXT BAT position. If a teletype unit which does not supply its own loop potential is used, place the TELETYPE MODE switch in the INT BAT position. Select a known broadcast station employing two-tone fsk transmissions for the set.

Note

When using Teletypewriter Set AN/TGC-14A(V), connect terminal box ground lead to (-) TELETYPE terminal on receiver panel.

- (1) Set the MODE switch at FSK, and the BANDWIDTH to USB or LSB depending upon the received signal characteristics.
- (2) Energize the auxiliary teletypewriter equipment (refer to instructions for the equipment).
- (3) Set the MEGACYCLES dials to receive the transmitter fsk channel.
- (4) Note the teletypewriter copy as a function of receiver operation.

g. MONITORING WITH HEADPHONES. - To verify operation of the headphone monitoring circuit, plug a headphone set into the PHONES jack and repeat the previous performance step of paragraph 2-5d. Note that the PHONE LEVEL control will adjust the level of volume at the headphones.

h. OPERATION OF SPECIAL CIRCUITS. - The noise blanking and notch filter circuits in the receiver are considered special circuits. While not essential for reception, they are provided as a supplement to enhance receiver performance. Tests of these circuits consist of operating the controls and observing the degree to which the circuit performs its intended function.

(1) NOISE BLANKING. - The noise blanking circuit (module A1A2A4) employs a gated amplifier stage in the main signal path to effectively open (blank) the signal circuit when a noise impulse is received. To test the noise blanking circuit, tune the receiver to a particularly noisy portion of the tuning range where impulse type noise exists, and monitor the noise using the loudspeaker. Rotate the NOISE BLANKING control in a clockwise direction and note an appreciable drop in the noise level. If an am or cw transmission is received, operation of the noise blanking circuit is evident by a distortion of the signal.

(2) NOTCH FILTER. - The notch filter circuit (module A1A1A4) contains a broad and a sharp bandpass rejection-filter circuit. Either filter can be inserted into the receiver main signal path and its relative position shifted over a nominal signal path bandwidth of 10 kc. To test the notch filter circuit, apply a signal generator test frequency or tune the receiver to any broadcast. Place the WIDTH control in the SHARP position and adjust the POSITION control, noting the rejection of a portion or all of the received test signal. Repeat this procedure with the WIDTH control at the BROAD position.

Note

Use of the notch filter circuit when the BANDWIDTH switch is in the 350 CPS position is impractical. The rejection notch will effectively remove all signals within this relatively narrow bandpass.

i. OPERATION WITH OTHER EQUIPMENT. - The efficiency of the receiver when used with teletype or other terminal equipment should be verified by actual operation. The following suggestions may aid in making these tests meaningful:

(1) RECEIVER. - Condition the receiver for the tests by initially pre-setting all controls according to table 3-2, as appropriate. Follow the instructions contained in paragraph 2-5c when tuning the receiver.

(2) OTHER EQUIPMENT. - Make sure that the external auxiliary equipment is in good operating condition prior to the test. When connecting external equipment, follow also the instructions contained in the technical manual for such equipment. Allow ample warm-up time if required.

2-6. PREPARATION FOR RESHIPMENT.

a. EQUIPMENT DISASSEMBLY. - The following steps form a logical sequence for receiver preparation prior to reshipment.

(1) Place the POWER switch in the OFF position and remove all primary power by opening the local power source switches.

(2) Disconnect all external cables from the panel connectors.

(3) If rack mounted, remove the receiver (see paragraph 2-4b and reverse the installation procedure).

(4) Replace the transit case and/or case cover (see paragraph 2-4a).

(5) Collect all re-usable mounting hardware, external cable connectors, the two primary power cables (ac and dc), and the two technical manuals. Spare parts to be returned with the receiver should be inventoried and replaced in their original containers, if possible. Provisions should be made for replacement of missing or damaged items prior to shipment.

b. REPACKAGING. - Refer to the latest packaging specifications for the instructions and requirements for packaging and packing the receiver. Also observe the following:

(1) Do not remove the normal complement of plug-in circuit modules for reshipment of equipment.

WARNING

Transit Case C43611-G1 is equipped with a pressure relief valve to permit safe transportation by aircraft. Valve MUST be opened (turned fully counterclockwise) prior to shipment, whether set is packed or unpacked.

SECTION 3

OPERATION

3-1. FUNCTIONAL OPERATION.

Radio Receiver R-1490/GRR-17, a part of Radio Receiving Set AN/GRR-17, is a light weight, low power consumption, solid state receiver, operable from either a 115 vac or a 24 vdc primary power source. The receiver is tuned over a frequency range from 2.0 to 30.0 mc, in steps of 100 cycles, by setting five frequency indicating dials to the desired signal frequency. Continuous tuning is also provided. The receiver is intended for general ground installations and the reception of usb or lsb (A3j), am (A3), cw (A1), and fsk (F1) broadcasts.

Receiver operation is characterized by a high frequency-stability permitting long periods of unattended operation, a high dynamic (input signal) range, and practically instantaneous tuning when the tuning dials are set to a signal frequency.

3-2. OPERATING PROCEDURES.

a. DESCRIPTION OF CONTROLS. - All controls for receiver operation are located on the front panel. Figure 3-1 shows the location of each control and table 3-2 contains a functional description of each control, jack, connector, and indicating device on the front panel.

b. MODES OF OPERATION. - Table 3-1 lists the receiver operating modes, the corresponding bandwidth selection for each mode, and indicates those modes where bfo operation is available. The bandwidths given for each mode are for normal receiver operation.

All operating modes can be monitored using either the panel mounted loudspeaker or a headset connected to the PHONES jack. Individual signal level controls are provided on the panel.

c. SEQUENCE OF OPERATION. (See also table 3-3.)

CAUTION

Before starting equipment for the first time, make sure that the primary power source to be used corresponds with the receiver requirements according to the information in paragraph 2-2a. Verify that the correct power connector on the panel has been connected to the primary source.

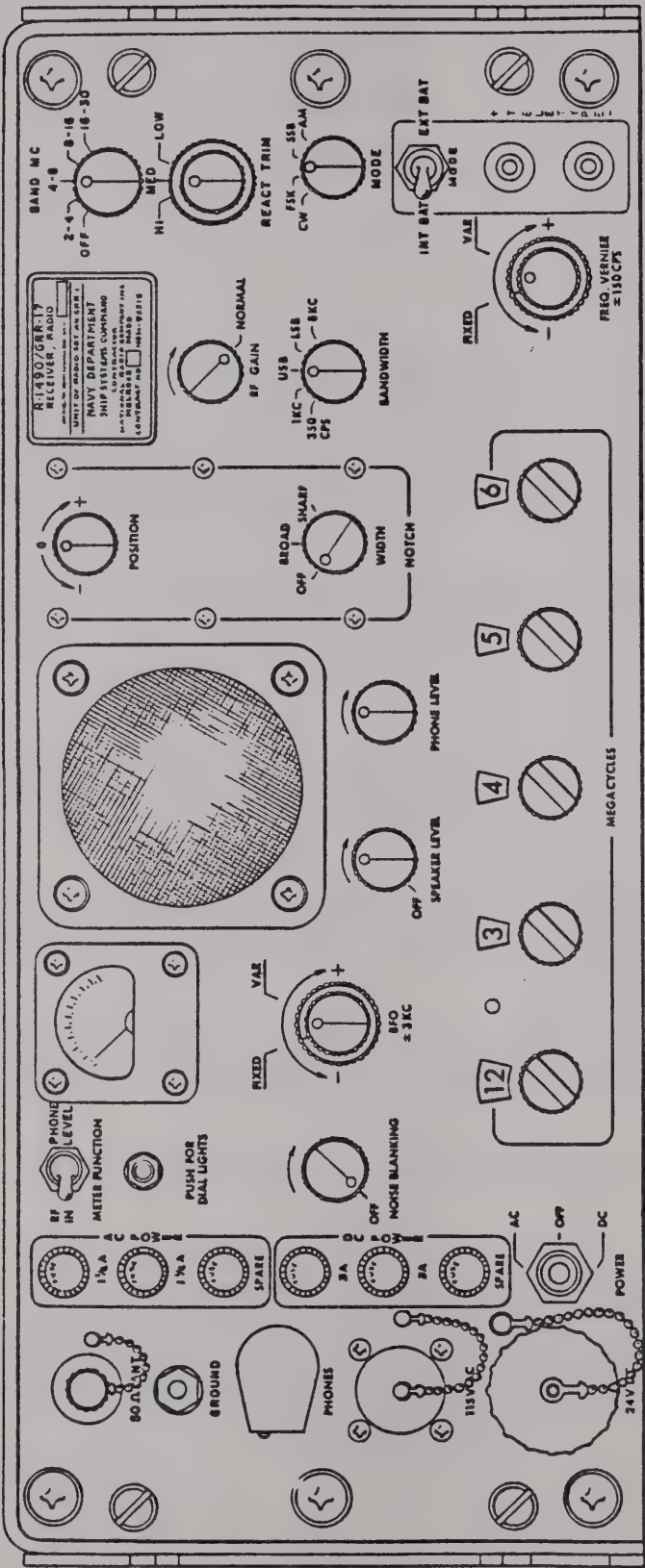


Figure 3-1. Radio Receiver R-1490/GRR-17, Front View

TABLE 3-1. OPERATING MODES AND BANDWIDTH SELECTIONS

OPERATING MODE	NORMAL BANDWIDTH SELECTION	BFO OPERATION AVAILABLE
CW	350 CPS or 1 KC	YES
FSK	USB or LSB	YES
SSB	USB or LSB	NO
AM	8 KC	NO
<p>Note</p> <p>For CW mode reception from an ssb transmitter using an uncompensated (off-set) sideband transmission, use the applicable USB or LSB BANDWIDTH switch position. The 350 CPS or 1 KC positions can impair reception unless the receiver is retuned to place the signal well within the narrower bandwidth.</p>		

TABLE 3-2. OPERATING CONTROLS AND DEVICES

CONTROL NAME	PRESET POSITION	CONTROL FUNCTION
POWER, AC/OFF/DC	OFF	Switch to control and select primary power source.
METER FUNCTION, RF IN/PHONE LEVEL	RF IN	Switch controlling circuit to be monitored by panel meter.
Signal Level Meter	None	Monitors signal level <u>or</u> audio output at headphone circuit.
PUSH FOR DIAL LIGHTS	Normally <u>off</u>	Switch for MEGACYCLES dials illumination.
NOISE BLANKING	OFF	Control to adjust the degree of impulse noise rejection.
BFO ± 3 KC, -/+, FIXED/VAR	Small knob: Center Large knob: FIXED	Dual concentric control. Large knob (switch) selects either a fixed or variable bfo frequency, controlled by small knob.
SPEAKER LEVEL	Clockwise 1/2 turn	Control to adjust speaker level.
PHONE LEVEL	Fully counter- clockwise	Control to adjust phone level.

TABLE 3-2. OPERATING CONTROLS AND DEVICES (Cont)

CONTROL NAME	PRESET POSITION	CONTROL FUNCTION
MEGACYCLES	Any position	Five switches to select signal frequency in megacycles. Dot denotes decimal point position.
NOTCH WIDTH, OFF/BROAD/SHARP	OFF	Switch selecting a broad or a sharp notch bandwidth.
NOTCH POSITION, -/+	0 (center)	Control to position rejection notch in receiver bandpass.
RF GAIN	NORMAL	Control to manually adjust the receiver rf gain.
BANDWIDTH, 350 CPS/ 1 KC/USB/LSB/8 KC	8 KC	Switch to select I-F bandwidth.
BAND MC	OFF	Switch to select proper antenna trimming circuit.
MODE, CW/FSK/SSB/ AM	AM	Switch to select operating modes.
REACT TRIM, HI/MED/ LOW	None	Dual concentric control. Large knob compensates for antenna resistive mismatch; small knob compensates for reactive mismatch.
FREQ VERNIER ± 150 CPS, -/+, FIXED/VAR	Small knob: Center Large knob: FIXED	Dual concentric control. Large knob (switch) selects either a fixed or variable vfo frequency controlled by small knob.
TELETYPE MODE	EXT BAT	Switch to select either external or internal loop potentials for teletype operation.
50 Ω ANT		Connector for antenna transmission line.
PHONES		Jack for external headset, or 600 ohm line.
115 V AC		Connector for ac primary power.
24 V DC		Connector for dc primary power.

TABLE 3-2. OPERATING CONTROLS AND DEVICES (Cont)

CONTROL NAME	PRESET POSITION	CONTROL FUNCTION
AC POWER		Fuses for ac primary power.
DC POWER		Fuses for dc primary power.
TELETYPE		Terminals for external teletypewriter. (Signal Line)

(1) STARTING.

(a) Set the POWER switch from OFF to the correct on position. (AC for ac and DC for dc power source.)

(b) Press the PUSH FOR DIAL LIGHTS switch and note that the MEGACYCLES selector dials are illuminated. Release the switch.

(c) If the desired signal frequency terminates in whole 100 cycle increments, use the incremental tuning method. If not, use the continuous tuning method.

(2) INCREMENTAL TUNING. - The incremental tuning method is used when the desired signal frequency terminates in a whole 100 cycle step. For example: 2.0050 mc or 12.0500 mc and 29.9902 mc. The last frequency is used as an example for the following incremental tuning procedure:

(a) Set the first (left hand) MEGACYCLES dial to read 29. Note the decimal point marked on the receiver panel.

(b) Set the remaining four dials, in succession, to read 9, 9, 0, 2.

(c) If an antenna other than 50 ohms is used, set the BAND MC switch to the range in which the desired signal frequency falls (in this case, the 16-30 position). Adjust the REACT TRIM and HI/MED/LOW controls for maximum output while listening to a known signal frequency.

Note

Under some combinations of antenna trimming circuit control settings, the desired signal may be considerably reduced.

(d) Adjust the SPEAKER LEVEL or the PHONE LEVEL control as required to obtain the desired output level.

(3) CONTINUOUS TUNING. - The continuous tuning method is used when the desired signal frequency terminates in other than whole 100 cycle steps. For example: 2.00505 mc, 12.05008 mc, and 29.99025 mc. Receiver tuning using the continuous method is identical to the incremental tuning method previously

described with the addition of another control adjustment. The latter frequency above will be used as an example:

(a) Set the MEGACYCLES dials to read 29.9902.

(b) Place the large knob of the FREQ VERNIER ± 150 CPS control at VAR. Adjust the small knob in a clockwise direction for a maximum receiver output indication.

(c) Repeat step (2)(c) above.

(d) The small FREQ VERNIER ± 150 CPS knob will adjust receiver tuning at least 150 cycles above or below the 100-cycles digit set on the fifth MEGACYCLES dial. Consequently, for the frequency example of 29.99025 mc the small knob should be turned in a clockwise (positive) direction, until the signal is received.

(4) OTHER OPERATING ADJUSTMENTS.

(a) USE OF MODE SELECTOR. - For the reception of unmodulated cw signals use the CW switch position; a ± 3 kc beat frequency is provided by adjustment of the BFO ± 3 KC control knobs. For modulated cw reception (mcw) and am reception, use the AM switch position. For reception of two-tone teletype signals (fsk), use the FSK switch position. For reception of either the upper or lower sideband of a single-sideband voice transmission (A3j), use the SSB switch position.

When a cw transmission is to be received from an ssb station which is employing a keyed 800 cycle sideband, select the appropriate USB or LSB bandwidth. If the sharper 350 CPS or 1 KC BANDWIDTH switch positions are used, the receiver tuning must be changed to place the 800 cycle sideband within the receiver bandpass. For a usb transmission, increase the MEGACYCLES dials setting by 800 cycles, and for an lsb transmission decrease the dial setting 800 cycles.

(b) USE OF BANDWIDTH SELECTOR. - The BANDWIDTH selector permits the selection of a 350 cycle or 1 kc receiver passband for the reception of conventional cw signals, individual 300 to 3500 cycle passbands for usb or lsb signal reception, and an 8 kc passband for am signal reception. Table 3-1 lists the bandwidths normally employed for each operating mode. In the event of cw reception from an ssb transmitter employing an off-set keyed sideband, use the applicable USB or LSB BANDWIDTH switch positions rather than the conventional 350 CPS or 1 KC positions.

(c) USE OF FREQ VERNIER ± 150 CPS CONTROL. - To tune the receiver incrementally, in steps of 100 cycles, the large (concentric) control knob is set at FIXED to disable the frequency vernier circuit. For continuous receiver tuning, limited to plus-or-minus 150 cycles from the signal frequency set at the MEGACYCLES tuning dials, the large knob is set at VAR to enable the vernier tuning circuit. The small knob now serves as a vernier tuning control.

(d) USE OF NOISE BLANKING CONTROL. - In the OFF control position, the noise blanking circuit is disabled. A clockwise rotation of the NOISE BLANKING control will cause rejection of unwanted impulse-type noise accompanying the signal. The rejection level, relative to the noise and signal amplitudes, is determined by the degree of control rotation. Normally, the control setting is

adjusted until signal distortion occurs. Then, the control is backed off to reduce distortion. At a maximum clockwise control setting both the noise and signal peaks are rejected.

(e) USE OF NOTCH FILTER CONTROLS. - In the OFF position, the NOTCH WIDTH control disables the notch filter circuit. In the BROAD and SHARP positions, a wide or narrow-band rejection filter is inserted into the receiver signal path. The POSITION control, in effect, shifts the rejection filter "notch" position to remove unwanted signal components within the receiver band-pass.

Normally, the SHARP switch position is used for rejection of interfering cw signals or heterodynes, and the BROAD position is used to reject larger segments of interference such as am broadcasts.

(f) USE OF BFO ± 3 KC CONTROL. - When the large (concentric) control knob is at the FIXED position, the adjustable-frequency bfo circuit (5 mc ± 3 kc) is disabled and a fixed frequency (5 mc) substituted when using the CW, FSK, and SSB MODE switch positions. No bfo operation is provided for the AM mode. In the VAR position, the adjustable-frequency bfo circuit is used for the CW and FSK MODE switch positions only; the fixed frequency circuit is retained for the SSB mode. The small control knob adjusts the beat-note pitch for cw reception and for monitoring fsk reception.

(g) USE OF RF GAIN CONTROL. - Usually, the RF GAIN control is set at the NORMAL position for signal level readings on the panel meter (METER FUNCTION switch at the RF IN position). Under some operating conditions, the reception of cw signals, for example, the RF GAIN control is adjusted to prevent receiver overload during strong signal reception. In this event, control adjustment will affect the panel meter reading (RF IN switch position).

(h) USE OF METER FUNCTION SWITCH. - The METER FUNCTION switch selects the receiver function monitored by the signal-level panel meter. In the RF IN position, conventional "S" meter operation is provided for all but the cw reception mode. In the PHONE LEVEL position, the meter monitors audio output at the PHONES jack on the panel. Individual scale calibrations are provided for each meter function.

(i) USE OF "PUSH FOR DIAL LIGHTS" SWITCH. - Window illuminating lamps at the MEGACYCLES tuning dials are controlled by the PUSH FOR DIAL LIGHTS momentary push-button switch.

(j) USE OF PHONES JACK. - The PHONES jack on the front panel is an audio output connection for an external headset or other terminal equipment with a load impedance of 600 ohms. Maximum undistorted output at this connection is 15 milliwatts. When the METER FUNCTION switch is at PHONE LEVEL, the panel meter reads the output level at the PHONES jack.

(k) USE OF TELETYPE MODE SWITCH AND TELETYPE TERMINALS. - The TELETYPE terminals on the panel are intended for connection to Teletypewriter Set AN/TGC-14A(V) or equivalent equipment when the TELETYPE MODE switch is in the EXT BAT position. This teletype output circuit is known as a "dry loop" because the terminals provide a switching function only and an external loop potential must be supplied by the attached teletype equipment. When the TELETYPE MODE switch is in the INT BAT position, the TELETYPE

terminals may be connected to equipment which does not supply its own loop potential. In this case, the AN/GRR-17 teletype output circuit provides the loop potential and is known as a "wet loop". When connecting teletype equipment to the TELETYPE terminals, polarity marks (+ and -) must be observed.

Note

When using Teletypewriter Set AN/TGC-14A(V), connect terminal box ground lead to (-) TELETYPE terminal on receiver panel.

(1) USE OF BAND MC SWITCH AND REACT TRIM, HI/MED/LOW CONTROLS. - The BAND MC switch selects one of four antenna transformers on the antenna trimming circuit module, each of which covers a portion of the frequency range of 2 to 30 mc. The HI/MED/LOW switch (large knob of the dual concentric control) tunes the selected antenna transformer to the range which most nearly approximates the impedance of the antenna connected to the receiver. The REACT TRIM control is an antenna trimming capacitor and tunes the primary of the selected antenna transformer to a close impedance match. When the BAND MC switch is in the OFF position, the antenna trimming circuit is bypassed, and the REACT TRIM, HI/MED/LOW controls do not function.

Note

The BAND MC switch and REACT TRIM, HI/MED/LOW controls are used when random-length antennas whose values are not nominally 50 ohms are connected to the receiver. When a 50 ohm antenna which is cut for the incoming signal frequency is used, the antenna trimming circuit should be bypassed by turning the BAND MC switch to OFF.

(5) STOPPING. - To stop the receiver, rotate the RF GAIN, PHONE LEVEL, and SPEAKER LEVEL controls fully counterclockwise. Place the POWER switch at the OFF position.

(6) AFTER USE. - No provisions are made for a "stand-by" condition of the receiver. Between periods of actual operation, the receiver may remain energized but the following steps are suggested by good operating practice.

- (a) Lower the RF GAIN and PHONE or SPEAKER LEVEL settings.
- (b) Disconnect the headset, etc., or other terminal equipment which is not a part of the permanent installation.
- (c) Log any abnormal performance noted during operation.
- (d) Perform any maintenance checks for the receiver described in the Maintenance Standards information in Section 5, Maintenance.

d. INDICATOR PRESENTATIONS.

(1) MEGACYCLES DIALS. - The signal frequency to which the receiver is tuned appears directly in the MEGACYCLES dials windows when the selector

dials are set. Note the decimal point on the panel between the first and second dial windows. The first dial registers the first one or two digits of the signal frequency ranging from 02 to 29, in megacycles. The remaining four dials to the right of the decimal point register the remainder of the signal frequency in divisions of 100 kc, 10 kc, 1 kc, and 100 cycles, respectively, each of the four dials having digits ranging from 0 to 9. Consequently, the highest frequency to which the MEGA-CYCLES dials can be set is 29.9999 mc. For reception at 30.0 mc, the FREQ VERNIER ± 150 CPS control extends the receiver tuning range ± 100 cycles.

(2) SIGNAL LEVEL METER. - The panel meter located near the speaker has a dual scale calibration in db. The signal level ("S" meter) scale is calibrated in db above the agc threshold, and the output level scale is calibrated from 0 dbm to ± 12 dbm. The METER FUNCTION switch selects the meter range.

e. NONOPERATING CONTROLS. - The following controls are not located on the receiver panel but are accessible following removal of the dust cover. They are intended for use by technicians in adjusting and calibrating the receiver and should be adjusted by a qualified technician only.

(1) CRYSTAL CALIBRATION ADJUSTMENT. - A trimmer capacitor located on the frequency standard module A1A1A1.

(2) RESERVE GAIN CONTROL. - A potentiometer adjustment located on the reserve gain amplifier (A2), p/o the 1st i-f module A1A2A3.

(3) AGC LEVEL CONTROL. - A potentiometer adjustment located on the agc amplifier (A2), p/o the 2nd i-f and agc amplifier module A1A2A6.

(4) VHF OSCILLATOR CONTROL. - A potentiometer adjustment located on the phase-locked loop (A3), p/o the front end module A1A2A2.

3-3. SUMMARY OF OPERATION.

A summary of the procedures for receiver operation in proper sequence, in the form of step-by-step instructions, is given in table 3-3. These instructions include the procedures for starting and stopping the receiver, tuning, mode selection, and changing frequency.

3-4. EMERGENCY OPERATION.

a. PARTIAL FAILURE. - Normally, good maintenance procedures require that electronic equipment be shut down for repairs as soon as a significant defect develops. Under unusual or emergency conditions, however, loss of equipment service for any length of time may not be acceptable, and a substitute method of operation must be found when possible. The substitute method will, in most cases, involve a reduction of equipment capabilities. If alternate equipment is not available, the lower operating efficiency must be accepted. When the emergency period is over, steps should be taken to restore the equipment to normal operation. Subject to the foregoing, the following emergency procedures are suggested.

(1) LOUDSPEAKER. - In the event of failure of the loudspeaker or its audio amplifier the signal monitoring function can be continued, using a headset connected to the PHONES jack. Individual loudspeaker and headset amplifiers with level controls are incorporated in the receiver. Conversely, the loudspeaker is a

TABLE 3-3. RADIO RECEIVER R-1490/GRR-17,
SUMMARY OF OPERATION

1. STARTING THE RECEIVER	
Step 1.	Set the POWER switch at AC or DC, depending on power source.
Step 2.	Set NOTCH WIDTH at OFF, NOISE BLANKING at OFF. Set BAND MC and HI/MED/LOW switches for antenna being used.
Step 3.	Set RF GAIN control at NORMAL, use SPEAKER LEVEL control to adjust loudspeaker output level.
2. TUNING	
Step 1.	Set the five MEGACYCLES dials to signal frequency, in megacycles.
Step 2.	If signal frequency does not terminate in an even 100-cycle increment, use continuous tuning method.
Step 3.	For continuous tuning, set FREQ VERNIER ± 150 CPS large (outer) knob at VAR. Adjust the smaller (inner) knob for maximum signal.
3. RECEPTION MODES	
Step 1.	<u>CW</u> . Set MODE switch at CW and BANDWIDTH switch at 1 KC. Set BFO ± 3 KC switch large (outer) knob to VAR and adjust smaller (inner) knob for desired beat note.
Step 2.	<u>FSK</u> . Set MODE switch at FSK and BANDWIDTH switch at either USB or LSB, depending on signal characteristics. Set TELETYPE MODE switch as required.
Step 3.	<u>SSB</u> . Set MODE switch at SSB and BANDWIDTH switch at either USB or LSB, depending on signal characteristics.
Step 4.	<u>AM</u> . Set MODE switch at AM and BANDWIDTH switch at 8 KC.
4. OTHER ADJUSTMENTS	
Step 1.	<u>NOISE BLANKING</u> . To reject impulse-type noise, turn NOISE BLANKING control clockwise until noise is reduced.
Step 2.	<u>NOTCH FILTER</u> . To reject interference in signal channel, set NOTCH WIDTH control at BROAD or SHARP. Adjust NOTCH POSITION control to remove interference.
Step 3.	<u>Signal Level Meter</u> . To monitor signal level, set METER FUNCTION switch at RF IN. To monitor PHONES output, set switch to PHONE LEVEL.

TABLE 3-3. RADIO RECEIVER R-1490/GRR-17,
SUMMARY OF OPERATION (Cont)

5. STOPPING THE RECEIVER
Step 1. Turn RF GAIN and SPEAKER LEVEL controls fully counterclockwise.
Step 2. Set the POWER switch at OFF.

normal substitute for the headset for monitoring purposes only. No provision has been made for attachment of external equipment to the loudspeaker output circuit.

(2) AGC CIRCUITS. - Failure of the receiver agc circuits to control receiver gain will not prevent reception and the set will usually be operative, subject to a degree of signal fading and signal overload. In this event the RF GAIN control should be retarded from the NORMAL position to prevent overload when a strong signal is being received.

(3) NOISE BLANKING. - Failure of the noise blanking circuit will not prevent signal reception, but copy can be affected if a high level of noise interference is present. Depending upon the reception mode employed, in some instances the noise interference can be reduced by selecting a narrower BANDWIDTH switch position.

(4) INTELLIGENCE FILTER. - In some instances, failure of the intelligence filter circuit will not prevent reception but only the ability to use all positions of the BANDWIDTH switch. In this event, depending upon the reception mode in use, the BANDWIDTH switch position can be changed to resume signal reception.

(5) PRIMARY POWER. - Interruption of the primary power source to the receiver can be remedied by an alternate power source of 115 vac or 24 vdc. The operator should be familiar with the power distribution system at the installation site and the availability of alternate or emergency power sources, and should be able to shift to an alternate source in an emergency.

b. OTHER THAN NORMAL. - In the event of complete failure of the receiver to operate using one of the reception modes, in an emergency reception can be resumed by selecting another appropriate mode and adjusting the receiver controls to permit signal reception. The following emergency methods will provide satisfactory signal reception accompanied in some instances by a degree of signal degradation.

(1) CW RECEPTION USING SSB MODE. - If the cw mode is inoperative, perhaps because of bfo circuit failure, cw reception can be continued by using the ssb mode and detuning the receiver to substitute the 5 mc carrier injection frequency for the bfo frequency.

(a) To use the ssb mode for the reception of cw signals, set the MODE switch at SSB and the BANDWIDTH switch at either USB or LSB.

(b) For the USB bandwidth, detune the receiver 1 kc below the signal frequency. A 1000-cycle beat note will be obtained. If you wish to change the beat note pitch, use the continuous tuning method and adjust the FREQ VERNIER ± 150 CPS control.

(c) For the LSB bandwidth, detune the receiver 1 kc above the signal frequency. Use the continuous tuning method to vary the beat note pitch.

Note

A final tuning adjustment for CW mode reception when using the SSB mode will combine adjustment of the FREQ VERNIER ± 150 CPS control with several trial positions of the 100 cps MEGACYCLES tuning dial.

(2) AM RECEPTION USING SSB MODE. - If the am operating mode is not functioning, am reception can be resumed by using the ssb mode and retuning the receiver slightly to superimpose the 5 mc carrier injection frequency upon the am signal carrier.

(a) Set the MODE switch at SSB, and the BANDWIDTH switch at either USB or LSB.

(b) Use the continuous tuning method and adjust the FREQ VERNIER ± 150 CPS control to obtain a "zero beat" with the signal carrier.

c. JAMMING. - Briefly, the jamming of transmitted signals is a deliberate attempt to prevent reception by the emission of interfering signals at or near the signal frequency. Unusual reception can be caused by jamming, interference from other stations, or a defect in the receiver. To avoid confusion as to the source of unusual reception, disconnect the receiver antenna. If the interference persists, it is probably being generated by a defective receiver circuit. If the interference stops, it is not caused by a receiver defect.

(1) TYPES OF JAMMING. - Broadly classified, jamming signals are either of the continuous wave or modulated wave type. Continuous wave jamming is a steady, unmodulated carrier, slightly off frequency to produce a constant beat-note in the receiver output. Modulated jamming appears in a wide variety of forms ranging from music, speech, various tone combinations, and random keying, to actual noise modulation, swept frequency, and various stepped tone patterns. Depending upon its characteristics, modulated jamming is often referred to by a name which implies its major effect, such as spark, sweep-through, bagpipes, gulls, noise, or tone.

(2) ANTIJAMMING PROCEDURES. - When the presence of jamming is suspected or recognized, immediately notify the superior officer and continue to operate the receiver. Continued operation is a basic anti-jamming technique; if the receiver is shut down, the jammer has accomplished his purpose. The following anti-jamming procedures are based upon general communications practices plus consideration of the receiver design features. Other tactical considerations concerning anti-jamming and countermeasure procedures will govern in cases of conflict with this manual.

(a) Continue to operate the receiver.

(b) If the jamming signal is very strong, adjust the RF GAIN control to prevent receiver blocking.

(c) When using the cw mode, set the BANDWIDTH switch at the narrowest bandwidth position, 350 CPS.

(d) Use the continuous tuning method and detune the receiver slightly to improve the desired signal, if possible.

(e) Adjust the NOISE BLANKING control to reduce impulse noise.

(f) Adjust the NOTCH controls to reject interference close to the desired signal frequency.

(g) Remember that the success or failure of antijamming methods will depend largely on the signal-to-noise ratio between the desired signal and the jamming signal. A combination of the steps described may work even though an individual step is not successful.

(h) Single sideband channels, because of their relatively narrow bandwidths, are not as affected by broadband noise-modulated jamming. If am reception is jammed and conditions permit, a shift to single sideband communication modes should be considered.

(i) In the event that a communication channel remains jammed after all possible antijamming techniques have been tried, a shift in operating frequency is indicated. The shift should be well outside the area of jamming frequencies.

(j) At the first opportunity, make an accurate record of the jamming signal characteristics, the apparent effectiveness of the jamming, and the success or failure of each antijamming measure attempted.

3-5. OPERATOR'S MAINTENANCE.

a. GENERAL. - Electronic technicians are usually responsible for the maintenance and repair of receiving equipment, although routine items of preventive maintenance which do not require elaborate test set-ups are normally assigned to the operator. Basic trouble shooting and the repair of minor defects may also be required of operating personnel from time to time. In order to meet this responsibility, the operator must have a thorough knowledge of the equipment including a complete familiarity with the function of all controls and the procedures governing their use. A general knowledge of circuit theory should be acquired so that the location and probable cause of minor electrical or mechanical failure may be determined. In this manner, minor troubles can often be corrected before they become serious. Under normal conditions, however, major repairs or precise circuit adjustments should not be attempted by other than qualified technicians.

b. OPERATING CHECKS. - The R-1490/GRR-17 is designed to operate for long periods of time without requiring adjustments other than those involved in changing the operating frequency or mode. The following checks should be performed periodically by the operator as preventive maintenance of the equipment.

(1) TUNING PROCEDURE. - Repeat the steps contained in the Summary of Operation, table 3-3, to verify the receiver tuning function.

(2) CONTROL FUNCTIONS. - Check each operating control and its function by tuning the receiver to a local station and noting the effect of each control on the received signal.

(a) MODE SWITCH. - The bfo circuit should be operable in the CW and FSK switch positions. (Use the BFO ± 3 KC control during this check.)

(b) BANDWIDTH SWITCH. - Place the BANDWIDTH switch successively in each position. Note the increase in selectivity evident at the narrower bandwidth positions.

(c) NOISE BLANKING CONTROL. - Adjust the NOISE BLANKING control and note the degree of noise reduction, accompanied by program distortion at the extreme control setting.

(d) NOTCH CONTROLS. - Employ both the BROAD and SHARP positions of the WIDTH control and note the ability to reject portions of the received signal channel as the POSITION control is adjusted.

(e) METER FUNCTION SWITCH. - Use both the RF IN and the PHONE LEVEL switch positions and note that the panel meter functions as a tuning meter in the RF IN position. In the PHONE LEVEL position, the PHONE LEVEL control should also control the panel meter reading.

(f) BAND MC SWITCH AND REACT TRIM, HI/MED/LOW CONTROLS. - Place the BAND MC switch in each of its four operating positions. For each position, vary the REACT TRIM and HI/MED/LOW controls, noting the effect on receiver sensitivity.

c. PREVENTIVE MAINTENANCE. - The Maintenance Standards information contained in Section 5, Maintenance, provides maintenance and operating personnel with a systematic method of checking the receiver and performing preventive maintenance.

d. EMERGENCY MAINTENANCE. - Operating personnel must expect the possibility of receiver failure when technician services are not immediately available. In an emergency, the need for keeping the receiver in operation is of utmost importance and the operator must be able to recognize major receiver failure symptoms, determine the particular area of trouble in the set, and make emergency repairs when possible. It is not practical to discuss every type of failure which may possibly occur. Instead, a general outline of trouble shooting techniques will be presented to aid the operator in developing a systematic approach to the problem.

(1) ISOLATING TROUBLE. - The receiver consists of a number of related functional circuits, mounted on individual plug-in circuit modules, each performing a specific task which contributes to receiver operation. Depending on the particular circuit involved, trouble symptoms can range from a noticeable reduction in receiver sensitivity or selectivity to a complete breakdown of the set. A haphazard search through the circuits will not accomplish much except by accident. A more effective approach concerns the identification of a faulty circuit, based upon observed trouble symptoms such as an abnormal meter reading, unnatural response of panel controls, etc. Make the following checks before attempting a detailed examination of the receiver.

(a) Check that all panel controls are in the intended positions and have not been accidentally moved.

(b) If the receiver is completely inoperative (no illumination at the MEGACYCLES dials windows when the PUSH FOR DIAL LIGHTS switch is pressed), check the primary power fuses located on the front panel. Verify that the primary power at the installation site is available for distribution.

(c) If the receiver is operative but reception is weak, check the antenna installation and connections. If the antenna transmission line is fed through a distribution panel, check the panel connections.

(d) Inspect all external cable connections at the front panel and make sure that they are secure.

(2) TROUBLE SHOOTING GUIDE. - Table 3-4 is intended to serve as a guide to help the operator find and correct minor troubles. In the event of major trouble, the technician should refer to the established trouble shooting procedures contained in Section 4, Trouble Shooting, and the Maintenance Standards information contained in Section 5, Maintenance, in this manual.

TABLE 3-4. RADIO RECEIVER R-1490/GRR-17,
TROUBLE SHOOTING GUIDE

INDICATION	PROBABLE CAUSE	REMEDIAL ACTION
1. Receiver dead. No lights when PUSH FOR DIAL LIGHTS button is pressed.	1. a. POWER switch at wrong position. b. Panel fuse(s) blown. c. No primary power at installation site.	1. a. Correct POWER switch position. b. Check, replace fuse(s). c. Check, restore power at installation site.
2. Operation all modes but FSK. No output at TELETYPE terminals.	2. a. Signal line dc voltage not supplied from teletype unit or receiver. b. Faulty fsk converter card (A2), p/o detector/amplifier module A1A2A7.	2. a. Check teletype unit and receiver TTY power supply. Restore dc signal-line power. b. Replace detector/amplifier module A1A2A7.

TABLE 3-4. RADIO RECEIVER R-1490/GRR-17,
TROUBLE SHOOTING GUIDE (Cont)

INDICATION	PROBABLE CAUSE	REMEDIAL ACTION
3. FSK mode functions but no output at speaker or headset.	3. Faulty detector/amplifier card (A1), p/o detector/amplifier module A1A2A7.	3. Replace detector/amplifier module A1A2A7.
4. Operation all modes, but no noise blanking.	4. Faulty noise blanking module A1A2A4.	4. Replace noise blanking module A1A2A4.
5. Receiver weak or dead over small part of frequency range, only (2-3, 3-5, 5-8, 8-12, 12-19, or 19-30 mc).	5. Faulty filter section in input filter module A1A2A1.	5. Replace input filter module A1A2A1.

SECTION 4

TROUBLE SHOOTING

4-1. INTRODUCTION.

This section contains information to enable the electronics technician to efficiently locate the cause of equipment malfunction and abnormal performance. Effective trouble shooting of electronic equipment consists of recognizing the fault symptom, identifying the circuit responsible, and isolating the defective component or maladjustment in order to repair the equipment and return it to normal operation. To perform these steps quickly and efficiently, the technician should clearly understand the purpose and operation of each functional circuit in the equipment, and follow a systematic, logical, trouble shooting procedure.

4-2. LOGICAL TROUBLE SHOOTING.

The following paragraphs describe a general trouble shooting technique based on six logical trouble shooting steps. If adequate field data of equipment faults is not available, a trouble shooting procedure similar to these steps should be used.

a. SYMPTOM RECOGNITION. - This is the first step in the logical trouble shooting procedure and requires a complete familiarity with the equipment operating characteristics. Many equipment troubles are not a direct result of component failure and are only apparent as a condition of less than peak performance. This type of trouble is usually discovered during the preventive maintenance checks contained in the Maintenance Standards section, Section 5, Maintenance. It is important to recognize performance deterioration as well as more apparent troubles. Obvious trouble symptoms such as poor sensitivity or selectivity, low output levels, or complete equipment breakdown are more readily observed.

b. SYMPTOM INVESTIGATION. - When a trouble symptom has been recognized, the situation should be investigated to elaborate the symptom and further identify the trouble. Equipment controls can be adjusted and panel meter readings noted in an attempt to identify the symptom with a particular equipment function or mode of operation. For example, if receiver operation is subnormal on one mode of operation and normal when using other modes, the trouble can be associated with that section of the receiver employed for the subnormal mode.

c. PROBABLE FAULTY SECTION. - The next step in a logical trouble shooting procedure is to make a number of tentative decisions as to the most likely functional section at fault. These decisions should be based upon the trouble symptom, a knowledge of the equipment circuits, and be limited to those functional sections which, if defective, could probably cause the trouble. The over-all block diagram of the equipment (figure 4-1) and the functional block diagram (figure 4-2), together with the over-all functional description of the

receiver should be referred to when deciding the possible faulty circuit section or sections. For example, using the fault symptom described in the previous paragraph, a number of tentative decisions can be made.

(1) The trouble can be caused by a faulty mode switch contact.

(2) Tuning, injection, and power supply circuits are not at fault because other modes provide normal operation.

(3) The trouble can be caused by a faulty functional circuit for use by the defective mode only.

d. LOCALIZING THE FAULTY SECTION. - To effectively localize the trouble and determine the faulty circuit section, test should be made in an order which will require the least testing time. The test sequence should be based on the validity of the tentative decisions and the difficulty in making the test. If the first functional section is not at fault, the next section must be tested, and so on, until the faulty section is located. Refer to the functional descriptions, service block diagrams, and test data for the particular section being tested. Perform tests and checks which will either eliminate or pinpoint the functional section under consideration. For example, using the previously discussed fault symptom, the following test sequence and procedures could be employed:

(1) Examine the mode switch contacts and check the circuit in question using an ohmmeter.

(2) If the cw mode is at fault, check the bfo circuit section.

(3) If the ssb mode is at fault, check for the presence of a carrier injection frequency at the demodulator circuit.

e. ISOLATING THE FAULTY COMPONENT. - After the faulty functional section or stage has been identified, the trouble should be pinpointed to the part or parts at fault. The service block diagram, simplified schematic diagram, part location illustrations, and test point data for the faulty section should be used. For example, using the previously discussed fault symptom, the following procedure could be followed to isolate the faulty component.

(1) Continuity at the suspected mode switch contacts can be established by circuit testing.

(2) If the cw mode is at fault, bfo output frequency and level can be measured at a suitable test point.

(3) If the ssb mode is at fault, the carrier injection frequency and level can be measured at a suitable test point.

f. FAULT ANALYSIS. - When the faulty component has been isolated by circuit continuity and voltage measurements, but before repairs are made, review the initial tentative decisions and the trouble shooting procedure employed in an attempt to establish the reason for component failure. Make sure that the defective part is the actual cause of trouble and not just the result of an undiscovered malfunction, perhaps in another associated circuit. For an example, a short-circuited

capacitor in a power supply decoupling circuit can cause a decoupling resistor, located in another circuit section, to overheat and burn out. A proper fault analysis would consider the following steps leading to the discovery of the short-circuited capacitor. Otherwise, replacement of the burned out resistor would not have solved the problem.

(1) The overheated resistor must have been subjected to an abnormally high current to cause it to overheat and burn out.

(2) Current of this magnitude would flow only if a short-circuit to ground occurred at the load end, not the power source end, of the resistor.

(3) A resistance measurement between the resistor load terminal and ground would verify this fault analysis. Other circuit tests and circuit tracing would locate the faulty capacitor causing resistor failure.

g. USE OF CARD EXTENSION. - An extender to permit tests and adjustments to be made on the synthesizer (A1A3A1) plug-in printed circuit cards, while actively a part of the receiver, is required for the use of the technician. To install the card extension, perform the following:

- (1) Remove primary power from the receiver.
- (2) Remove the card to be tested or adjusted, using the card puller.
- (3) Insert the card extension into the compartment in place of the card.
- (4) Insert the card into the extension socket.

CAUTION

Always de-energize the receiver before removing or replacing cards or modules. Otherwise, the making or breaking of live circuits will damage the connection terminals and can damage components.

To remove the card extension, remove primary power from the receiver and perform steps (2) through (4) described above in a reverse order.

4-3. OVER-ALL FUNCTIONAL DESCRIPTION.

a. GENERAL. - Radio Receiver R-1490/GRR-17, a dual conversion super-heterodyne, operates in the frequency range from 2.0 to 30.0 mc without the usual bandswitching. The all solid-state receiver is tuned, in increments of 100 cycles, over its frequency range by setting five digital tuning dials to the signal frequency. Continuous tuning is available to tune the receiver 150 cycles above or below the selected 100-cycle increment.

The receiver has output connections for a headset or other external terminal equipment and for the connection of teletype equipment. The following reception modes are provided:

- (1) CW - Continuous-wave telegraphy (A1).
- (2) FSK - Two-tone frequency-shift teletype (F1).
- (3) SSB - Upper or lower single-sideband (A3j).
- (4) AM - Amplitude modulation (A3).

All injection frequencies to the signal path mixing stages are developed by the synthesizer section of the receiver which is controlled by the five digital tuning dials. Synthesized frequencies exhibit the same stability and accuracy as the 3 mc frequency standard employed, one part in 10^7 per day. The internal power supply contains individual circuits to supply +125, +24, +18, +15, and +5 volts dc to the receiver circuits, and will operate from a 115 volt ac, 50-400 cps, power source, or a 24 volt dc power source.

b. BASIC BLOCK DIAGRAM. - Figure 4-1 is a basic block diagram of the receiver with the main signal path indicated by a heavy line. It shows the relation between the main signal path circuits and the synthesizer circuits, and the location of these circuits on the front panel, front deck, and rear deck sections. Note that the signal path input circuit is unconventional. No continuously tuned preselector stages are employed preceding the first mixer. In fact, no mechanical tuning of the receiver is required or necessary. The first frequency injection to the up-converter stage (p/o A1A2A2) is supplied, in precise increments of 100 cycles, by the synthesizer circuits in response to the MEGACYCLES dials setting.

An rf signal at the antenna is passed through the antenna trimming circuit (A1A1A6) to one of the filter sections of the input filter module (A1A2A1), converted to 112 mc at the up-converter stage (p/o A1A2A2), passed through the 112 mc roofing filter FL1 (p/o A1A2), and amplified by a portion of the first i-f module (A1A2A3). Following a second conversion to 5 mc in the first i-f module, the signal is passed through the noise blanker module (A1A2A4), the remaining portion of the first i-f module (A1A2A3), the intelligence filter module (A1A2A5), and the notch filter module (A1A1A4) for amplification by the second i-f/agc amplifier module (A1A2A6). The signal is then detected and amplified by the detector/af amplifier module (A1A2A7), and applied to the loudspeaker and headset circuits or to the teletype output circuit, depending upon the mode of reception employed.

The first injection frequency from 82 to 110 mc is generated by the vhf oscillator stage (p/o A1A2A2) in precise 100-cycle increments. When the MEGACYCLES dials are set to the signal frequency the second injection frequency of 117 mc, subject to a ± 150 cycle adjustment when continuous tuning is used, is supplied by the synthesizer circuit to obtain conversion from 112 mc to a 5 mc i-f frequency. A third injection frequency of 5 mc, via the bfo module (A1A1A3), is applied from the synthesizer to the ssb demodulator stage in the detector/af amplifier module (A1A2A7) when the cw, fsk, or ssb reception modes are used. The bfo module functions as an amplifier circuit to supply a fixed 5.0 mc injection frequency for the ssb reception mode, but operates as a variable frequency (5.0 mc ± 3 kc) oscillator as well for the cw and fsk modes.

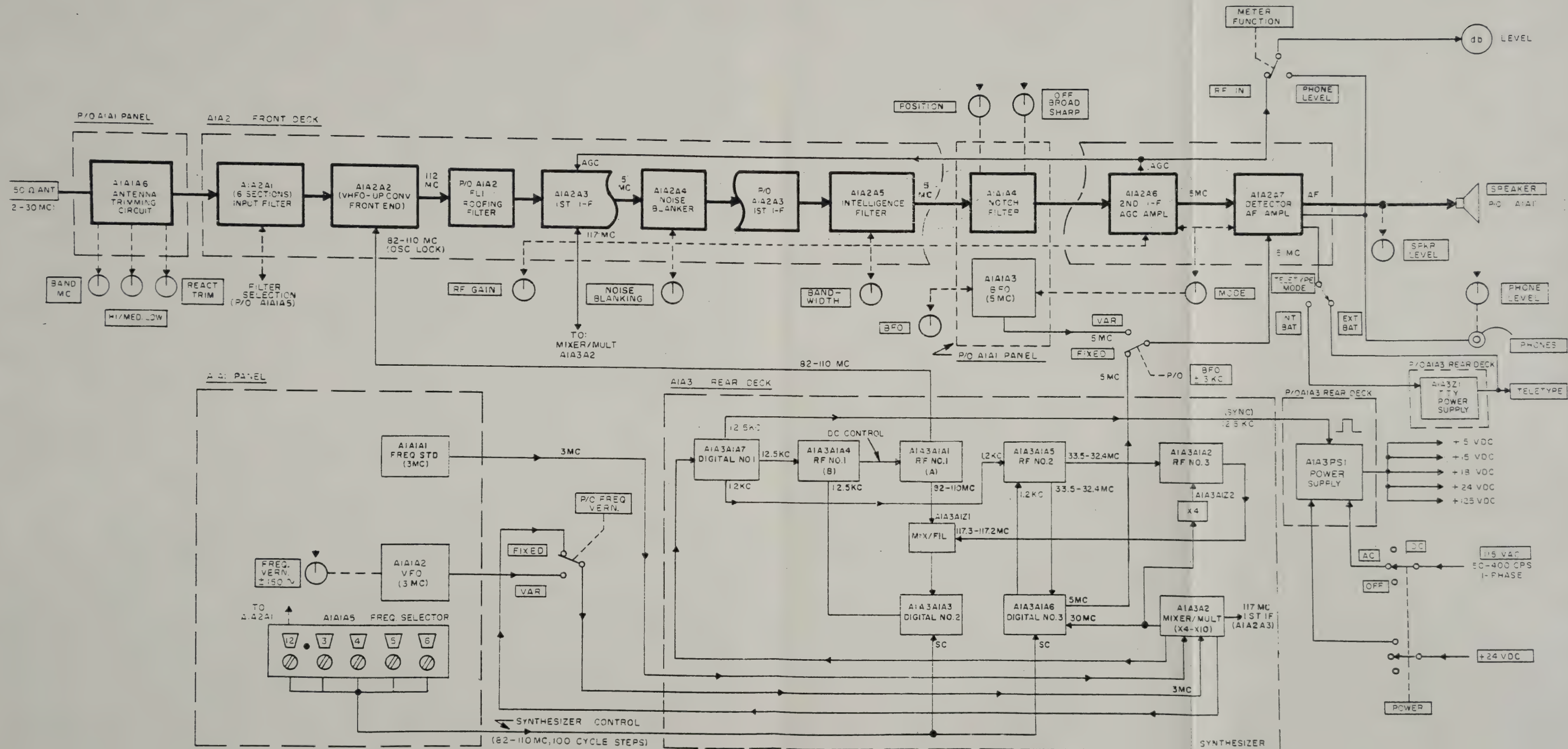


Figure 4-1. Radio Receiver R-1490/GRR-17,
Basic Block Diagram

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The synthesizer circuits are all solid state and employ digital frequency techniques using phase-locked voltage controlled oscillators and a 3 mc crystal-controlled frequency standard to develop literally thousands of synthesized frequencies, each with the same accuracy and stability as the frequency standard. A phase-locking circuit in the front-end module (A1A2A2) corrects the voltage controlled vhf oscillator output frequency over its 82 to 110 mc range. Two of the regulators (+5 v, +18 v) in the power supply module (A1A3PS1) employ solid-state switching circuits timed by a 12.5 kc pulse from the synthesizer. The remaining regulator (+15 v) is a conventional series-control type. The +125 volt supply is unregulated.

c. FUNCTIONAL BLOCK DIAGRAM. - Figure 4-2 is a detailed functional block diagram of the receiver. The main signal path is indicated by a heavy line and arrow heads are affixed to secondary signal paths of importance to show the functional direction of signal flow. The following paragraphs present a detailed description of the major circuit modules and their function in relation to the overall receiver function.

(1) SIGNAL PATH. - Signals at the antenna go through the antenna trimming circuit (A1A1A6) and are applied to the front-end module (A1A2A2) through one of six filters contained in the input filter module (A1A2A1). The appropriate filter is selected when the first (mc) dial of the MEGACYCLES selector (A1A1A5) is set to a signal frequency. For example, if the MEGACYCLES dials are set at 02.0000 mc, filter FL2 (2.0 to 3.0 mc) is used. Consequently, a group of frequencies from 2.0 to 3.0 mc is applied to the up-converter in the front-end module. The vhf oscillator frequency is also selected when the MEGACYCLES dials are set. For the example above, the vhf oscillator supplies a 110 mc injection frequency to the up-converter. The 112 mc sum frequency at the up-converter output is passed through roofing filter A1A2FL1; other sum frequencies outside the filter bandpass are rejected.

From the roofing filter, the signal is amplified by a 112 mc i-f amplifier in the first i-f module (A1A2A3), passed through a second filter (FL1), further amplified, and applied to second conversion mixer Z1. The 117 mc second frequency-injection from the mixer/multiplier module (A1A3A2) is amplified by the 117 mc buffer amplifier and combined with the 112 mc signal to produce a 5 mc difference frequency which goes to the noise blanking module (A1A2A4). Output from the noise blanker, via filter FL2, is amplified by the 5 mc amplifier in the first i-f module.

The 5 mc i-f signal then goes to the intelligence filter module (A1A2A5) which contains four bandpass filters, each having characteristics corresponding to the operating mode selected by the MODE switch. The 5 mc signal then passes through the notch filter module (A1A1A4) to the second i-f/agc amplifier module (A1A2A6) for additional amplification.

The signal now is applied to the detector/af amplifier module (A1A2A7). This module contains the am and ssb detector circuits and the fsk converter circuit, and their related af amplifiers. For the am and ssb modes of reception, following detection the af signal is amplified by the individual speaker and headset amplifiers. For the fsk mode of reception, digital logic circuits convert the two-tone teletype signal to a mark-and-space keying function available at the TELETYPE output terminals in the teletype external battery mode; in the internal battery mode the keying function is used to turn the TTY power supply (A1A3Z1) on

and off. The keying potential developed is now available at the TELETYPE output terminals.

(2) FIRST FREQUENCY-INJECTION. - The receiver first frequency injection is generated by the vhf phase-locked oscillator in the front-end module (A1A2A2). The injection frequency, ranging from 82 to 110 mc to cover the receiver tuning range, is phase locked in increments of 100 cycles by a precise corresponding frequency from the synthesizer section. In the previous example, the MEGACYCLES dials were set for a 02.0000 signal frequency. This dial setting automatically applies a 110.0000 mc synthesized frequency to the phase-locked loop circuit (p/o front-end module A1A2A2). Phase detector CR1-CR2 compares the two frequencies and develops a dc control voltage to correct the varactor tuned vhf oscillator to assure a precise 110.0000 mc first injection frequency.

(3) SECOND FREQUENCY-INJECTION. - The 117 mc second injection frequency is supplied from the mixer/multiplier module (A1A3A2). For incremental receiver tuning, the mixer/multiplier module (A1A3A2) derives this frequency from the 3-mc frequency standard module (A1A1A1). When the receiver is continuously tuned, the 3 mc injection frequency is derived from the vfo module (A1A1A3). Consequently, the 117 mc frequency can be varied ± 150 cycles by tuning the vfo to provide continuous tuning of any 100 cycle increment set at the MEGACYCLES dials. The 117 mc signal is amplified by a 117 mc buffer amplifier (p/o A1A2A3) before being applied to the 2nd conversion mixer Z1.

(4) CARRIER INJECTION. - A third frequency injection at the signal path is a 5 mc frequency, supplied by the synthesizer section, which is applied to ssb demodulator Z1 in the detector/af amplifier module (A1A2A7) for the detection of ssb signals. This process is also known as carrier injection or reinsertion. Demodulator Z1 is also used for cw mode reception. For this mode, the bfo module (A1A1A2) provides a variable 5 mc frequency in place of the fixed 5 mc injection frequency to provide adjustable sidetone signals.

(5) SYNTHESIZER. - The all solid-state synthesizer circuits use digital circuit techniques to supply precise injection frequencies to the receiver signal path. Because all synthesized frequencies are derived from a 3 mc frequency standard, they exhibit the same degree of frequency accuracy and stability as the source. In addition to frequency mixing, dividing, and multiplying circuits, the synthesizer uses several voltage controlled oscillators (vco), arranged in a phase-locked loop. The loop circuit compares the vco output frequency with a reference frequency based on the frequency standard, and corrects the oscillator frequency. A digital-type pulse counter in the feedback loop, programmed by the MEGACYCLES dials settings, functions as a precise variable-frequency divider and permits a large number of synthesized vco frequencies to be developed with precision using only one reference frequency per vco.

The first injection frequency from 82 to 110 mc is supplied directly from the vco circuits in the rf #1(A) card (A1A3A1A1). The feedback loop containing the pulse counter ($\div N$) is located in the digital #2 card (A1A3A1A3). The rf #1(B) card (A1A3A1A4) contains the ramp generator, phase detector, and discriminator circuits for tuning the particular vco in use, correcting its frequency, and comparing the output frequency with a 12.5 kc reference frequency. The mc and 100 kc dials on the MEGACYCLES selector (A1A1A5) program the pulse counter ($\div N$) and control the development of a first injection frequency in 100 kc increments only. A detailed description of circuit operation is provided later in this section.

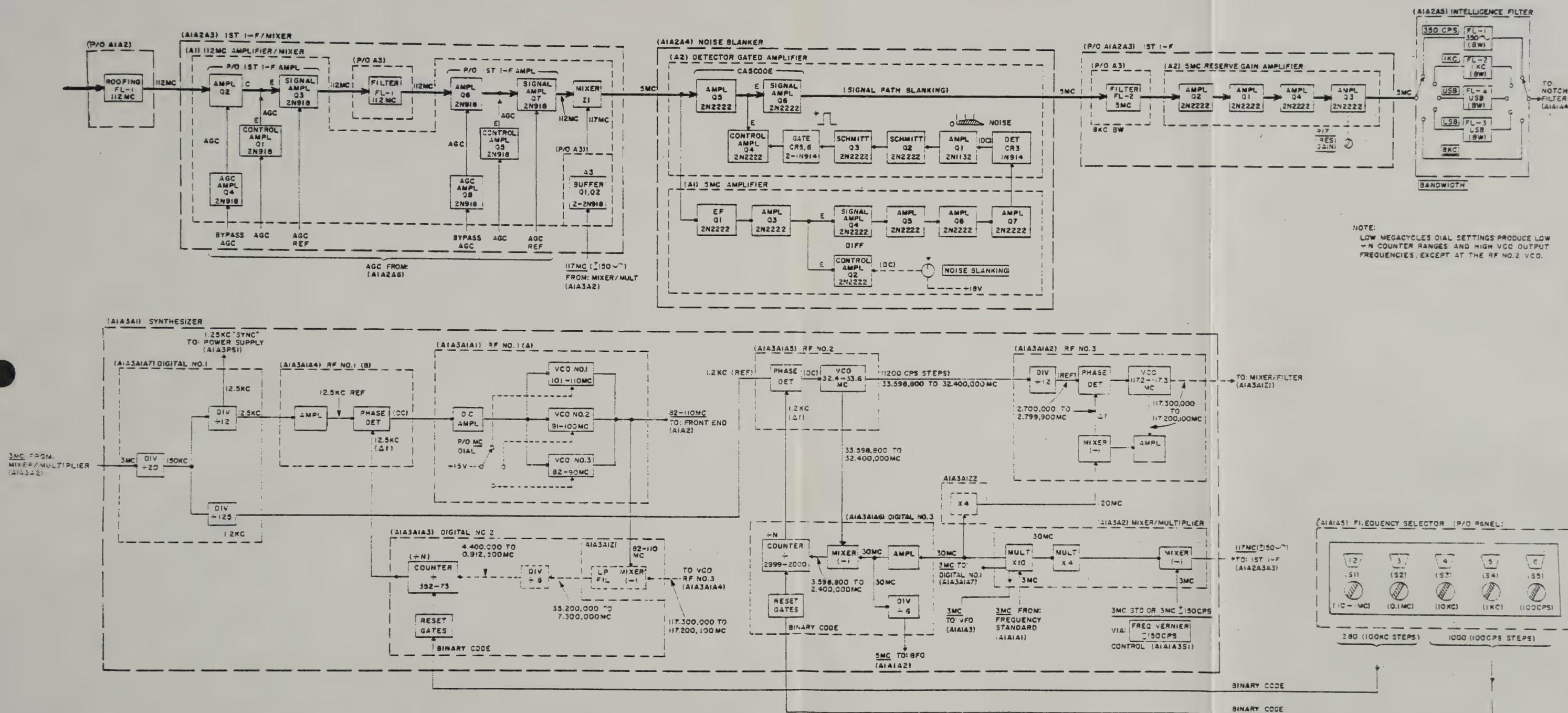
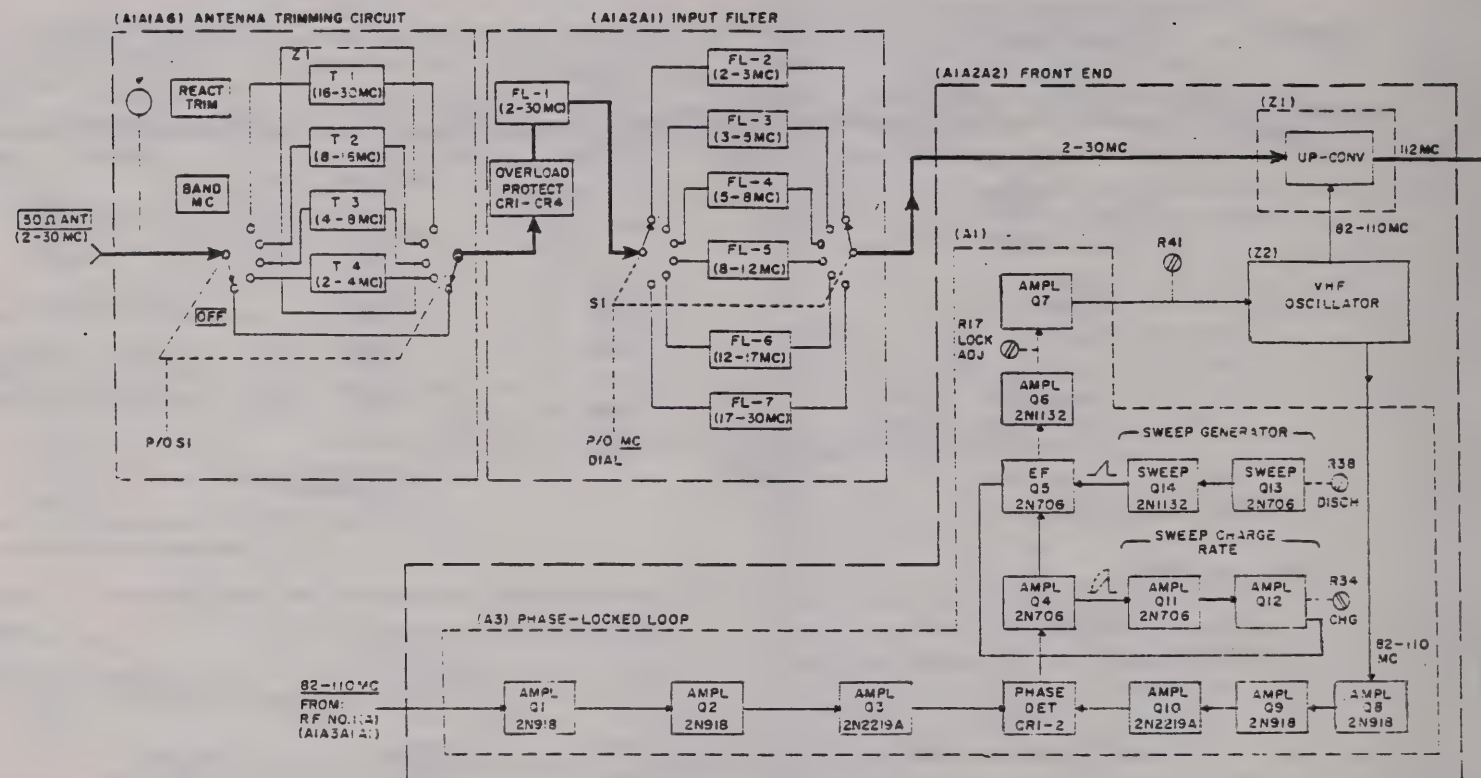
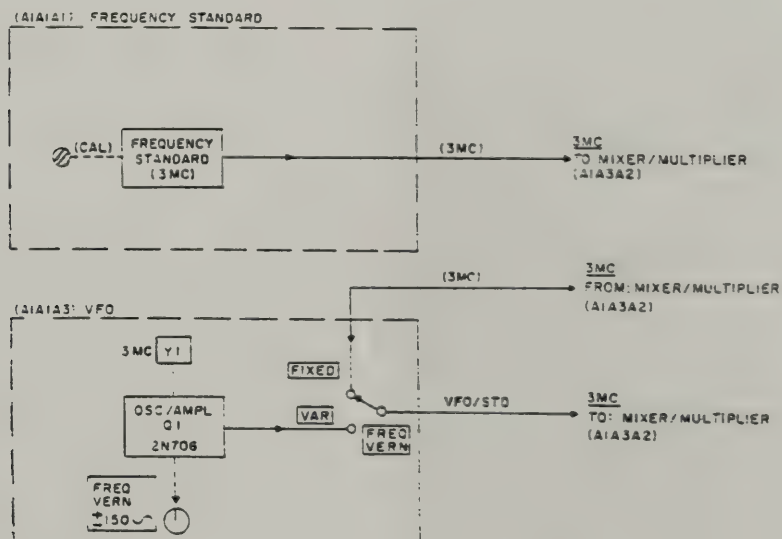
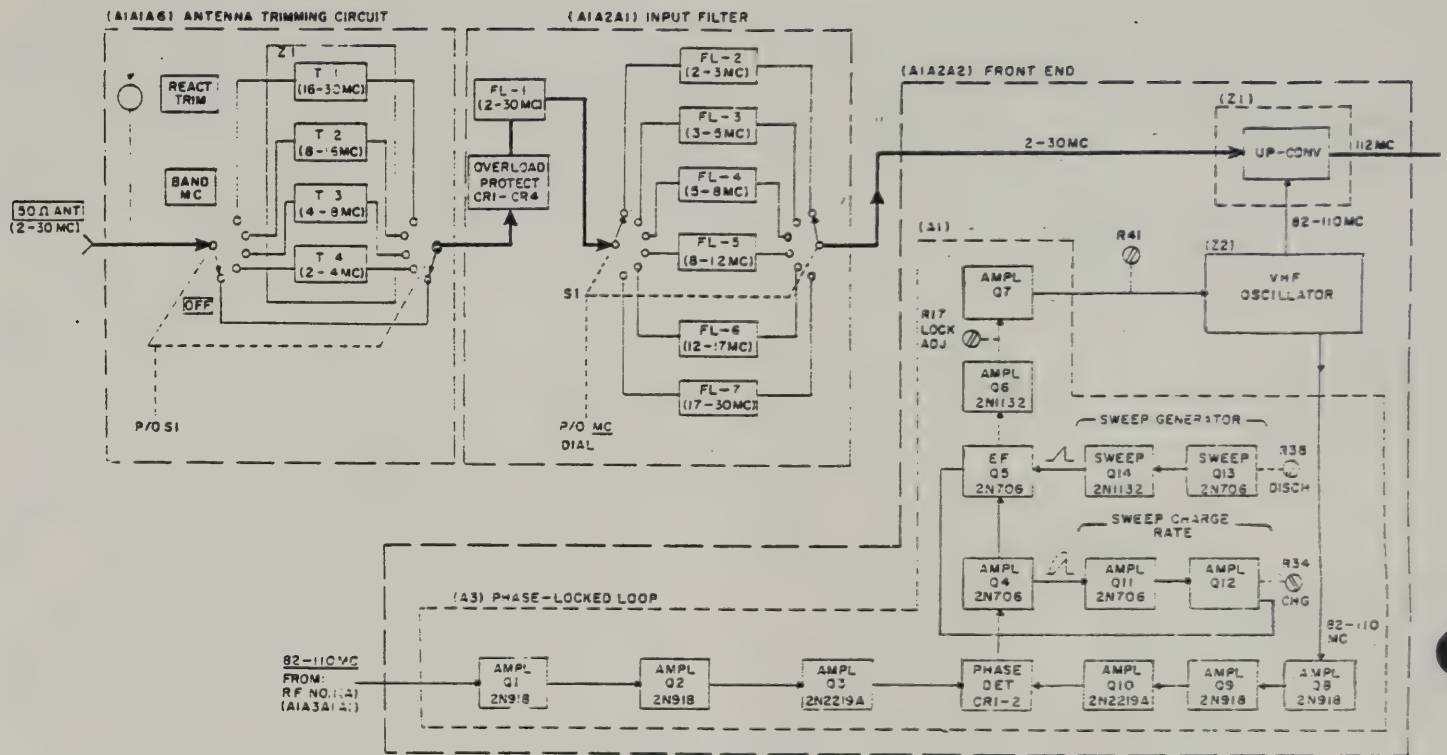


Figure 4-2. Radio Receiver R-1490/GRR-17,
Functional Block Diagram (Sheet 1 of 2)





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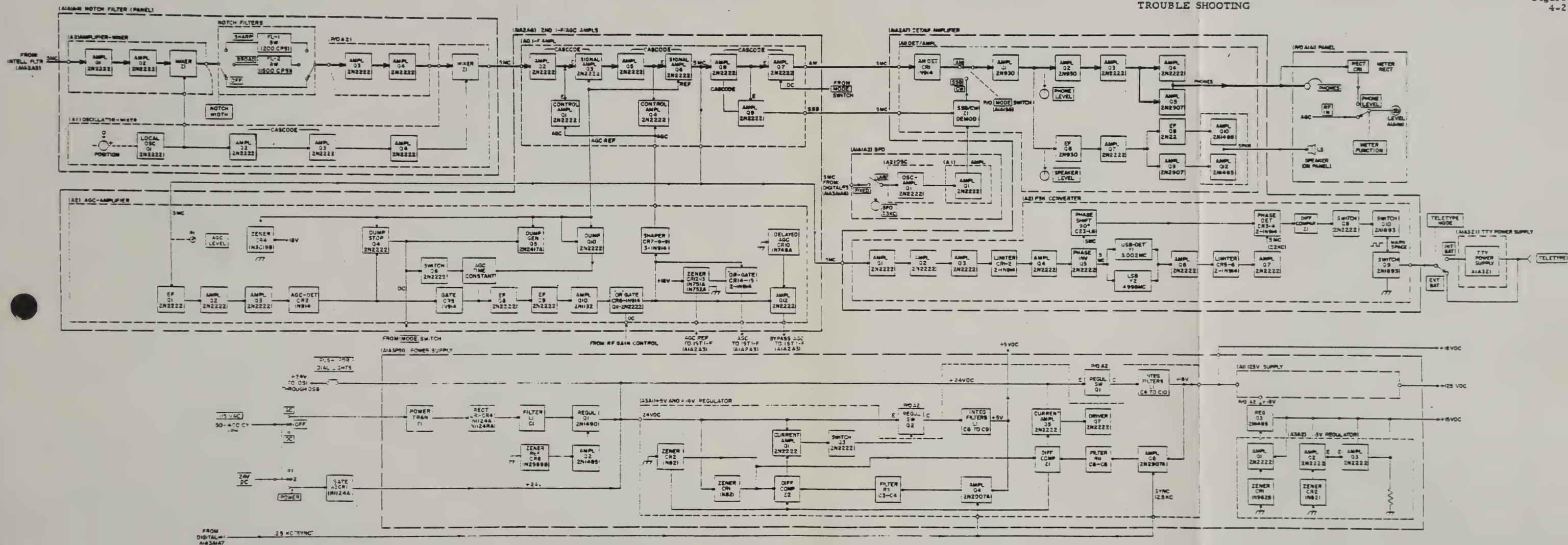


Figure 4-2. Radio Receiver R-1490/GRR-17,
Functional Block Diagram (Sheet 2 of 2)

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To obtain synthesization of the 82 to 110 mc first injection frequency in additional increments of 10 kc, 1 kc, and 100 cycles, a second vco and phase-locked loop circuit is used. The rf #2 card (A1A3A1A5) contains the vco circuit with a ramp generator, phase detector, and discriminator to tune the vco over a frequency range of approximately 32 to 34 mc, correct its frequency, and compare the loop output with a 1.2 kc reference frequency. The feedback loop with its pulse counter ($\div N$) is contained in the digital #3 card (A1A3A1A6). The 10 kc, 1 kc, and 100 cycle dials on the MEGACYCLES selector program the pulse counter ($\div N$) to control the vco and produce incremental frequencies which are processed at the rf #3 card (A1A3A1A2) and combined with the initial 82 to 110 mc frequencies at mixer Z1 in the digital #2 card (A1A3A1A3) to drive the first pulse counter ($\div N$).

In this manner, the three vco circuits in the rf #1(A) card (A1A3A1A1) can be programmed to supply 280,000 discrete injection frequencies, 100 cycles apart, over a frequency range from 82 to 110 mc corresponding to a signal frequency range from 29.9999 to 2.0 mc, respectively. For continuous tuning of any 100 cycle increment, the vfo module (A1A1A3) supplies a 3 mc frequency which can be tuned ± 150 cycles using the FREQ VERNIER ± 150 CPS control. This module replaces the 3 mc frequency standard at the mixer/multiplier module (A1A3A2) for the production of the 117 mc second frequency injection, only. It is not used for the production of other frequencies. A detailed circuit description is supplied later.

The mixer/multiplier module (A1A3A2), in addition to supplying the 117 mc second injection frequency, also supplies a 30 mc standard frequency to the digital #3 card (A1A3A1A6) and to the X4 multiplier (A1A3A1Z2) for the production of the synthesized tuning frequencies. The 3 mc standard frequency is amplified by a section of the mixer/multiplier circuit prior to application at the digital #1(A) card (A1A3A1A7A1).

(6) FREQUENCY STANDARD. - The crystal-oscillator frequency standard module (A1A1A1) supplies a precise 3 mc standard frequency to the digital #1(A) card (A1A3A1A7A1) via the mixer/multiplier module (A1A3A2). Although an oven is not used to maintain crystal temperature, its accuracy and stability is one part in 10^7 per day and 5 parts in 10^7 for 30 days. The module contains an adjustment to permit calibration using a primary frequency standard.

(7) POWER SUPPLY. - The receiver power supply module (A1A3PS1) contains individual circuits to supply +5, +15, +18, and +125 volts dc to the receiver. For operation from a 115 volt ac power source, the supply has a conventional power transformer, rectifier, filter, and a 24 volt dc regulator circuit. The individual regulators operate from this 24 volt dc source. For operation from a 24 volt dc power source, the power transformer and 24 volt regulator circuit are bypassed. The +5 volt and +18 volt regulating circuits use a solid state switching circuit which is synchronized by a 12.5 kc pulse supplied by the digital #1(B) circuit (A1A3A1A7A2). In addition, the TTY power supply (A1A3Z1) provides a 120 volt, 60 ma loop potential for external teletype equipment.

(8) MEGACYCLES FREQUENCY SELECTOR. - The MEGACYCLES frequency selector (A1A1A5) contains the five selector switches for tuning the receiver, in increments of 100 cycles, from 2.0000 to 29.9999 mc. Illuminated windows above each selector dial register the signal frequency, from left to right, in a decade step sequence of mc, 100 kc, 10 kc, 1 kc, and 100 cycles. Each dial registers numerals from 0 to 9 except the mc dial which reads from 02 to 29, only.

These selector dials control switches which program the two digital pulse counters in the synthesizer section. In addition to this function, the mc dial, selects the appropriate bandpass filter at the input filter module (A1A2A1), and also selects the particular voltage controlled oscillator (vco) in the rf #1(A) card (A1A3A1A1) to be used. Because no mechanical tuning or bandswitching components are employed in the receiver, the desired signal is received immediately following tuning using the five MEGACYCLES dials.

4-4. MODULE CIRCUIT DESCRIPTION AND TROUBLE SHOOTING.

The following paragraphs describe the operation of each module in the receiver and the function of each circuit employed. Trouble shooting information and test data is provided to assist the maintenance technician in diagnosing the malfunction and quickly and efficiently locating the cause of trouble.

a. CIRCUIT DESCRIPTION. - Simplified schematic diagrams of each module circuit, or functional circuit within the module, are provided to identify the major circuit elements and supplement the circuit descriptions. Servicing block diagrams of each module showing the circuit and stage arrangements are used as a pictorial guide for trouble shooting. Wherever possible, simplified schematic diagrams are located adjacent to the circuit discussion in the text for quick reference. The servicing block diagrams are located at the end of this manual section. Refer to Section 5, Maintenance, for module removal and replacement data.

b. TROUBLE SHOOTING. - Unless otherwise instructed, trouble shooting procedures are performed with the receiver energized. All module test points equipped with a test jack are exposed when the receiver transit case and dust cover are removed and the rear deck section separated from the receiver. Both the front panel and rear deck sections can be separated from the front deck section; the connecting cables allow circuit tests to be made with the receiver energized. Refer to Section 5 for illustrations showing the location of each receiver component, and for the module schematic diagram and interconnecting diagrams. The following trouble shooting information is supplied for each module in the receiver.

(1) PRELIMINARY CHECK. - This paragraph describes initial checks to be made before trouble shooting the module circuit.

(2) TEST EQUIPMENT. - Required test equipment and special tools for trouble shooting a receiver module are contained in this paragraph.

(3) CONTROL SETTINGS. - Panel control functions are given in table 3-2, Section 3, together with the initial control settings. This paragraph describes control settings to be made for a particular test.

(4) TEST DATA. - This paragraph contains test information and data to aid in locating a faulty module circuit or component.

c. REFERENCES. - Refer to the Handbook for Electronic Circuits (NAV-SHIPS 900,000.102) for a description of conventional electronic circuits used in similar receivers.

4-5. INPUT FILTER A1A2A1. (See figure 4-3.)

The input filter, in series with the receiver antenna circuit, consists of a 3 db attenuator (T-pad), a diode signal-limiting circuit, a broad-band filter, and

six bandpass filters selected by the mc dial of the MEGACYCLES selector (A1A1A5). Faulty operation of the input filter module can affect a particular segment of the total frequency range (a segment covered by one of the six selectable filters) or prevent reception completely.

a. DESCRIPTION. - The T-pad attenuator consisting of resistors R1 thru R3 provides a stable terminating impedance for the filters. The overload protection circuit, diodes CR1, CR3, and Zener diodes CR2, CR4, will conduct extremely large signals to ground, protecting the receiver input circuit from damaging overloads. Broadband filter FL1 passes the receiver frequency range from 2.0 to 30.0 mc, rejecting all other frequencies, to improve the over-all noise factor. The individual filters FL2 thru FL7 are selected by the mc dial of MEGACYCLES selector for a particular segment of the receiver frequency range. Each filter provides a sharp bandpass characteristic, less than an octave wide, to reject spurious frequencies outside its bandpass and improve the receiver noise factor. C1 and L1 form a low-pass filter to improve rejection of vhf signals.

b. PRELIMINARY CHECK. (See figure 4-3.) - With power off, make a preliminary check of the input filter module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to the module.
- (3) Rotation of the filter selector switch when the mc MEGACYCLES dial is sequentially positioned from 02 to 29.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D and VTVM ME-286/U, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Preset all controls as indicated in table 3-2.

WARNING

Potentials as high as 125 volts are present in the power supply circuits. Avoid contact.

e. TEST DATA. (See figures 5-5 and 5-18.) - Trouble shooting the input filter module consists of applying a test signal from the signal generator to the module input and noting the signal level at the module output for each of the six input filters. The receiver need not be energized for this test. Perform the following:

- (1) Connect signal generator to the 50 Ω ANT connector (A1A1J1) and adjust generator for a 100 millivolt, 2.5 mc, unmodulated test signal. Connect the rf VTVM to pin C of XA2 after removing the front end module (A1A2A2).
- (2) Set the mc dial of the MEGACYCLES selector to read 02; the remaining dial positions are not important. Note the VTVM reading. The over-all insertion loss of the input filter module should be less than 5 db, or a voltage loss ratio of two.
- (3) Repeat steps (1) and (2) using the test frequencies and mc dial settings in the following list.

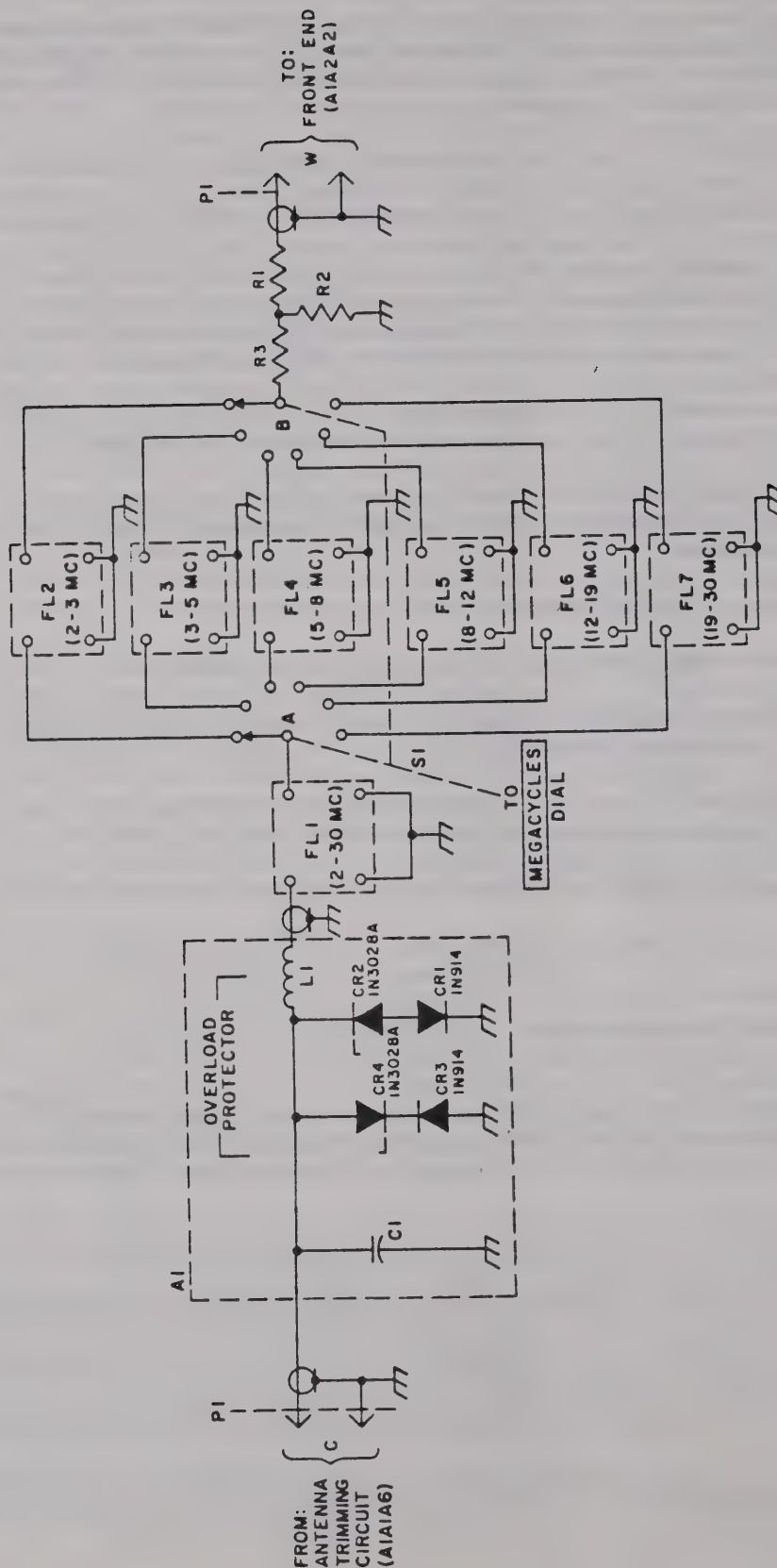


Figure 4-3. Input Filter A1A2A1, Simplified Schematic Diagram

<u>Test Signal</u>	<u>MC Dial</u>
4.0 mc	04.
6.5 mc	06.
10.0 mc	10.
15.5 mc	15.
24.5 mc	24.

Note

Setting the mc dial to the readings listed selects the bandpass filter to be tested. The test signal frequency is at the center of the filter bandpass.

4-6. FRONT END A1A2A2. (See figures 4-4 and 4-5.)

The front-end module contains the vhf oscillator circuit (Z2), the up-converter circuit (Z1), and the phase-locked loop circuit (A1). Faulty operation of the front-end module can affect the receiver frequency calibration or prevent reception completely.

a. DESCRIPTION. - The receiver first frequency-conversion is performed at the front-end module. An 82 to 110 mc first injection frequency, generated by the vhf oscillator (Z2), is combined with rf signals from the input filter module (A1A2A1) to obtain the 112 mc first intermediate frequency. Mixing is performed by the up-converter (Z1) circuit. The vhf oscillator output frequency is "locked" to an "absolute" frequency supplied by the synthesizer (A1A3A1) circuits by the phase-locked loop circuit (A1). Consequently, the vhf oscillator frequency has the same frequency accuracy and stability as the 3 mc frequency standard (A1A1A1).

(1) VHF OSCILLATOR (Z2). (See figure 4-4.) - The vhf oscillator is tuned from 82 to 110 mc by a dc varactor control voltage supplied from the phase-locked loop circuit (A1). The oscillator is a sealed nonrepairable unit.

A sample of the oscillator output frequency is supplied to the phase-locked loop circuit (A1). Oscillator output is 1 watt with a 50 ohm load.

(2) UP-CONVERTER (Z1). (See figure 4-4.) - The up-converter-mixer circuit consists of the sealed sub-module (Z1). An 82 to 110 mc first injection-frequency, supplied in increments of 100 cycles by the vhf oscillator circuit (Z2), is combined with the received 2.0 to 30.0 mc received signal frequency to obtain frequency up-conversion. The 112 mc sum frequency is applied to the roofing filter A1A2FL1. Primarily, the high dynamic range of the receiver is contributed by the up-converter circuit operation. Signal linearity is retained even in the presence of strong signals. The up-converter is a sealed nonrepairable unit.

(3) PHASE-LOCKED LOOP (A1). (See figure 4-5.) - The phase-locked loop circuit consists of separate buffer amplifiers for the synthesizer and vhf oscillator input signals, a phase detector, a direct-coupled dc amplifier, and a sweep generator and ramp rate circuit. The dc varactor-control voltage derived by this

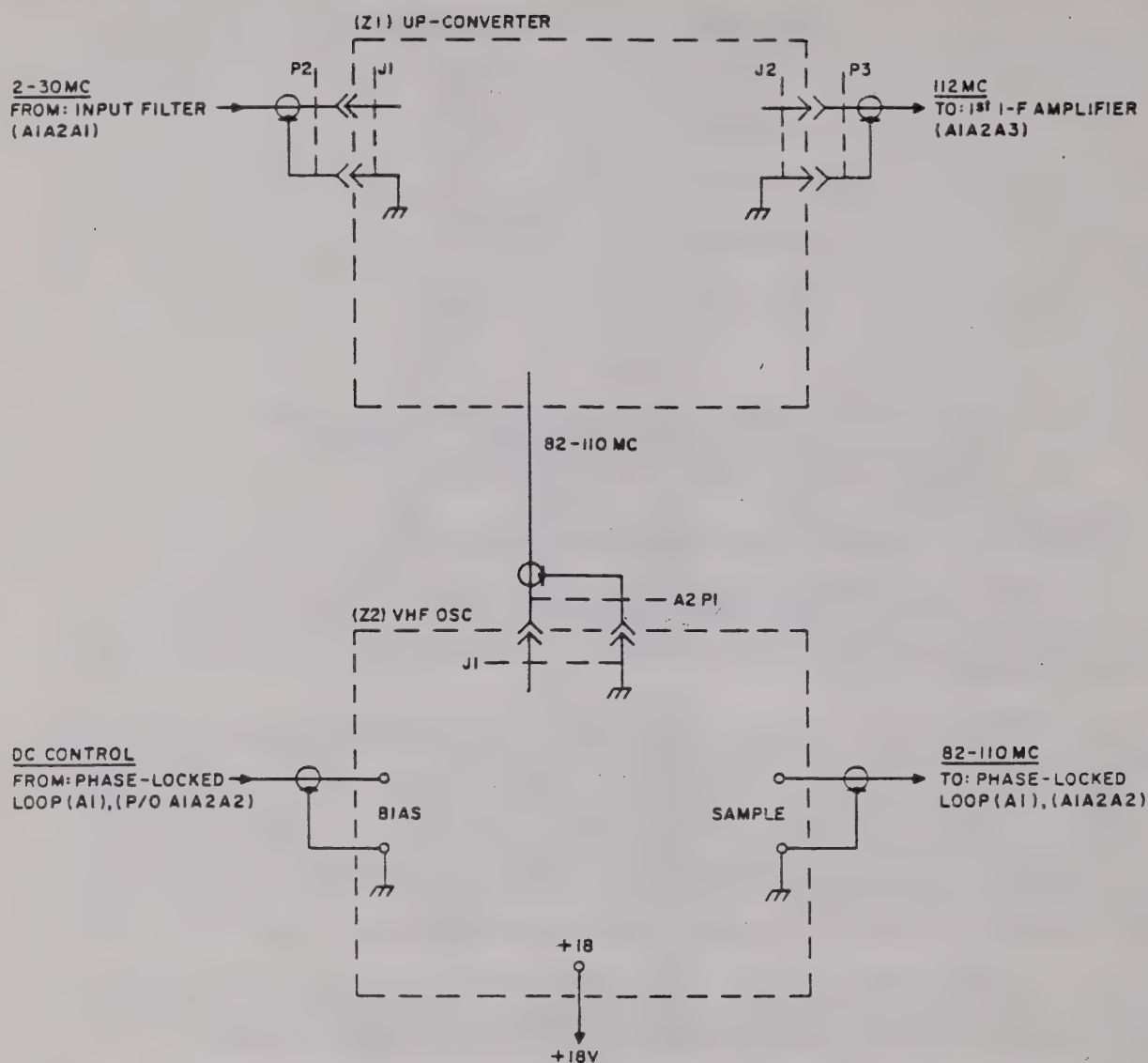


Figure 4-4. Front-End AlA2A2; VHF Oscillator (Z2) and Up-Converter (Z1),
Simplified Block Diagram

circuit is applied to the vhf oscillator (Z2) to select and lock the oscillator frequency.

(a) BUFFER AMPLIFIERS. - The buffer amplifier for the synthesizer 82 to 110 mc input signal consists of a cascode circuit using Q1 and Q2, and the amplifier Q3. Amplifier output is applied to the phase detector through network Z1. The vhf oscillator input-signal buffer amplifier employs a similar circuit using cascode amplifiers Q8 and Q9, and amplifier Q10. The two buffer amplifiers raise the input signal levels in order to obtain sufficient output from the phase detector.

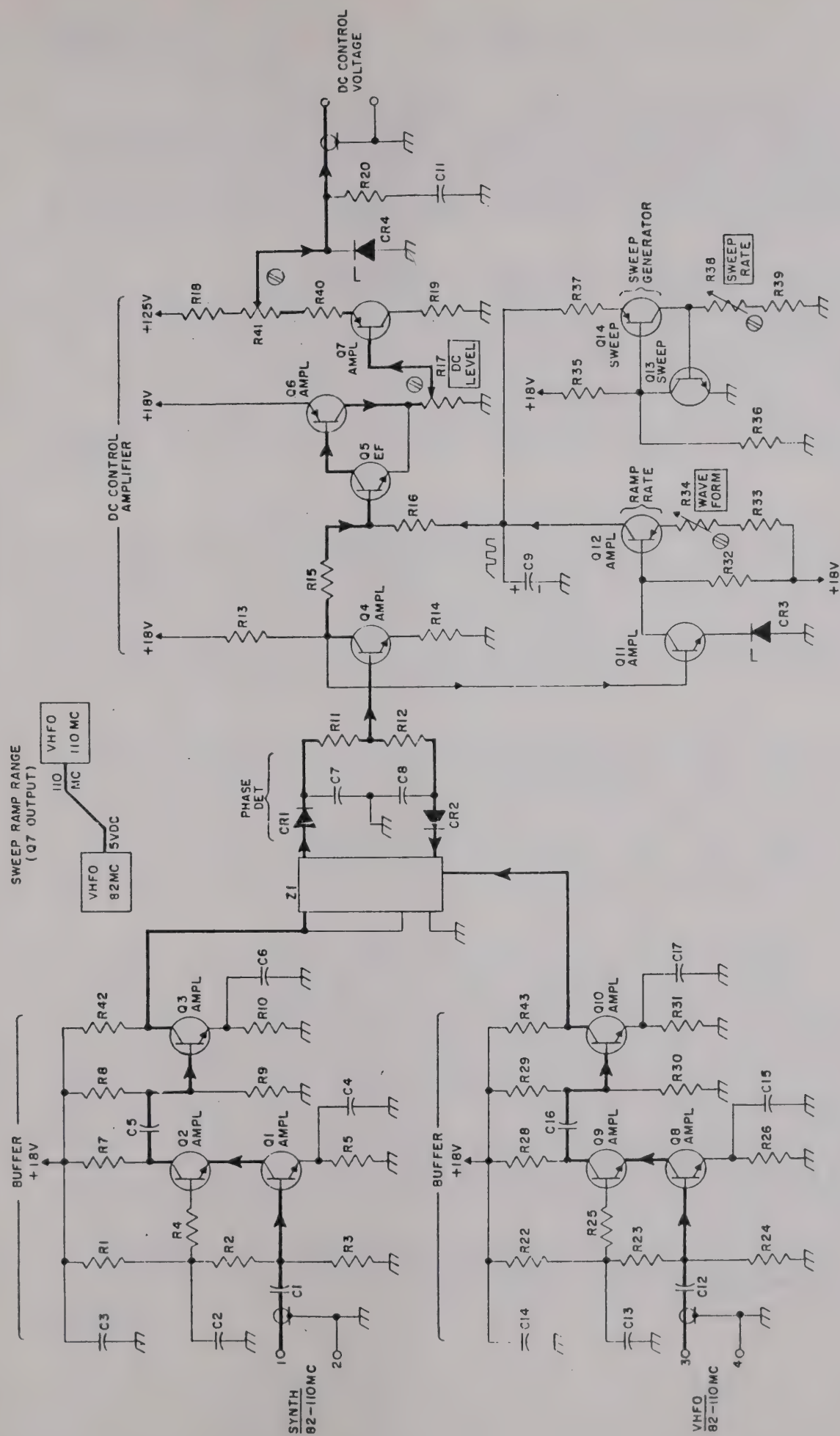


Figure 4-5. Front End A1A2A2; Phase-Locked Loop (A1), Simplified Schematic Diagram

(b) PHASE DETECTOR. - Network Z1 provides for the efficient transfer of signals from the two buffer amplifiers to the phase detector CR1, CR2. The phase detector compares the vhf oscillator and synthesizer frequencies, producing a dc voltage directly proportional to the phase (and frequency) difference between them. When a large frequency difference exists, the phase detector output becomes modulated with this "beat" frequency. The output is amplified by the dc amplifier circuit which follows.

(c) DC AMPLIFIER. - Phase detector output is amplified by a direct-coupled amplifier consisting of Q4 thru Q7. Stages Q5 and Q6 are arranged in a Darlington circuit for a maximum current gain. Output amplifier Q7 supplies a dc output voltage ranging from 5 volts to 110 volts, depending upon the signal level at the phase detector output. This dc control voltage, applied to the vhf oscillator (p/o A1), controls the oscillator frequency from 82 to 110 mc. Adjustment R17 sets the maximum dc level from Q7 at 110 volts dc, corresponding to a vhf oscillator output frequency of 110 mc. Zener diode CR4 limits the level of dc applied to the vhf oscillator to a safe value. Adjustment R41 sets the lowest value of voltage.

(d) SWEEP GENERATOR AND RAMP RATE CONTROL. - To insure operation of the phase-locked loop circuit and the development of a dc control voltage, especially when a wide frequency difference exists between the two input signals, Q13 and Q14 function as a sawtooth sweep generator in conjunction with the RC time constant network formed by resistor R16 and capacitor C9. The circuit is the equivalent of a "unijunction" transistor sweep generator and adjustment R38 varies the sweep rate. The resultant dc ramp (saw-tooth) waveform generated is amplified by Q5 thru Q7 in the dc amplifier circuit and appears as a varactor control signal at the vhf oscillator (Z2).

To increase the ramp rise-time and therefore the speed of vhf oscillator response, Q11 and Q12 function as a ramp rate-control circuit. When the ramp voltage value exceeds a threshold set by Zener diode CR3 at the emitter of Q11, Q11 and Q12 conduct to charge capacitor C9 at a faster rate. As the vhf oscillator approaches the selected operating frequency, the Zener diode threshold voltage exceeds the dc control voltage and cut-off occurs at Q11. The ramp rise-time is decreased, slowing down the vhf oscillator response as a "null" condition is approached. Adjustment R34 varies the ramp waveform for optimum operation.

(e) LOOP OPERATION. - The dc control amplifier, Q4 thru Q7, has a frequency range extending to approximately 10 kc. Consequently, when a larger difference in frequency between the two input signal occurs the dc ramp generated by Q13 and Q14 starts the vhf oscillator sweeping. Continuous sweeping does not occur. Rather, the oscillator is swept from 82 mc upward until the frequency difference between the two input signals is less than 10 kc. When this occurs, a large dc signal appears at the phase detector output modulated by the "beat" frequency difference between the two signals. The vhf oscillator continues sweeping toward 110 mc until a loop "null" is approached, accompanied by a reduction in the phase detector output. The ramp rate circuit Q11 and Q12 is disabled, slowing the oscillator sweep rate as the two input frequencies become matched. During the "null", a small phase difference still exists between the input signals of a sufficient level to maintain the dc control voltage at that value to "lock" the oscillator.

Each time the synthesizer frequency to the loop circuit is changed by re-setting the MEGACYCLES dials on the receiver panel, a sweep ramp is generated

by the charging of capacitor C9. A dc control voltage of 5 volts at the output of Q7 corresponds to an oscillator frequency of 82 mc. As the dc control voltage is increased to a maximum of 110 volts, the oscillator frequency increases to 110 mc. If one of the two input signals is removed, the sweep ramp will reoccur, sweeping the vhf oscillator continuously from 82 to 110 mc at a rate of approximately three sweeps each second until the signal input is replaced.

b. PRELIMINARY CHECK. (See figure 4-51.) - With the power off, make a preliminary check of the front-end module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use Multimeter AN/USM-116, Signal Generator AN/URM-25D, VTVM ME-286/U, and Oscilloscope Tektronix 545A with head CA. No special tools are required.

d. CONTROL SETTINGS. - Preset all controls according to table 3-2. Set the MEGACYCLES dials for reception of a 02.0000 mc signal.

WARNING

Potentials as high as 125 volts are present in power supply circuits. Avoid contact.

e. TEST DATA. (See figures 5-5 and 5-19.) - Trouble shooting the front-end module consists of tracing signals through the signal path circuit and observing the phase-locked loop operation. Signal tracing is performed by checking the signal levels present at the first i-f amplifier (A1A2A3) circuit test point.

- (1) Connect signal generator to 50 Ω ANT connector on the panel (A1A1J1). Adjust generator for a 2.0 mc, 10 millivolts, unmodulated test signal.
- (2) Using the rf VTVM, measure signal level at test point J1(TP) on the first i-f module (A1A2A3). This should be a minimum of 5.5 millivolts, rms. Remove the signal generator and VTVM.
- (3) Connect oscilloscope to terminal 7 of phase-locked loop circuit (A1). Calibrate oscilloscope to measure a 100 volt peak-to-peak signal.
- (4) Disconnect synthesizer output cable at J1 on card rf #1(A) (A1A3A1A1). Note sweep ramp pattern on oscilloscope. Ramp level should be approximately 25 volts to 110 volts dc as it sweeps.
- (5) Reconnect synthesizer cable at J1 on card rf #1(A). Note locking of vhf oscillator at approximately 75 volts of ramp level.
- (6) Set MEGACYCLES dials on panel to read 29.9999 mc. Note sweep ramp action and vhf oscillator locking at approximately 25 volts dc of ramp level.
- (7) Remove test equipment. Remove test cable and replace front-end module in the front deck.

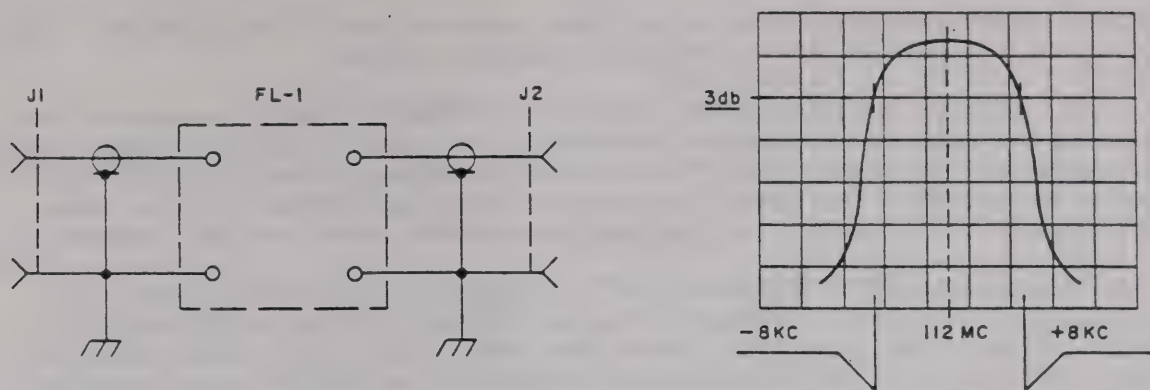


Figure 4-6. Roofing Filter A1A2FL1, Functional Diagram

4-7. ROOFING FILTER A1A2FL1. (See figure 4-6.)

The 112 mc roofing filter FL1 dictates the initial bandpass of the receiver signal path immediately following the front-end module (A1A2A2). Faulty filter operation can influence the receiver over-all gain and bandwidth or prevent reception completely.

a. DESCRIPTION. - The sealed 112 mc filter contains a balanced crystal-lattice circuit with a 112 mc center frequency. Nominal bandwidth is 16 kc at the -3 db points and the insertion loss is approximately 3 db.

b. PRELIMINARY CHECK. (See figure 4-6.) - With power off, make a preliminary check of the roofing filter with emphasis on the following:

(1) Cable connections to the filter component.

c. TEST DATA. (See figure 5-4.) - Trouble shooting the 112 mc roofing filter FL1 is not recommended. Because of the low signal level and high frequencies involved, signal tracing at this circuit will not be practical. Trouble shooting should be limited to an actual replacement of the filter FL1, if it is the cause of faulty operation.

4-8. FIRST I-F MODULE A1A2A3. (See figures 4-7 and 4-8.)

The first i-f module contains the 112 mc i-f amplifier and mixer (A1), and the 5 mc reserve gain i-f amplifier (A2), and includes the 112 mc roofing filter FL1, the 8 kc bandwidth 5 mc filter FL2, and the 117 mc buffer amplifier (A3). The main signal path between these two circuit sections is opened for insertion of the noise blanking module (A1A2A4) circuit described in paragraph 4-9. Faulty operation of the first i-f module can reduce signal strength, increase the receiver noise level, or prevent reception completely.

a. DESCRIPTION. - The receiver second frequency conversion is performed in this module, following signal amplification by the 112 mc i-f amplifier circuit. The conversion is performed by mixer Z1 (A1A2A3A1Z1). A 117 mc second injection frequency, supplied by the mixer/multiplier module (A1A3A2) in the synthesizer section (A1A3), is amplified by the 117 mc buffer amplifier (A3) and combined with the 112 mc first i-f frequency to obtain a 5 mc i-f output

frequency. Prior to amplification by the 5 mc reserve gain i-f amplifier the 5 mc signal frequency is passed through the noise blanking circuit.

(1) 112 MC AMPLIFIER/MIXER (A1). - The 112 mc i-f amplifier circuit contains two identical amplifiers employing four transistors in a special circuit arrangement. Bandpass filter FL1 couples the output of the first circuit to the input of the second. The special circuits permit a high dynamic range of agc voltage for control of amplifier gain without an adverse affect on signal linearity.

The first special circuit consists of Q1 through Q4. Q1 and Q3 form a dc differential amplifier with a fixed agc reference voltage applied to the base of Q3, and a signal derived agc voltage applied to the base of Q1. The 112 mc input signal to the module goes to the base of Q2 through a series-tuned circuit consisting of L2 and C3. The amplified signal at the collector of Q2 has two paths to follow. One is to ground via Q1 and capacitor C5, the other is to filter FL1 through cascode amplifier Q3 and the tuned circuit L6, C14, and C15. Because the reference agc voltage is constant, signal output to filter FL1 is determined by the value of agc voltage applied to Q1.

In addition to the agc action of Q1, Q4 also controls the gain of Q2 by functioning as a variable resistance in series with the Q2 emitter by-pass capacitor C12. The by-pass agc voltage applied to the base of Q4 controls its conduction and therefore its collector-to-emitter impedance, over a range from saturation to cut-off. Consequently, the current degeneration provided by emitter resistor R5 can be controlled by varying the by-pass agc voltage. Tuned circuit L7, C8, is tuned to 112 mc. When Q4 is biased to cut-off, the tuned circuit is adjusted to cancel the effect of the Q4 collector-to-emitter capacitance and assure removal of all by-pass capacitance at the emitter resistor R5.

The second special circuit consists of Q5 through Q8. Circuit operation is identical to that previously described for Q1 through Q4. Q5 and Q7 form the dc differential amplifier, Q7 the cascode stage, and Q8 the variable impedance stage in series with the Q6 emitter by-pass capacitor C25. A tuned circuit similar to that formed by L7, C8, is not required in this circuit.

During a typical operation, bypass agc is applied at relatively low levels of signal strength to control the gain of Q3 and Q7 by varying the degree of emitter by-passing. At higher signal levels, agc voltage is applied (in addition) to Q1 and Q5 to govern the output of Q3 and Q7 by controlling the differential amplifier operation. All agc voltages including the fixed reference agc are supplied by the agc amplifier circuit (A2) of the second i-f/agc amplifier module (A1A2A6). The capacitor signal dividers formed by C14 and C15 at tuned circuit L6, and C29 with C30 at tuned circuit L13, are used to obtain a low impedance output connection.

Mixer Z1 employs a diode balanced-modulator circuit. The 112 mc signal from Q7 is combined with the 117 mc second injection frequency to obtain a 5 mc output frequency. The balanced modulator circuit attenuates the 117 mc frequency and, although the 112 mc frequency also appears at the mixer output, it is attenuated by the low pass filter formed by C31, C32, and L14.

(2) 5 MC RESERVE GAIN AMPLIFIER (A2). (See figure 4-8.) - The 5 mc reserve gain i-f amplifier consists of bandpass filter FL2 and two cascode amplifiers Q1, Q2, and Q3, Q4. Transformer coupling is employed between the stages. The circuit arrangement assures a high dynamic signal range capability.

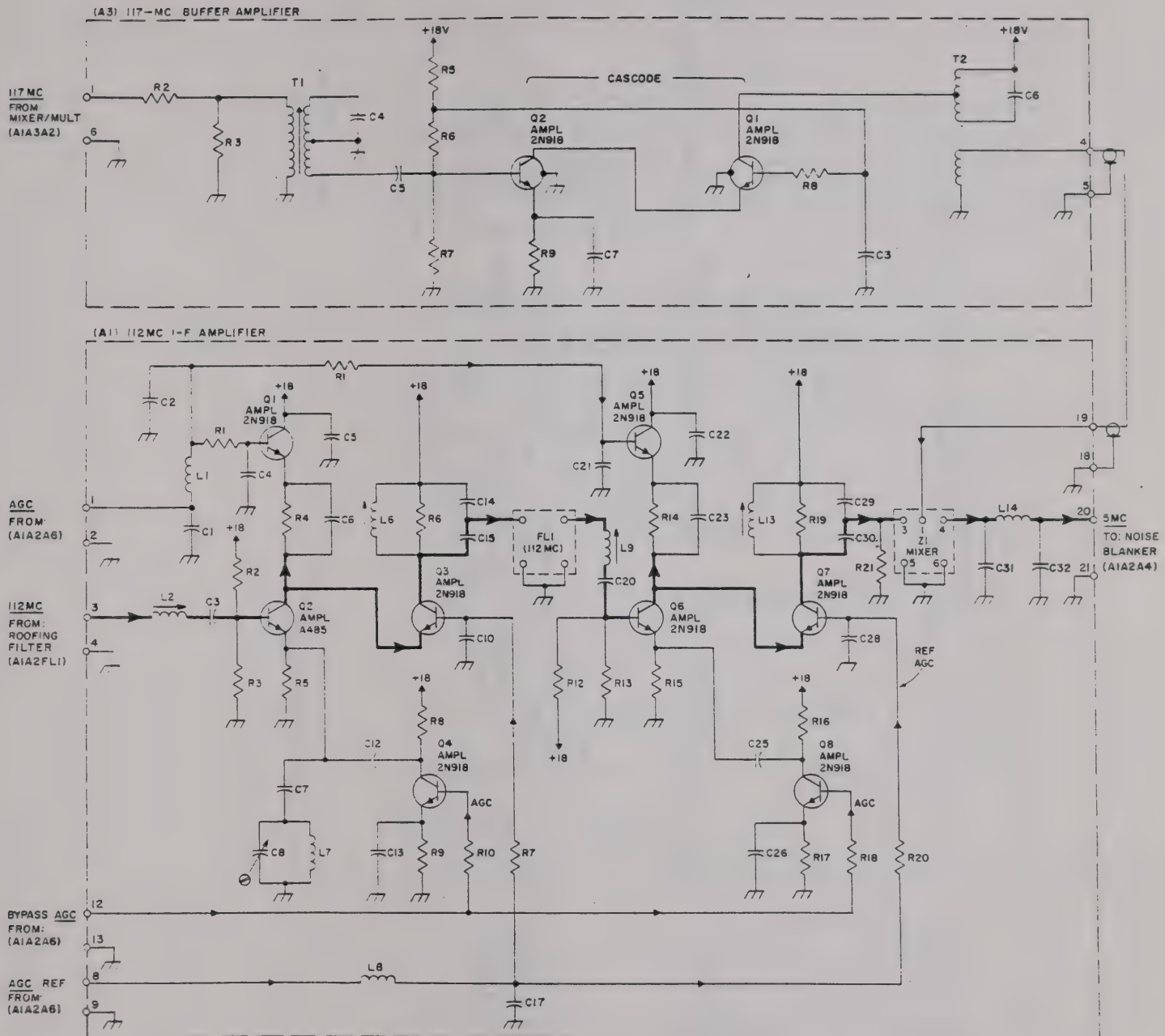


Figure 4-7. First I-F Module A1A2A3; 112 MC I-F Amplifier (A1) and 117 MC Buffer Amplifier (A3), Simplified Schematic Diagram

ORIGINAL

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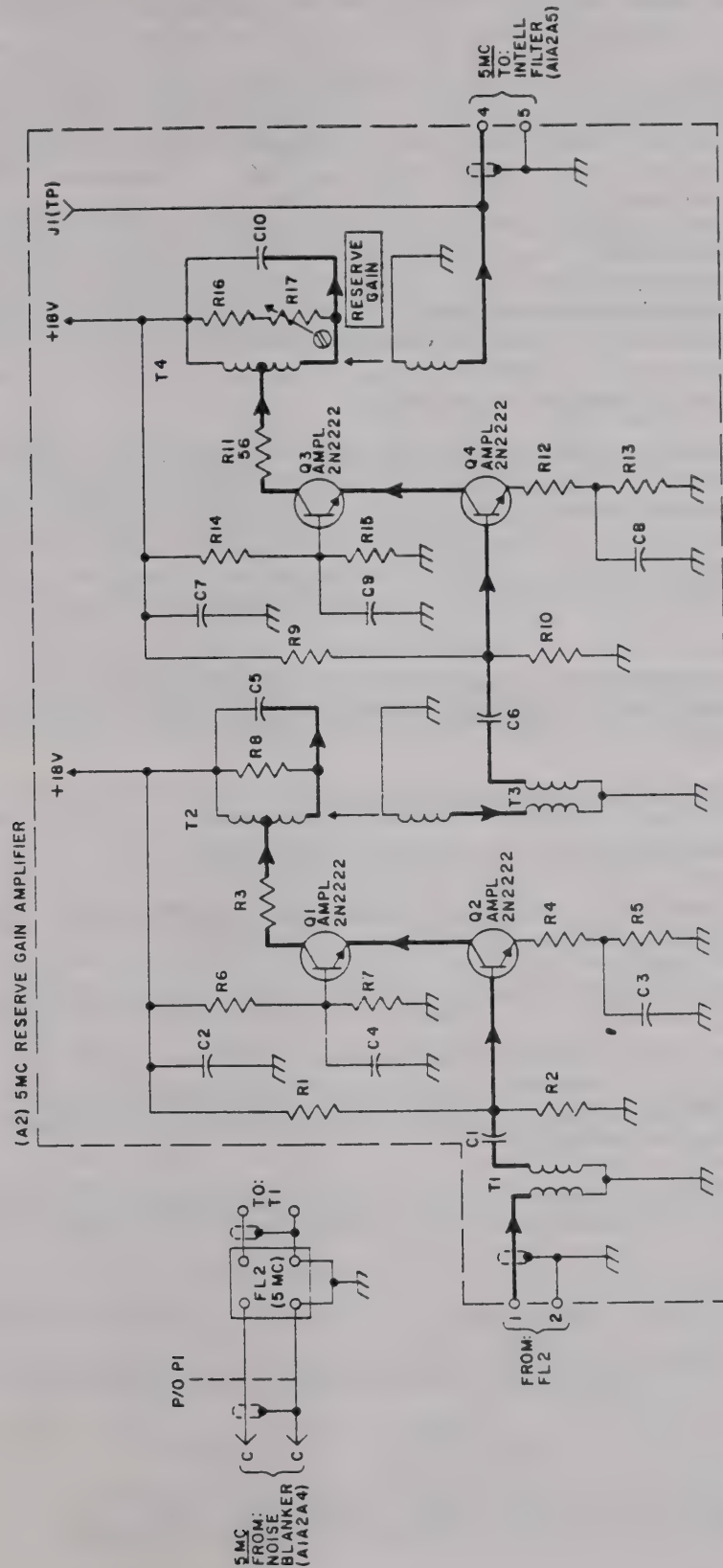


Figure 4-8. First I-F Module A1A2A3; 5 MC Reserve Gain Amplifier (A2),
Simplified Schematic Diagram

Adjustment R17 sets the amplifier output level and is usually set to provide approximately 20 db of reserve gain. This reserve gain factor is available to compensate for circuit aging over the service life of the receiver.

A 5 mc signal from the noise blanker module (A1A2A4) passes through 8 kc bandpass filter FL2 (p/o module A1A2A3) to the reserve gain amplifier input at transformer T1. Q1 and Q2 form a cascode amplifier circuit with the primary of transformer T2 serving as a load for the collector of Q1. Capacitor C5 tunes the primary winding and resistor R8 provides circuit damping to broaden the tuned circuit bandpass. The secondary of T2 couples the 5 mc signal to a similar cascode amplifier using Q3 and Q4, via transformer T3. The primary of T4, tuned by capacitor C10, functions as the tuned circuit load for the collector of Q3. Amplifier output is obtained at the secondary of T4. Adjustment R17 across the primary of T4 performs a circuit damping function as well as serving as an output level adjustment. Resistors R3 and R11 in the collector circuit of Q1 and Q3, respectively, function as parasitic suppressors.

(3) 117 MC BUFFER AMPLIFIER (A3). - The buffer amplifier consists of cascode amplifier Q1, Q2, input transformer T1 and output transformer T2. The 117 mc injection frequency from mixer/multiplier A1A3A2 is amplified prior to application at mixer Z1 in the 112 mc i-f amplifier/mixer circuit (A1). The secondaries of transformers T1 and T2 are tuned to 117 mc by capacitors C4 and C6, respectively. Resistors R2 and R3 form a signal attenuator at the input of transformer T1.

b. PRELIMINARY CHECK. (See figure 4-52.) - With power off, make a preliminary check of the 1st i-f module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D and VTVM ME-286/U, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Preset all controls as indicated in table 3-2.

e. TEST DATA. (See figure 5-5 and figures 5-21 through 5-24.) - Trouble shooting the first i-f module consists of applying a test signal from the signal generator to the receiver input and noting the signal level at the module output test point. Perform the following:

- (1) Connect signal generator to the 50 Ω ANT connector (A1A1J1) and adjust generator for a 10 millivolt, 2.0 mc, unmodulated test signal. Connect the rf VTVM to test point J1(TP) on the 5 mc reserve gain amplifier circuit (A2).
- (2) Set the MEGACYCLES dials to receive a 02.0000 mc signal.
- (3) Note the VTVM reading. It should be at least 30 millivolts, rms.

Note

This test also checks the signal path circuit (gated amplifier) in the noise blanker module (A1A2A4).

4-9. NOISE BLANKER A1A2A4. (See figures 4-9 and 4-10.)

The noise blanker module contains the 5 mc amplifier (A1), and the detector/gated amplifier circuit (A2). Faulty operation of the noise blanker module can cause signal distortion, reduce the signal strength, or prevent reception completely. Or, faulty operation can be evident as failure of the circuit to provide noise blanking.

a. DESCRIPTION. - Actual blanking of impulse type noise, rather than conventional noise suppression by clipping or limiting, is performed by this module. Essentially, the noise blanker consists of a 5 mc broadband amplifier which supplies noise samples; a Schmitt trigger to generate the blanking pulse, in response to a detected noise pulse; and a gated amplifier stage in the receiver main signal path.

When a noise pulse is received exceeding the level set by the NOISE BLANKING control, it is detected and applied to the Schmitt trigger circuit. The Schmitt trigger fires, opening the main signal path circuit just for the duration of the noise pulse. The level setting range for noise blanking is sufficient to cause blanking of the desired signal peaks when maximum blanking is used.

(1) 5 MC AMPLIFIER (A1). - The 5 mc noise amplifier consists of stages Q1 through Q7, forming a broadband high-gain amplifier exhibiting a fast response to impulse type noise and signal frequencies. Q2, Q3, and Q4 form a level control circuit with Q2 and Q4 functioning as a differential amplifier. A dc voltage from the NOISE BLANKING control is applied to the base of Q2, controlling the differential balance and therefore the signal level appearing at the output of Q4.

A 5 mc sample signal from mixer Z1 in the first i-f module (A1A2A3) is applied to the base of emitter follower Q1 via C1. Transformer T1 couples the signal to amplifier Q3. The output at the collector of Q3 has two paths to follow. One is to ground via Q2 and capacitor C6, the other to transformer T2 through cascode amplifier Q4. Consequently, the signal level at T2 is determined by the dc level applied to Q2 from the NOISE BLANKING control circuit. Stages Q5, Q6, and Q7, coupled by transformers T3 and T4, amplify the signal and apply it to the blanking circuit detector CR3 in the detector/gated amplifier circuit (A2). The +18 volt supply to all amplifier stages is controlled by the switch section of the NOISE BLANKING control. In the control OFF position, the supply is removed.

(2) DETECTOR/GATED AMPLIFIER (A2). - The detector/gated amplifier circuit consists of a gated amplifier in the receiver main signal path, Q4, Q5, and Q6, a Schmitt trigger composed of Q2 and Q3, and a diode detector CR3. Q4, Q5, and Q6 form a special gating circuit, similar to the three stage amplifiers employed in the 112 mc i-f amplifier (A1) in the first i-f module (A1A2A3).

Q4 and Q6 form a dc differential amplifier and the gating pulse from Schmitt trigger Q2 and Q3 is applied to Q4. Q5 and Q6, in turn, form a cascode amplifier in the receiver main signal path. The received signal (and noise) at the collector of Q5 has two paths to follow. One is to ground via Q4 and capacitor C8, whenever the Schmitt trigger operates, the other is to output transformer T2 through Q6. The Schmitt trigger provides a blanking action by effectively opening the main signal path circuit to the emitter of Q6 when Q4 conducts, by-passing the signal to ground via C8.

The received signal (and noise) amplified by the 5 mc amplifier circuit (A1)

is applied to detector CR3; diodes CR1 and CR2 perform a temperature compensating function to stabilize the level of detector operation. Amplifier Q1 raises the level of the detected signal and noise, and differentiation network C3 and R5 develops a trigger pulse to fire Schmitt trigger Q2 and Q3. Diode CR4 protects the base junction of Q2 in the event of extreme pulse levels. When the Schmitt trigger circuit fires, the generated pulse drives Q4 to saturation to remove the signal present at the collector of Q5 and drives Q6 to cut off. Because the Schmitt trigger fires during the duration of the differentiated pulse only, gating amplifier Q4 blanks the signal path just for this time period. The "or" gate formed by diodes CR5 and CR6 protects gating amplifier Q4 by limiting the junction reverse potential.

During operation of the noise blanking circuit, the NOISE BLANKING control sets the gain of the 5 mc amplifier (A1) and therefore the signal level applied to detector CR3. Normally, this setting is such that only the impulse noise peaks extending beyond the signal intelligence are detected. Consequently, blanking of the signal path occurs for the duration of each noise pulse only. An increase in the NOISE BLANKING control setting beyond this point will result in blanking of signal intelligence peaks as well as the more predominant noise peaks.

b. PRELIMINARY CHECK. (See figure 4-53.) - With power off, make a preliminary check of the noise blanking module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.
- (3) Operation of the NOISE BLANKING control and switch.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D, and Oscilloscope Tektronix 545A with head CA, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, adjust the NOISE BLANKING control as directed.

e. TEST DATA. (See figures 5-25 and 5-26.) - Trouble shooting the noise blanking module consists of checking the signal level at which blanking occurs, and verifying that the main signal path circuit is blanked and then restored.

(1) Connect signal generator to test point A1J1(TP) (noise blanker A1A2A4) and adjust the generator for a 5.0 mc test signal, modulated 100 per cent at 400 cycles. Connect the oscilloscope to test point A2J1(TP). Set the NOISE BLANKING control fully clockwise.

(2) Slowly increase the signal generator output until the dc blanking pulse appears, and note the generator signal level. It should be 60 uv, or less.

(3) Connect oscilloscope to test point A2J2(TP) and repeat step (2). Note disappearance of the 5 mc signal as blanking occurs. Adjust the NOISE BLANKING control over its range using various signal generator levels. Note that the control functions and that signal blanking occurs cleanly and abruptly. (Increase generator level as required.)

(4) Set the NOISE BLANKING control to OFF. Note that the signal level at A2J2(TP) is approximately 20 db greater than the signal generator output level, a voltage factor of 10.

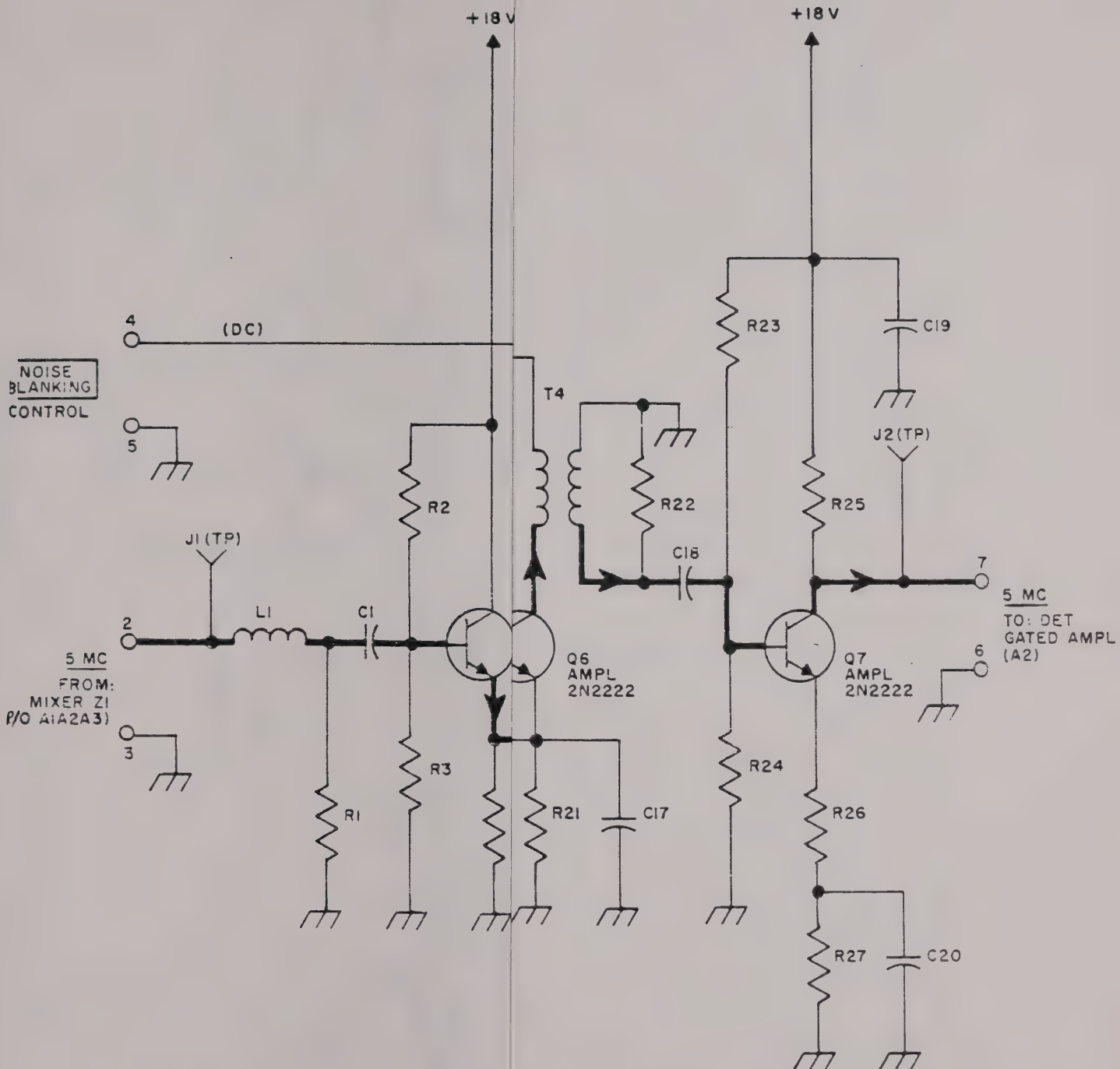


Figure 4-9. Noise Blanker A1A2A+;
5 MC Amplifier (A1),
Simplified Schematic Diagram

is applied to detector CR3; diodes CR1 and CR2 perform a temperature compensating function to stabilize the level of detector operation. Amplifier Q1 raises the level of the detected signal and noise, and differentiation network C3 and R5 develops a trigger pulse to fire Schmitt trigger Q2 and Q3. Diode CR4 protects the base junction of Q2 in the event of extreme pulse levels. When the Schmitt trigger circuit fires, the generated pulse drives Q4 to saturation to remove the signal present at the collector of Q5 and drives Q6 to cut off. Because the Schmitt trigger fires during the duration of the differentiated pulse only, gating amplifier Q4 blanks the signal path just for this time period. The "or" gate formed by diodes CR5 and CR6 protects gating amplifier Q4 by limiting the junction reverse potential.

During operation of the noise blanking circuit, the NOISE BLANKING control sets the gain of the 5 mc amplifier (A1) and therefore the signal level applied to detector CR3. Normally, this setting is such that only the impulse noise peaks extending beyond the signal intelligence are detected. Consequently, blanking of the signal path occurs for the duration of each noise pulse only. An increase in the NOISE BLANKING control setting beyond this point will result in blanking of signal intelligence peaks as well as the more predominant noise peaks.

b. PRELIMINARY CHECK. (See figure 4-53.) - With power off, make a preliminary check of the noise blanking module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.
- (3) Operation of the NOISE BLANKING control and switch.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D, and Oscilloscope Tektronix 545A with head CA, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, adjust the NOISE BLANKING control as directed.

e. TEST DATA. (See figures 5-25 and 5-26.) - Trouble shooting the noise blanking module consists of checking the signal level at which blanking occurs, and verifying that the main signal path circuit is blanked and then restored.

(1) Connect signal generator to test point A1J1(TP) (noise blanker A1A2A4) and adjust the generator for a 5.0 mc test signal, modulated 100 per cent at 400 cycles. Connect the oscilloscope to test point A2J1(TP). Set the NOISE BLANKING control fully clockwise.

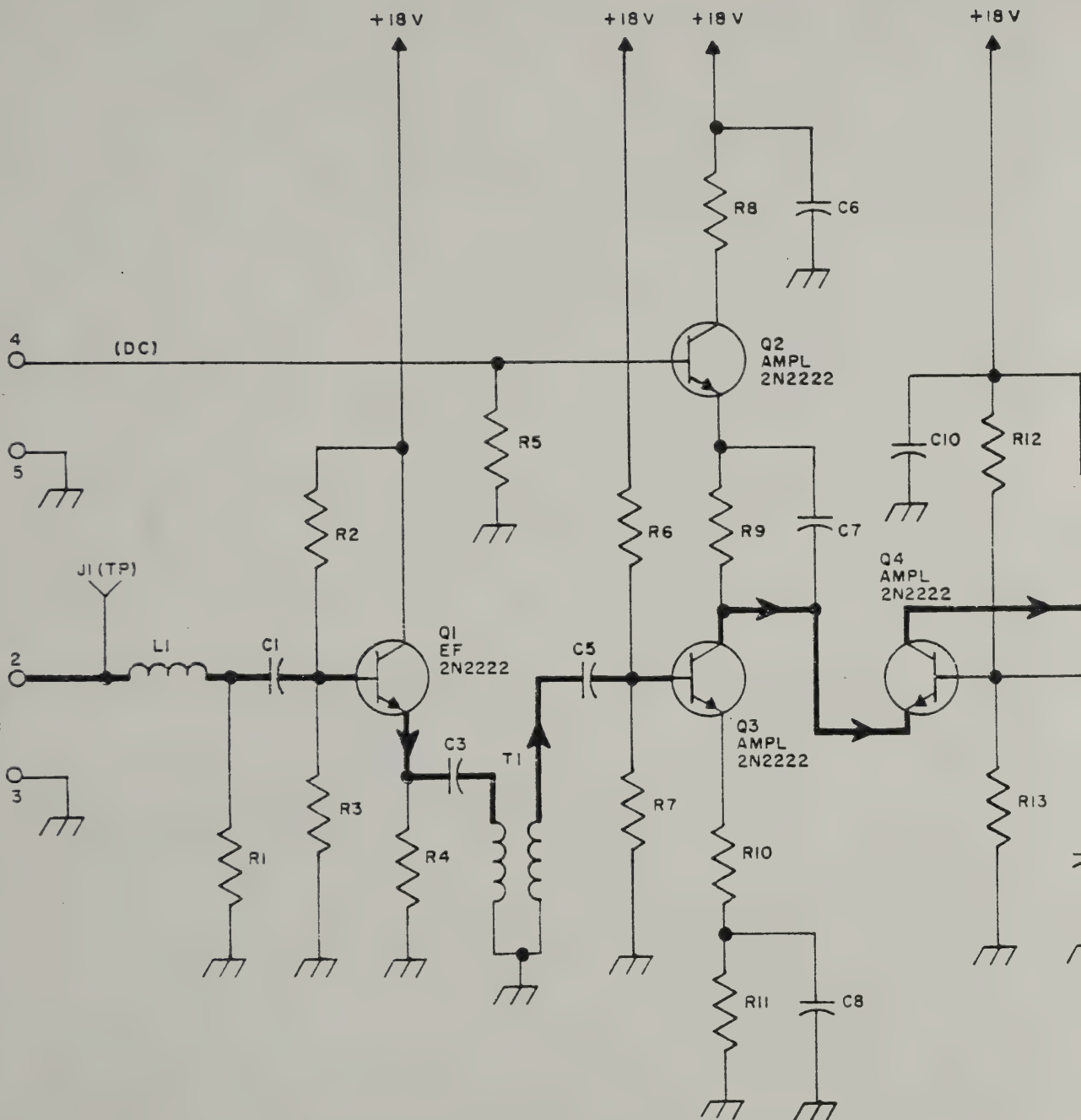
(2) Slowly increase the signal generator output until the dc blanking pulse appears, and note the generator signal level. It should be 60 uv, or less.

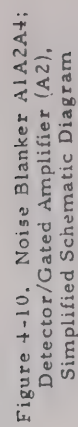
(3) Connect oscilloscope to test point A2J2(TP) and repeat step (2). Note disappearance of the 5 mc signal as blanking occurs. Adjust the NOISE BLANKING control over its range using various signal generator levels. Note that the control functions and that signal blanking occurs cleanly and abruptly. (Increase generator level as required.)

(4) Set the NOISE BLANKING control to OFF. Note that the signal level at A2J2(TP) is approximately 20 db greater than the signal generator output level, a voltage factor of 10.

NOISE
BLANKING
CONTROL

5 MC
FROM:
MIXER Z1
P/O A1A2A3)





4-10. INTELLIGENCE FILTER A1A2A5. (See figure 4-11.)

The intelligence filter module contains the BANDWIDTH selector switch and selectable bandpass filters for the cw, usb, and lsb reception modes. Faulty operation of the intelligence filter module can cause poor reception of a selected mode, or prevent reception completely.

a. DESCRIPTION. - This module provides the bandpass requirements for the various reception modes by selecting the appropriate intelligence filter. Filters FL1 (350 cycles) and FL2 (1 kc) provide a bandpass of 350 cycles and 1 kc, respectively. Filters FL3 and FL4 (300-3500 cycles) provide the bandpass required for upper and lower sideband reception. The bandwidths given are applicable at nominal 3 db points of the passband. The 8 KC position of the BANDWIDTH selector by-passes the filters through a "pi" type attenuator composed of resistors R4, R5, and R6. The attenuator inserts a signal loss similar to that encountered in the bandpass filters to maintain the signal level when changing from one BANDWIDTH selector position to the 8 KC position.

A 5 mc signal from the first i-f module (A1A2A3) goes to the BANDWIDTH selector switch S1 through a "pi" network consisting of resistors R1, R2, and R3. The network attenuates the input signal but primarily serves as a constant impedance signal-source for the intelligence filters. With exception of the 8 KC BANDWIDTH selector position, the over-all receiver bandwidth is determined by the particular intelligence filter selected. In the 8 KC position, the bandwidth is determined by the bandpass characteristics of FL2 in the first i-f module (A1A2A3).

b. PRELIMINARY CHECK. (See figure 4-11.) - With power off, make a preliminary check of the intelligence filter module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.
- (3) Operation of the BANDWIDTH selector switch.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D and VTVM ME-286/U, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, adjust the BANDWIDTH control as directed.

e. TEST DATA. (See figure 5-27.) - Trouble shooting the intelligence filter module consists of checking the signal insertion loss offered by the circuit for each position of the BANDWIDTH selector. Perform the following:

- (1) Remove first i-f module A1A2A3. Connect signal generator to pin W at A2XA3 and adjust generator for a 5.0 mc, 100 mv, unmodulated test signal. Connect the rf VTVM to test point A1J1(TP) at the second i-f/agc amplifier module (A1A2A6).

- (2) Set BANDWIDTH selector at 350 CPS, retune generator for maximum output, and note the VTVM reading. It should be 18 mv or more, representing a module insertion loss of approximately 15 db (a voltage ratio of 5.6 to 1).

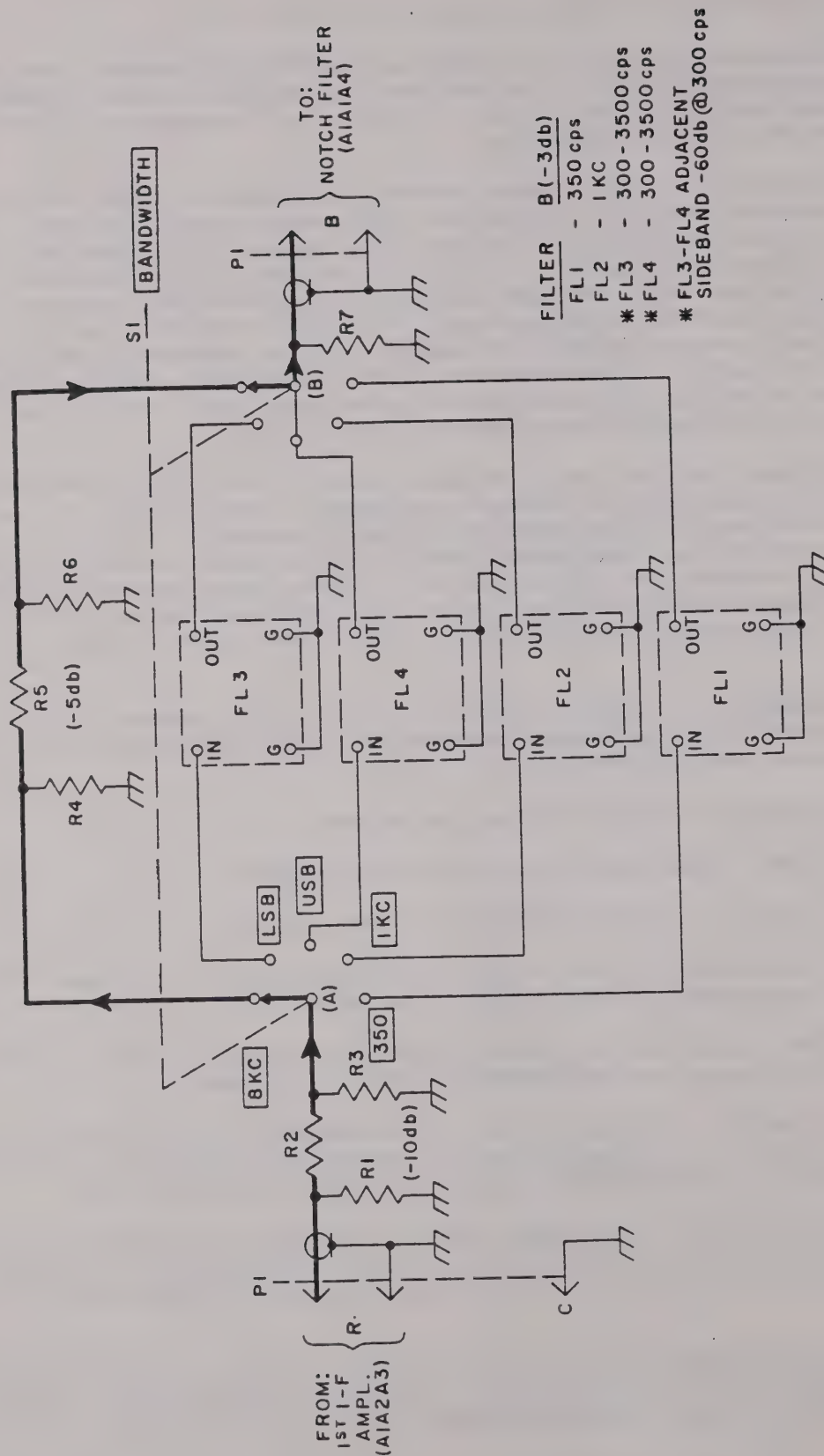


Figure 4-11. Intelligence Filter ALA2A5, Simplified Schematic Diagram

(3) Repeat step (2) for the remaining BANDWIDTH selector positions. Module insertion loss should be 15 db or less for each position.

4-11. NOTCH FILTER A1A1A4. (See figures 4-12, 4-13, and 4-14.)

The notch filter module, located on the front panel section (A1A1), consists of an amplifier-mixer circuit (A2), an oscillator-mixer circuit (A1), and bandpass filters FL1 and FL2 with the width selector switch S1. Faulty operation of the notch filter module can be evident as a failure of the circuit to provide a rejection notch or a complete loss of reception.

a. DESCRIPTION. - The notch filter provides the operator with a choice of a broad or sharp signal-rejection notch circuit, inserted into the main signal path when the WIDTH control is set at the BROAD or SHARP positions. In addition, the position of the selected notch or signal-rejection slot, with relation to the received signals, can be shifted within the signal path bandpass by adjusting the POSITION control. To perform this operation, two mixer stages are inserted into the main signal path. The 5 mc signal frequency is converted to 3.5 mc, passed through the selected notch filter, and reconverted back to 5 mc. A local oscillator, arranged in a drift-cancellation loop circuit, supplies the required 1.5 mc injection frequency to the two mixers. The POSITION control tunes the local oscillator over a small frequency range, centered at 1.5 mc, to obtain the effect of shifting the notch filter within the signal path bandpass. Because the output from the first mixer is a difference frequency and that from the second mixer a sum frequency, the local oscillator and amplifier circuit forms a drift-cancelling loop between the two mixers. The local oscillator frequency can be varied without changing the 5 mc output frequency from the second mixer, thereby maintaining the specified receiver frequency stability.

(1) AMPLIFIER-MIXER (A2). - The amplifier-mixer circuit consists of cascode amplifier Q1 and Q2, the first mixer Z1, and cascode amplifier Q3 and Q4. A 5 mc signal frequency from the intelligence filter module (A1A2A5) goes to the cascode amplifier Q1 and Q2 via transformer T1. Following signal amplification, it is applied to the first mixer Z1 through transformer T2. The primary of T2 is tuned to 5 mc by capacitor C5; resistor R7 functioning as a damping resistor. Mixer Z1 combines the 5 mc signal frequency with the local oscillator (p/o A1) 1.5 mc frequency to obtain the 3.5 mc frequency applied to the notch filters FL1 or FL2, via WIDTH selector switch S1. The resultant signal is then amplified by cascode amplifier Q3 and Q4, through transformer T3, and applied to output transformer T4. The primary of T4 is tuned by capacitor C9, resistor R13 providing a damping function. The 3.5 mc signal from the secondary of T4 is applied to a second mixer in the oscillator-mixer circuit (A1).

(2) OSCILLATOR-MIXER (A1). - The oscillator-mixer circuit consists of local oscillator Q1, cascode amplifier Q2 and Q3, amplifier Q4, and the second mixer stage Z1. Oscillator Q1 is arranged in a modified Colpitts circuit with the primary of transformer T1, tuned by capacitors C3, C4, C5, and C1 forming the tank circuit. Variable capacitor C1, adjusted by the POSITION control, will tune the oscillator frequency approximately 8 kc above or below the nominal 1.5 mc output frequency stipulated. Oscillator output is coupled to two circuits at the secondary of T1. One circuit is the first mixer Z1 (p/o amplifier-mixer A2), via coupling capacitor C6; the other circuit is cascode amplifier Q2 and Q3, through the attenuation network formed by resistors R5, R6, R7, and R8. The primary of transformer T2 is tuned to 1.5 mc by capacitor C9, and the secondary couples the signal to amplifier Q4. C13 passes the 1.5 mc signal to the second mixer Z1

where it is combined with a 3.5 mc frequency from amplifier-mixer circuit (A2) to obtain the 5 mc output frequency.

(3) CIRCUIT OPERATION. - When the WIDTH selector is at the OFF position, notch filters FL1 and FL2 are by-passed. The signal path frequency is converted to 3.5 mc at the first mixer Z1 (p/o A2) and back to 5 mc at the second mixer Z1 (p/o A2). Adjustment of the POSITION control to tune the local oscillator Q1 will have no effect on the 5 mc output frequency because of the drift-cancelling loop circuit arrangement, with or without the insertion of filters FL1 or FL2. When the WIDTH selector is at the BROAD or SHARP position, a rejection filter is placed in series with the 3.5 mc main signal path. Now, when the POSITION control is adjusted, the notch apparently is shifted within the signal path bandpass to remove undesired signal reception. Actually, the notch or rejection slot remains fixed at the nominal 3.5 mc center frequency. The signal frequencies are shifted instead. The maximum POSITION control range of approximately ± 8 kc will shift the local oscillator Q1 over a frequency range from 1.492 to 1.508 mc, and cause a corresponding shift in the 3.5 mc signal path frequency from 3.508 to 3.492 mc. For example: An interfering signal at 5.004 mc can be converted to 3.5 mc and removed by rejection filter FL1, simply by tuning the local oscillator to a frequency of 1.5004 mc ($5.004 - 1.5004 = 3.500$ mc).

The width of the signal path bandpass and therefore the usable range of the POSITION control is determined by the bandwidth selected by the BANDWIDTH control (p/o intelligence filter A1A2A5). The 8 KC or widest bandwidth selection is more than adequately covered by the POSITION control range, permitting the operator a wide degree of adjustment. Conversely, the 350 CPS bandwidth selection is not suitable for notch filter application because of the very narrow bandwidth involved. The two notch filters have a nominal 3.5 mc center frequency. The sharp filter FL1 has a 200 cycle bandpass, and the broad filter FL2 a 1.5 kc bandpass at 6 db down points on the response curve.

(4) DRIFT-CANCELLING LOOP. (See figure 4-14.) - The drift-cancelling loop for the local oscillator Q1 is formed by amplifier stages Q2 through Q4, terminating at the second mixer Z1 (all p/o A1). Figure 4-14 shows a functional diagram of the notch filter circuit, identifying the loop stages. Actual signal frequencies have been assigned, including a drift frequency, as an example to illustrate the drift-cancellation process. A local oscillator frequency shift of 1 kc has been assumed and appears adjacent to the signal frequencies, but is enclosed in parentheses for identification.

Local oscillator Q1, in the absence of a frequency shift, supplies a 1.5 mc frequency to two signal paths. One path, via mixer Z1 (p/o A2), provides a frequency conversion from 5.0 to 3.5 mc which passes through the selected notch filter and amplifier Q3, Q4, to mixer Z1 (p/o A1). The other path, through amplifiers Q2, Q3, and Q4 also reaches mixer Z1 (p/o A1), where the 3.5 mc frequency is converted back to 5.0 mc. Assuming a +1 kc shift in the oscillator Q1 frequency to 1.5001 mc, as shown in the example, the mixer Z1 (p/o A1) output frequency becomes 3.4999 mc ($5.0000 - 1.5001 = 3.4999$). Consequently, mixer Z1 (p/o A2) combines a 3.4999 mc and a 1.5001 mc frequency to obtain 5.0 mc ($3.4999 + 1.5001 = 5.0000$), output frequency. Although the oscillator Q1 frequency has been shifted +1 kc, the mixer Z1 (p/o A1) output frequency remains the same.

In the example, drift-cancellation (or shift-cancellation) of the local oscillator Q1 is obtained by arranging the circuit so that the first mixer Z1 output difference frequency is utilized, and the second mixer Z1 output sum frequency is

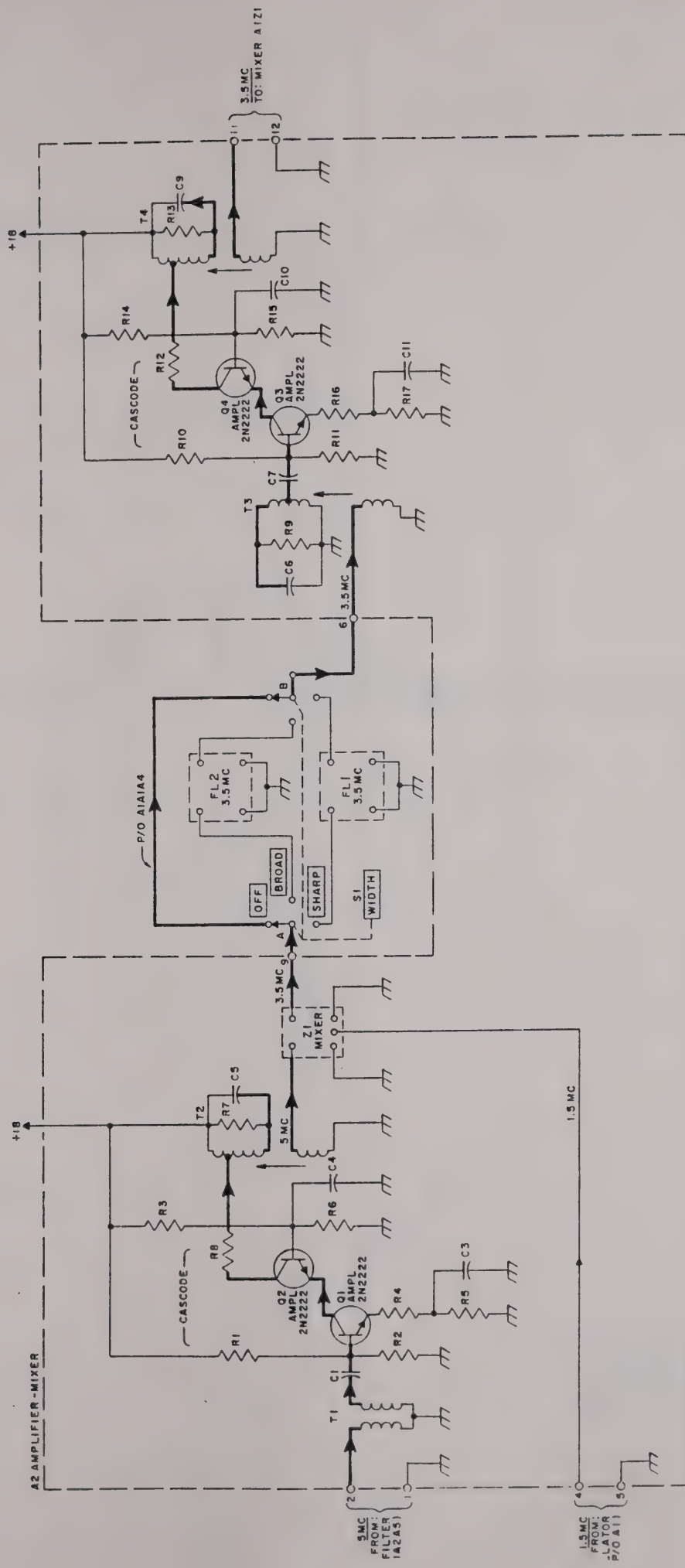


Figure 4-12. Notch Filter A1A1A4;
Amplifier-Mixer (A2),
Simplified Schematic Diagram

ORIGINAL

((1

D

(11

(A1) OSCILLATOR-MIXER

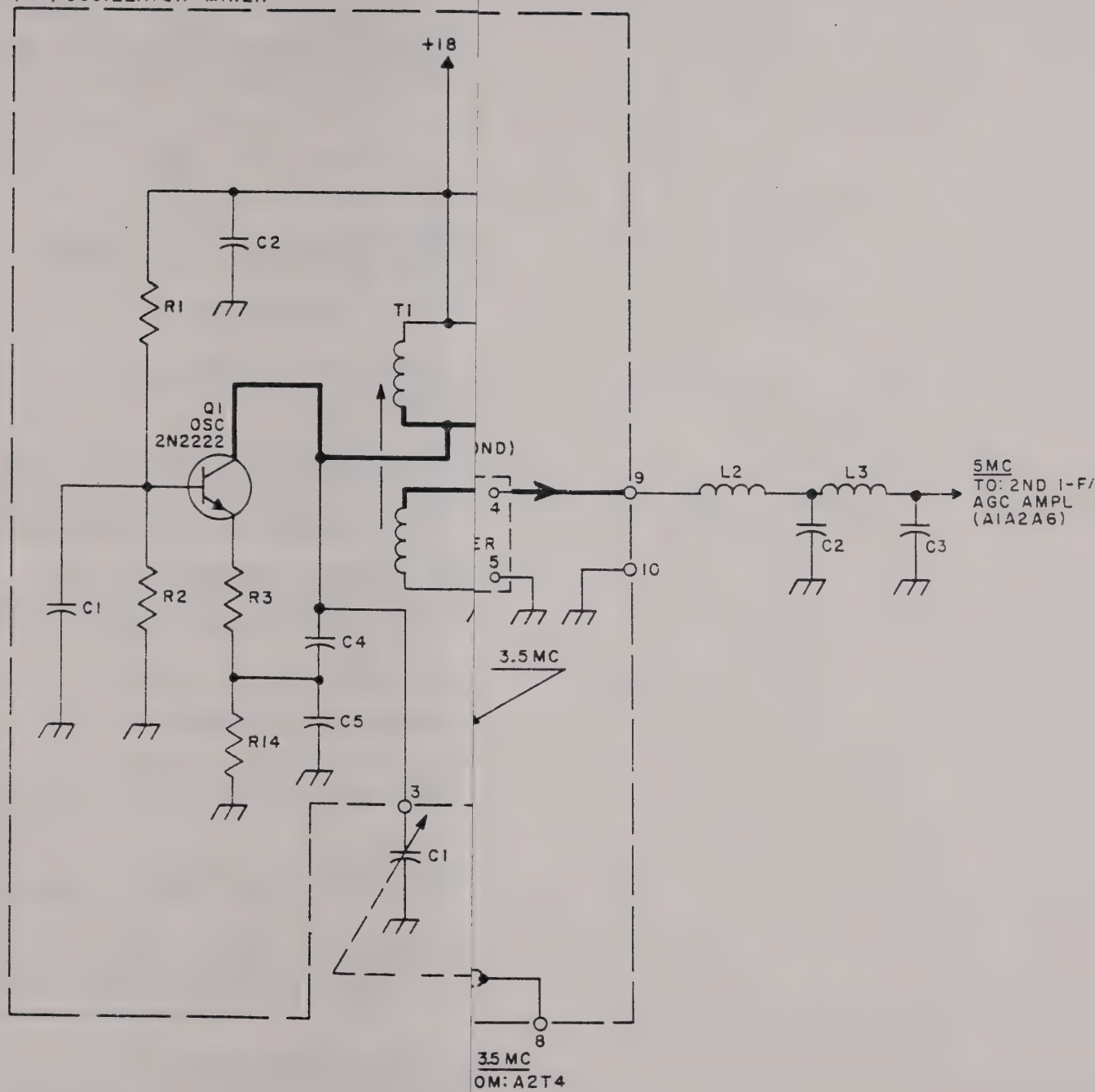


Figure 4-13. Notch Filter A1A1A4;
Oscillator-Mixer (A1),
Simplified Schematic Diagram

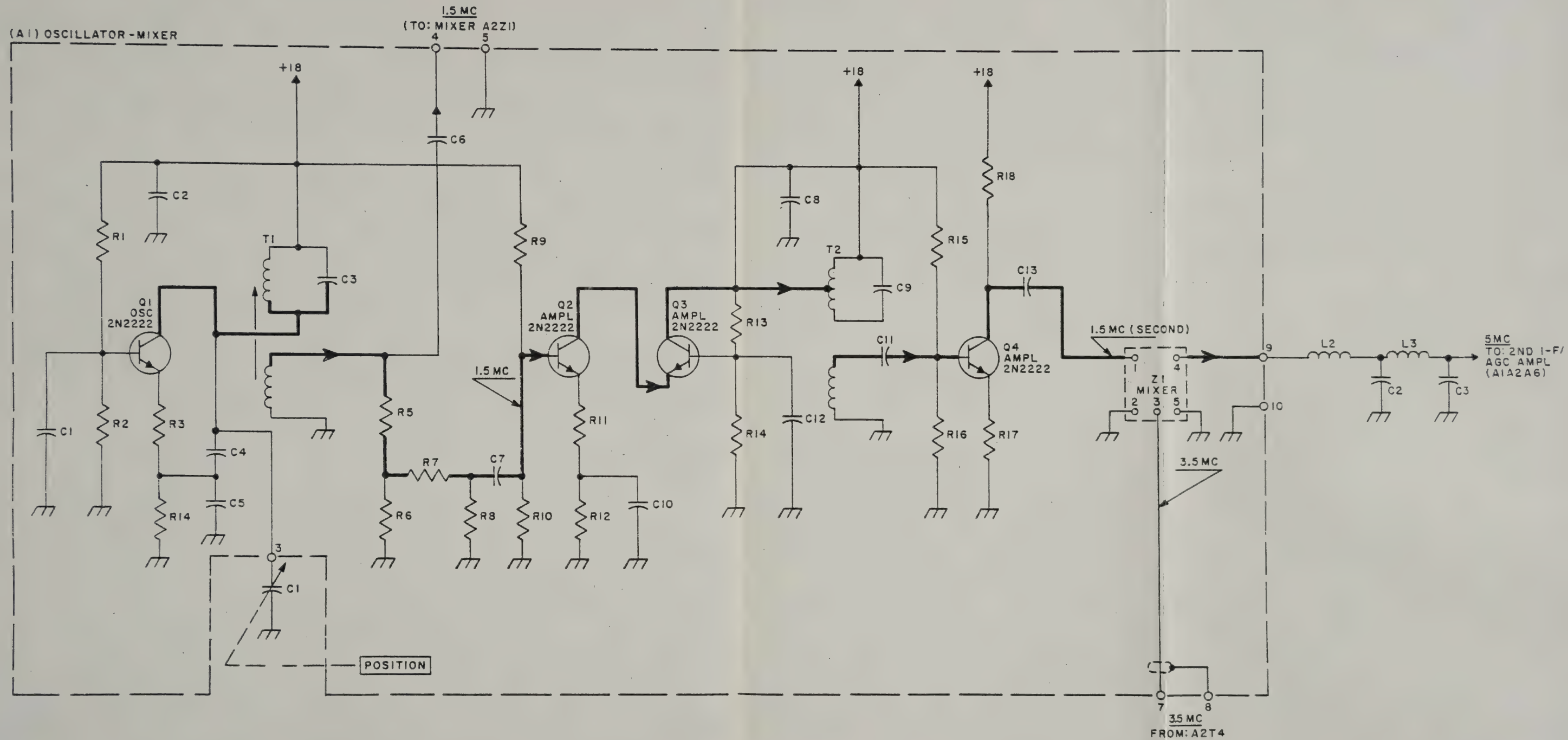


Figure 4-13. Notch Filter A1A1A4;
Oscillator-Mixer (A1),
Simplified Schematic Diagram

ORIGINAL

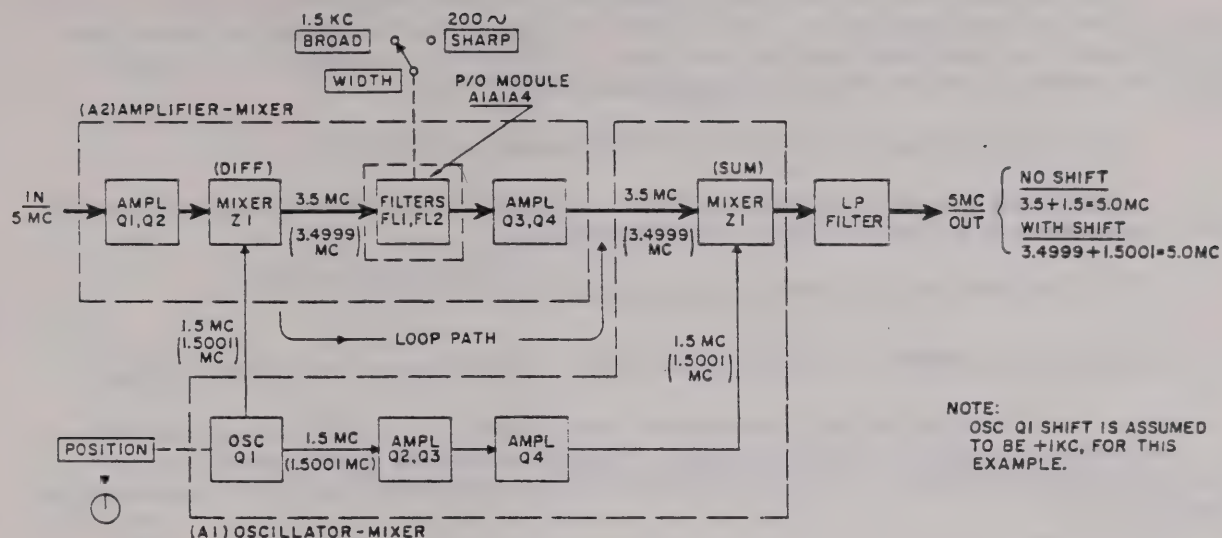


Figure 4-14. Notch Filter A1A1A4; Drift-Cancelling Loop, Functional Block Diagram

used. Because the main and the loop signal-path frequencies are shifted equally but in opposite directions (3.49999 versus 1.5001 for a 1 kc shift) there is no net frequency shift at the output of mixer Z1 (p/o A1). A negative frequency shift is cancelled in the same manner.

b. PRELIMINARY CHECK. (See figure 4-54.) - With power off, make a preliminary check of the notch filter module before beginning trouble shooting, with emphasis on the following:

- (1) Cable connections (if any) attached to module.
- (2) Operation of the WIDTH and POSITION controls.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D, Frequency Counter 5245L, and VTVM ME-286/U, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, adjust the WIDTH and POSITION controls as directed.

e. TEST DATA. (See figures 5-14, 5-15, and 5-16.) - Trouble shooting the notch filter module consists of checking the rejection effect of the two notch filters and the POSITION control range, using a signal generator test signal. Perform the following:

(1) Remove noise blanker module A1A2A4 and connect the signal generator to pin W of connector A2XA4. Adjust generator for a 5.0 mc, 50 mv, unmodulated test signal. Connect the rf VTVM to test point A1J3(TP) at the second i-f/agc amplifier module (A1A2A6). Place MODE switch at CW.

- (2) Note the VTVM reading. It should be 20 mv, or more.

(3) Set the WIDTH control to BROAD. Adjust POSITION control and note the filter notch characteristics. The VTVM reading should drop at the notch center. Increase the generator output until the VTVM reads the same as in step (2). (This is an output level increase of approximately 55 db.)

(4) Repeat step (3) with the WIDTH control at SHARP.

(5) Tune the generator to 5004 kc. Adjust the POSITION control and note the presence of a notch in the filter response.

(6) Repeat step (5) with the generator tuned to 4996 kc.

4-12. SECOND I-F/AGC AMPLIFIER A1A2A6. (See figures 4-15 and 4-16.)

The second i-f/agc amplifier module contains the 5 mc second i-f amplifier (A1), and the agc amplifier (A2) circuits. Faulty operation of this module can reduce the signal strength, increase the receiver noise level, or prevent reception completely.

a. DESCRIPTION. - This module provides additional amplification of the 5 mc i-f signal prior to demodulation at the detector/af amplifier module (A1A2A7). In addition, it contains the receiver agc amplifier which supplies agc voltages to the first i-f amplifier module (A1A2A3), the 5-mc i-f amplifier portion of this module, and to the RF IN circuit of the panel mounted signal-level meter.

(1) SECOND I-F AMPLIFIER (A1). - The 5 mc second i-f amplifier consists of three special stages of amplification, utilizing a triple-transistor configuration similar to that described in paragraph 4-9a(1). The first stage employs Q1 and Q3 as a differential amplifier, with Q2 and Q3 forming a cascode amplifier. Agc voltage is applied to Q1 to control the stage gain. The next stage using Q4, Q5, and Q6 functions in a similar fashion. The final stage with Q7, Q8, and Q9 differs only in the function of Q7. This transistor, in response to a switching voltage from the receiver MODE switch, selects the particular detector circuit to be used in the next module, detector/af amplifier (A1A2A7), by switching the output circuits. For the cw and ssb modes, Q8 and Q9 form a cascode amplifier circuit. For the am mode, Q7 and Q8 operate as a cascode amplifier.

A 5 mc signal from the notch filter module (A1A1A4) is applied to the primary of transformer T1. The transformer secondary is tuned to 5 mc by capacitor C24 to reject other frequency components present at the notch filter output. Resistor R1 damps the tuned circuit. The amplified signal at the collector of Q2 has two paths to follow: one to ground via Q1 and capacitor C3, the other to transformer T2 through cascode amplifier Q3. The signal division is determined by the agc voltage applied to the base of Q1, and thereby the differential amplifier balance to control the over-all stage gain. The primary of T2 is tuned by capacitor C8, with resistor R11 providing the damping function.

The next stage using Q4, Q5, and Q6 duplicates the first stage function. Transformer T3 couples the signal to the base of Q5, and the tuned circuit at the collector of Q6 consists of the primary of transformer T4, tuning capacitor C17, and damping resistor R21. A fixed agc reference voltage, supplied from the agc amplifier circuit (A2) is applied to Q3 and Q6 to initially set the stage output levels in the absence of an applied agc voltage to Q1 and Q4.

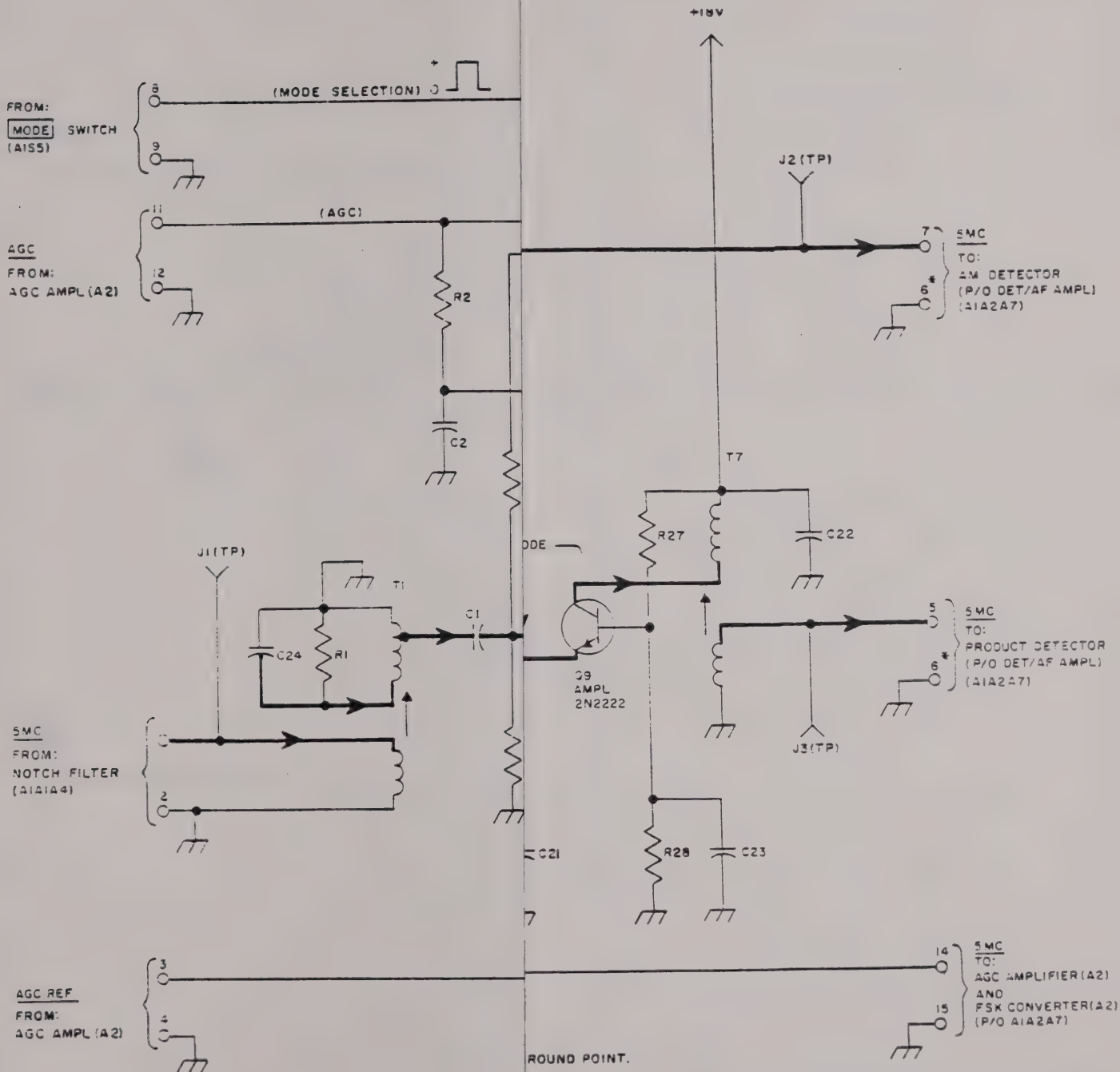


Figure 4-15. Second I-F/AGC Amplifier
A1A2A6: Second I-F Amplifier (A1),
Simplified Schematic Diagram

(3) Set the WIDTH control to BROAD. Adjust POSITION control and note the filter notch characteristics. The VTVM reading should drop at the notch center. Increase the generator output until the VTVM reads the same as in step (2). (This is an output level increase of approximately 55 db.)

(4) Repeat step (3) with the WIDTH control at SHARP.

(5) Tune the generator to 5004 kc. Adjust the POSITION control and note the presence of a notch in the filter response.

(6) Repeat step (5) with the generator tuned to 4996 kc.

4-12. SECOND I-F/AGC AMPLIFIER A1A2A6. (See figures 4-15 and 4-16.)

The second i-f/agc amplifier module contains the 5 mc second i-f amplifier (A1), and the agc amplifier (A2) circuits. Faulty operation of this module can reduce the signal strength, increase the receiver noise level, or prevent reception completely.

a. DESCRIPTION. - This module provides additional amplification of the 5 mc i-f signal prior to demodulation at the detector/af amplifier module (A1A2A7). In addition, it contains the receiver agc amplifier which supplies agc voltages to the first i-f amplifier module (A1A2A3), the 5-mc i-f amplifier portion of this module, and to the RF IN circuit of the panel mounted signal-level meter.

(1) SECOND I-F AMPLIFIER (A1). - The 5 mc second i-f amplifier consists of three special stages of amplification, utilizing a triple-transistor configuration similar to that described in paragraph 4-9a(1). The first stage employs Q1 and Q3 as a differential amplifier, with Q2 and Q3 forming a cascode amplifier. Agc voltage is applied to Q1 to control the stage gain. The next stage using Q4, Q5, and Q6 functions in a similar fashion. The final stage with Q7, Q8, and Q9 differs only in the function of Q7. This transistor, in response to a switching voltage from the receiver MODE switch, selects the particular detector circuit to be used in the next module, detector/af amplifier (A1A2A7), by switching the output circuits. For the cw and ssb modes, Q8 and Q9 form a cascode amplifier circuit. For the am mode, Q7 and Q8 operate as a cascode amplifier.

A 5 mc signal from the notch filter module (A1A1A4) is applied to the primary of transformer T1. The transformer secondary is tuned to 5 mc by capacitor C24 to reject other frequency components present at the notch filter output. Resistor R1 damps the tuned circuit. The amplified signal at the collector of Q2 has two paths to follow: one to ground via Q1 and capacitor C3, the other to transformer T2 through cascode amplifier Q3. The signal division is determined by the agc voltage applied to the base of Q1, and thereby the differential amplifier balance to control the over-all stage gain. The primary of T2 is tuned by capacitor C8, with resistor R11 providing the damping function.

The next stage using Q4, Q5, and Q6 duplicates the first stage function. Transformer T3 couples the signal to the base of Q5, and the tuned circuit at the collector of Q6 consists of the primary of transformer T4, tuning capacitor C17, and damping resistor R21. A fixed agc reference voltage, supplied from the agc amplifier circuit (A2) is applied to Q3 and Q6 to initially set the stage output levels in the absence of an applied agc voltage to Q1 and Q4.

AN/GRR-17
TROUBLE SHOOTING

TM-05866A-15

Figure
4-15

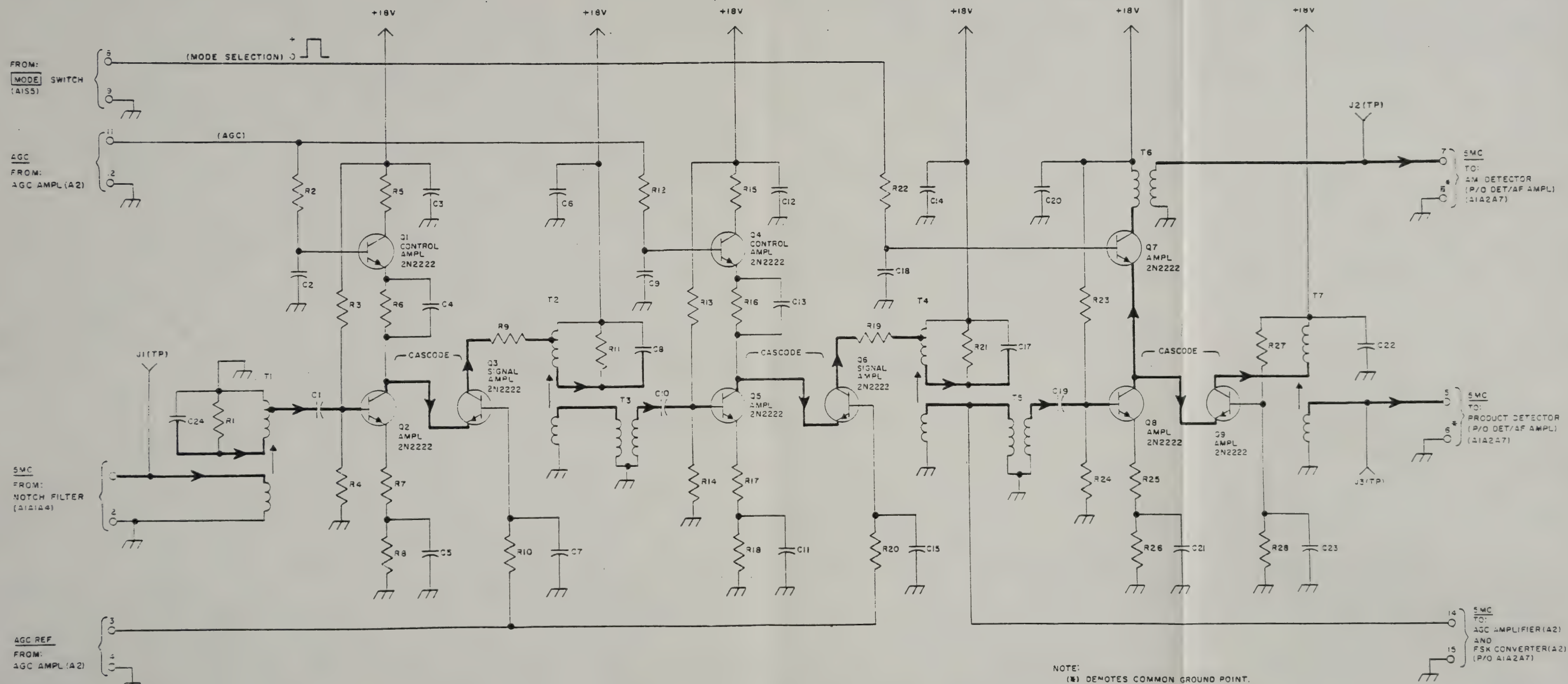


Figure 4-15. Second I-F/AGC Amplifier
A1A2A6: Second I-F Amplifier (A1),
Simplified Schematic Diagram

ORIGINAL

4-15/4-16

HOOTING

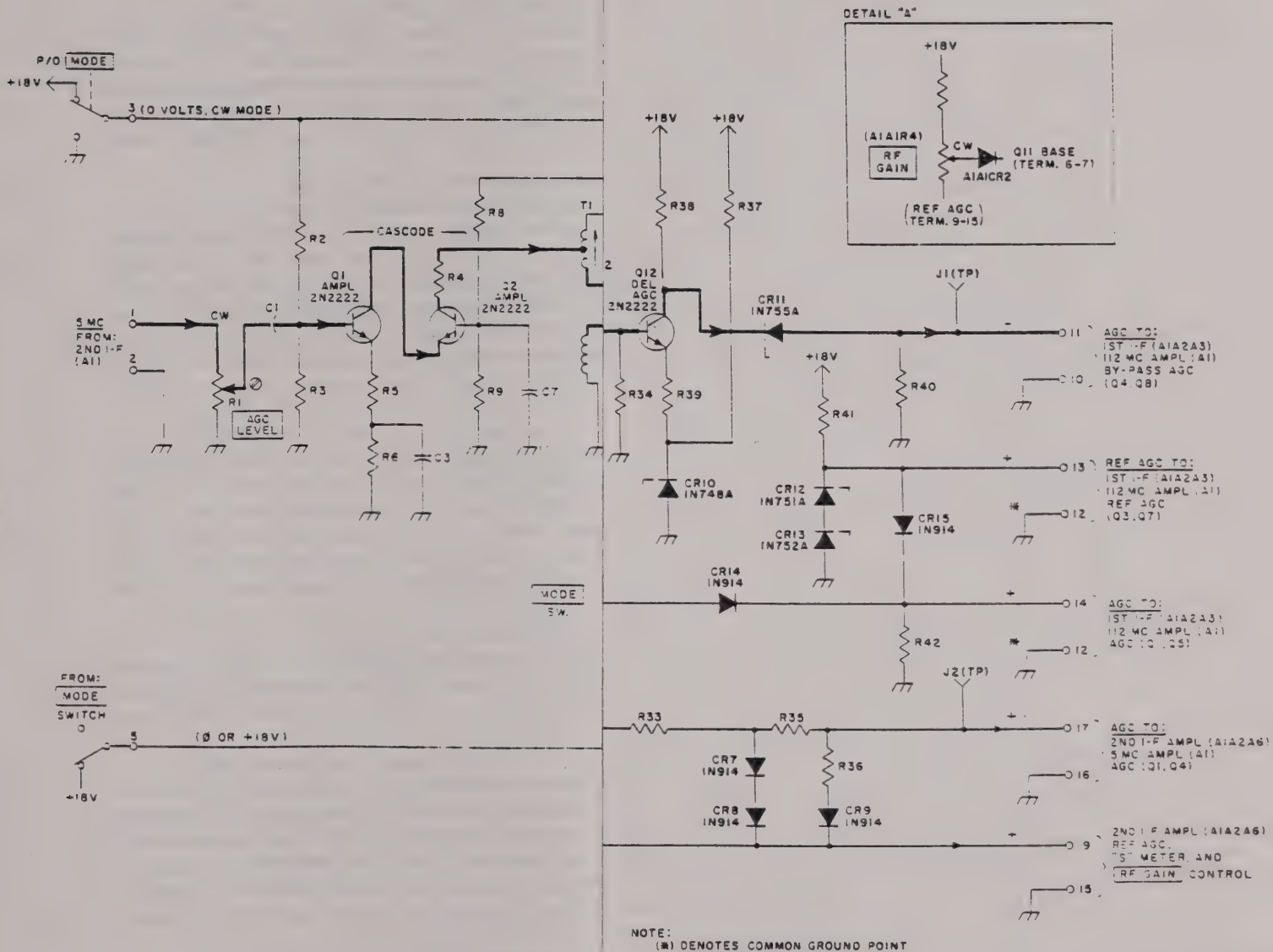


Figure 4-16. Second I-F/AGC Amplifier
A1A2A6: AGC Amplifier (A2),
Simplified Schematic Diagram


$$\frac{1}{2} - \frac{1}{4} = \frac{1}{4} \quad \frac{1}{2} - \frac{1}{4} = \frac{1}{4}$$

Transformer T5 couples the signal to the final amplifier stage. In the absence of a dc switching voltage from the MODE switch, cascode amplifier Q8 and Q9 supplies a 5 mc signal to the product detector (p/o detector/af amplifier A1A2A7), via transformer T7. When the MODE switch is at the AM position, a positive voltage is applied to the base of Q7 and Q9 becomes cut off, diverting the signal through transformer T6 to the am detector circuit (p/o detector/af amplifier A1A2A7). When Q7 is triggered "on", the common emitter current by-passes Q9 and it becomes cut off.

(2) AGC AMPLIFIER (A2). - The agc amplifier circuit contains the input amplifier Q1, Q2, and Q3; the agc detector/agc dump circuit consisting of diode CR2, dc amplifier Q8, Q9, and Q10, and dump circuit Q4, Q5, Q6, and Q7; and the agc distribution circuit Q11 and Q12, and CR6 through CR15. These circuits develop, process, and control the agc reference, agc by-pass, and conventional agc voltages which control the gain of the receiver i-f amplifier circuits.

(a) INPUT AMPLIFIER. - The input amplifier consists of cascode amplifier Q1 and Q2, and amplifier Q3, including the initial agc delay circuit of Zener diode CR1. A 5 mc signal from the second i-f amplifier circuit (A1) is applied to the base of Q1 through the AGC LEVEL control R1. The primary of T1, in the Q2 collector circuit, is tuned to 5 mc by capacitor C5 with resistor R7 performing a damping function. From the secondary of T1, the signal is amplified by Q3 and applied to the CR1 agc delay circuit, via auto-transformer T2. Capacitor C10 tunes the transformer to 5 mc and the collector of Q3 is tapped-down to obtain a low-impedance match.

The first or initial agc delay circuit consists of inductor L3, capacitor C13, and the Zener diode CR1. The regulated potential across CR1 is applied to the agc detector CR2 as a back-bias, through inductor L3. Capacitor C13 performs an rf by-pass function. Consequently, the 5 mc signal level must exceed the bias level before agc detector CR2 can conduct, producing an agc voltage. This circuit delays all agc voltages supplied by the agc amplifier, with exception of the reference agc voltages contributed by Zener diode circuits.

(b) DETECTOR/AGC DUMP CIRCUIT. - The agc detector and dump circuit consists of detector CR2, gate CR5, dc amplifier Q8, Q9, and Q10 and dump circuit Q4, Q5, and Q7. Q6 functions as a switch-circuit to change the agc time constant developed by capacitor C16 and resistor R21.

The amplified 5 mc signal from Q3 is detected by diode CR2, and the resultant dc voltage charges time-constant capacitor C16 through resistor R18. Gate diode CR5 assures that in the absence of a signal C16 will discharge at a slow rate through resistor R21, rather than an unintended path in the previous stages. Agc voltage developed at C16 is amplified by a three stage dc amplifier. Q8 and Q9 form a Darlington circuit for a high current gain, and the inverted PNP stage Q10 supplies the agc distribution and control circuits which follow.

The agc dump circuit consisting of Q4, Q5, and Q7 removes the charge at capacitor C16 in the absence of a received signal, in preparation for the signal reappearance. In this fashion, the long agc time constant contributed by C16 and R21 is removed and re-established, at intervals determined by the received signal characteristics, for optimum gain control in direct proportion to the signal level at all times. With a signal present, Q4 samples the detector CR2 output and becomes saturated, limiting the voltage on the emitter of unijunction stage Q5 to stop its operation. In the absence of a signal, Q4 becomes cut off permitting

capacitor C15 to charge from the +18 volt supply via resistor R19. When a high level of charge is obtained, dump generator Q5 "fires" generating a sawtooth output pulse. The pulse causes Q7 to saturate and provide a quick discharge path for capacitor C16 to remove most of its charge. The generation of a dump pulse by Q5 will continue until a signal reappears to saturate Q4. The dump cycle described is repeated each time the received signal pauses sufficiently to cut off Q4, and allow C15 to charge to the firing point of Q5.

Resistor R18 sets the time-constant for charging capacitor C16, and resistor R21 the time-constant for capacitor discharge. The resultant fast-attack slow-decay agc voltage characteristics are directly related to the values of R18 and R21, 4.7 k and 10 mego, respectively, and are employed for the receiver USB and LSB reception modes. For the reception using the FSK and AM modes, the decay time is speeded-up by the operation of Q6. With the MODE switch on the receiver panel at FSK or AM, a positive potential is applied to the base of Q6 causing it to saturate and effectively ground the lower end of resistor R25. This switch-action places R25 in parallel with resistor R21, and capacitor C16 is discharged at a faster rate to obtain a fast decay time for the agc voltage. In addition, the MODE switch applies a +18 volt potential to resistor A1A1R6, placing it in parallel with R19 to allow capacitor C15 to charge at a faster rate. This action causes dump generator Q5 to "fire" more quickly and is compatible with the speed-up in the C16 discharge time. Agc is not employed for the CW mode of operation. With the MODE switch at CW, the +18 volt supply is removed from agc amplifier stages Q1 through Q3 to disable this portion of the circuit.

Zener diode CR4 supplies the agc reference voltage for the operation of several receiver circuits. It also establishes an "above ground" termination for the emitter circuits of Q4, Q5, and Q7 and the dc amplifiers Q8, Q9, and Q10. Diode CR3 functions as a dc clamp to establish the minimum agc dump level when Q7 saturates. In this manner, capacitor C16 is not completely discharged by Q7, but only to the level necessary to remove agc voltage at the input circuit (base-to-emitter) of dc amplifier Q8.

(c) AGC DISTRIBUTION AND CONTROL. - The agc distribution and control circuit consists of "or" gate CR6 and Q11, a (second) agc delay circuit using CR10 and Q12, a (second) agc reference supply using CR12 and CR13, an agc shaping circuit employing CR7, CR8, and CR9, and the "or" gate formed by CR14 and CR15. These circuits control the distribution of agc voltages to the various receiver circuits.

Diode CR6 and transistor Q11 form a logic "or" gate at the input of dc amplifier Q12. The gate permits application of an agc control voltage from dc amplifier Q10 or the RF GAIN control circuit via Q11, but prevents the RF GAIN control from loading the normal agc signal path. When the RF GAIN control setting produces a dc voltage greater than the signal derived voltage, the RF GAIN control assumes a manual control of receiver gain. Agc voltage to operate the signal level meter on the receiver panel is supplied from the agc signal path through resistor R31.

Dc amplifier Q12 amplifies the agc voltage, from either source, subject to the delay potential of Zener diode CR10. The agc voltage must exceed that of the Zener diode to obtain agc output voltage from Q12. This circuit action allows a maximum receiver gain for weak signal reception by limiting or delaying the development of agc voltage until stronger signals are received. Zener diode CR11, in conjunction with resistor R40, functions as a dc clamp to re-establish the agc

voltage with respect to ground, following amplification by Q12. Agc voltage from this circuit is applied to the first i-f amplifier module (A1A2A3) at terminals 11-10.

Zener diodes CR12 and CR13, in series, supply the agc reference voltage for the first i-f amplifier at terminals 13-12. The logic "or" gate by diodes CR14 and CR15 applies this reference agc voltage as a conventional agc voltage to the first i-f amplifier at terminals 14-12, until the signal derived agc voltage via CR14 exceeds the reference agc value, acquiring control. This circuit action occurs only during the reception of strong signals.

Diodes CR7, CR8, CR9 and resistors R33, R35, and R36 form a step-type agc voltage shaping network, tailoring the agc response to fit the requirements of the second i-f amplifier (A1A2A6) at terminals 17-16. Response shaping is a function of diode conduction and the related dc voltage drop at resistors R33 and R35, in series with the agc distribution circuit. The reference voltage developed by Zener diode CR4 serves to reverse-bias the diodes, preventing conduction until the signal developed agc voltage, through R33, exceeds the bias value. Diode conduction occurs in two steps, and the resultant agc voltage does not rise in value as rapidly as the unshaped agc voltage. When the bias voltage exceeds the agc voltage during the reception of weak signals, diode conduction does not occur and the agc voltage from the network is directly proportional to the signal level. For stronger signals causing CR9 to conduct, the conduction current produces a dc voltage drop across R33 and R35, opposing the agc voltage and reducing its value. Consequently, the resultant agc voltage is not proportional to the signal level. For higher signal levels, diodes CR7 and CR8 conduct increasing the opposing voltage drop at R33, to produce a greater decrease in the shaped agc voltage with respect to the unshaped agc voltage. Actually, the shaping network tapers the agc voltage response curve to fit the control requirements of the second i-f amplifier (A1A2A6).

Zener diode CR4 supplies a fixed reference voltage to the second i-f amplifier (A1A2A6), the RF GAIN control circuit and also to the signal-level panel meter circuit, via the METER FUNCTION switch on the front panel. When used for manual control of receiver gain, the RF GAIN control regulates the gain of the first i-f amplifier (A1A2A3) at distribution terminals 11-10 and 14-12, and the second i-f amplifier (A1A2A6) at terminals 17-16.

b. PRELIMINARY CHECK. (See figure 4-55.) - With power off, make a preliminary check of the second i-f/agc amplifier module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.
- (3) Operation of the RF GAIN control.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D, VTVM ME-286/U, and VTVM AN/USM-116, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, adjust the RF GAIN and the MODE controls as directed.

e. TEST DATA. (See figures 5-28 and 5-29.) - Trouble shooting the second i-f/agc amplifier module consists of measuring the i-f amplifier (A1) gain and checking operation of the agc amplifier (A2), using a signal generator test signal. Perform the following:

(1) Connect signal generator to the 50 Ω ANT connector (A1A1J1) and adjust generator for a 5 mc, 10 mv, unmodulated test signal. Set the MODE switch to SSB.

(2) Remove the detector/af amplifier module A1A2A7 and connect the rf VTVM (with 50 ohm termination) to pin A of connector A2XA7.

(3) Adjust A1R1 for a meter reading of 25 to 30 mv (rms).

(4) Replace detector/af amplifier module A1A2A7. Set MODE switch to AM. Connect rf VTVM to test point A1J2(TP). Meter should read 55 mv (rms), minimum.

(5) Connect generator to test point A1J1(TP). Connect dc VTVM to test point A2J1(TP). Adjust generator level, starting at 10 mv and increasing.

(6) Note VTVM reading. It should change from approximately +2.5 volts to zero volts for a generator level change of 20 db.

(7) Connect dc VTVM to test point A2J2(TP) and repeat the step (5) test signal adjustment. The meter reading should change from approximately +9.5 volts to +10.5 volts when the generator level is increased to maximum output.

(8) Reconnect dc VTVM to test point A2J1(TP) and remove the signal generator. Adjust the RF GAIN control over its range and note the VTVM reading.

(9) Meter reading should duplicate that noted in step (6) when adjusted from its counterclockwise to clockwise limits.

4-13. DETECTOR/AF AMPLIFIER A1A2A7. (See figures 4-17 through 4-23.)

The detector/af amplifier module contains the signal detectors and af amplifiers (A1), and the fsk converter circuits (A2). Faulty operation of this module can directly affect the operation of individual reception modes, and can prevent completely the reception of a particular mode.

a. DESCRIPTION. - This module consists of the individual am and ssb detector circuits, the headset audio amplifier, and the speaker audio amplifier. In addition, it contains the fsk converter circuit for detection of two-tone teletype-writer signals.

(1) DETECTOR-AMPLIFIER (A1). - Two detector circuits are employed: one for detection of am signals, the other for detection of cw and ssb signals. After detection, the signal is amplified by separate headset and loudspeaker amplifiers. Audio output is available for monitoring purposes at the panel mounted speaker, and at the HEADSET jack (A1A1J2) on the receiver panel.

(a) DETECTOR CIRCUITS. (See figure 4-17.) - When the receiver MODE switch is at the AM position, the am detector circuit using diode CR1 is employed. A 5 mc signal from the second i-f/agc amplifier module (A1A2A6) is

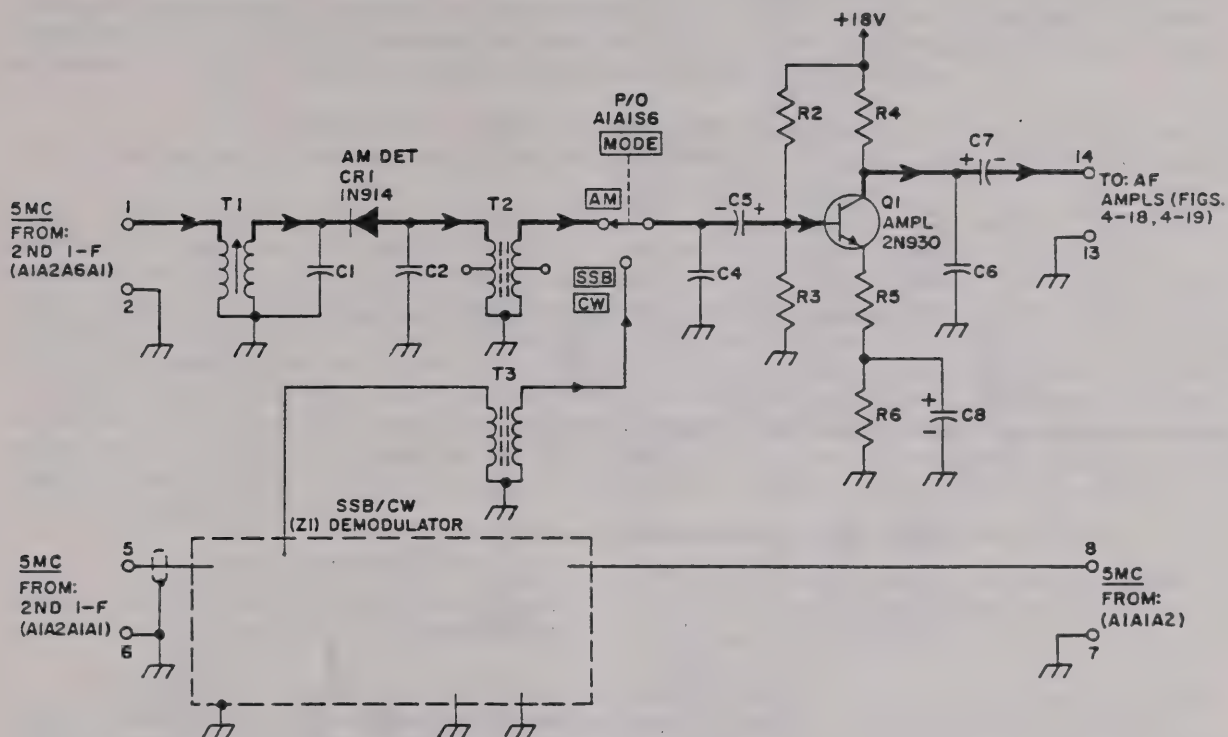


Figure 4-17. Detector/AF Amplifier A1A2A7; Detector Circuits (p/o A1), Simplified Schematic Diagram

applied to CR1 via transformer T1, the primary of T2 serving as the diode load. The detected signal is amplified by Q1 prior to amplification by the headset and speaker amplifiers in following circuits.

For the other MODE switch positions, product detector Z1 supplies a detected signal through transformer T3 to amplifier Q1. Z1 functions as a balanced demodulator to combine the 5 mc signal with the 5 mc bfo frequency from the bfo module (A1A1A2). For cw reception, the bfo frequency can be adjusted by the BFO ± 3 KC panel control; for ssb reception the bfo frequency is a fixed 5 mc frequency injection.

(b) HEADSET AMPLIFIER. (See figure 4-18.) - The headset amplifier provides audio amplification for the operation of a headset or other terminal equipment connected to the HEADSET jack.

An af signal from the detector circuits goes to amplifier Q2 through the PHONE LEVEL control (A1A1R3). Output from Q2 is applied to the base of Q3 via coupling capacitor C13. Diodes CR2, CR3, and CR4 replace the conventional bias resistors to provide a temperature compensated bias for Q3. Output from Q3 drives the complementary amplifier Q4 and Q5 which employs both an NPN and PNP type transistor, and functions as a direct-coupled, push-pull amplifier. Capacitors C17 and C27 couple the amplifier output to the HEADPHONES jack via output transformer A1A2A8T1 and also block the dc supply voltage from appearing



at these terminals. Diodes CR5 and CR6 provide operating bias and temperature compensation to obtain a stable operation at low signal levels. Resistor R16 and capacitor C15 form a degenerative feedback loop from the amplifier output to the emitter of Q2 to stabilize amplifier gain and reduce distortion.

(c) **SPEAKER AMPLIFIER.** (See figure 4-19.) - The speaker amplifier provides audio amplification for the operation of the panel mounted speaker.

An af signal from the detector circuits is amplified by Q6 and Q7, after passing through the **SPEAKER LEVEL** control (A1A1R2), to drive the direct-coupled, push-pull complementary amplifier Q8 and Q9. Diodes CR8, CR9, and CR10 supply a temperature compensated bias for amplifier operation. Q8 and Q9, in turn, drive the Class B output amplifier Q1 and Q2 (p/o module A1A2A7). Diode CR11 supplies the temperature compensated bias for amplifier operation. Capacitor C26 couples the amplifier output to output transformer T4. Resistor R33 and capacitor C25 limit the amplifier high-frequency response to reduce high-frequency noise at the speaker. A switch (S1, p/o A1A1R2) mounted on the **SPEAKER LEVEL** control disables the speaker amplifier when the control is at OFF by opening the +18 volt supply circuit.

(2) **FSK CONVERTER (A2).** - The fsk converter circuit demodulates audio frequency-shift teletype signals (1575 to 2425 cps) appearing as a two-tone modulation on the 5 mc (i-f) frequency at the converter input.

Detection of audio fsk signals is performed at 5 mc by an rf phase detector circuit employing high-Q crystal phase-discriminator circuits, rather than at audio frequencies using af filters. Converter output is in the form of a switching function, using transistors which require the application of an external signal-loop potential to operate. This potential is supplied by the external teletype equipment connected to the receiver. The fsk converter circuit consists of an amplifier-limiter circuit, a phase detector and discriminator circuit, and the output switching circuit. The **TELETYPE** terminals on the receiver panel provide the external connection to the output switching circuit when the **TELETYPE MODE** switch is in the **EXT BAT** position; in the **INT BAT** position, the output switching circuit drives the **TTY** power supply (A1A3Z1).

(a) **AMPLIFIER-LIMITER.** (See figure 4-20.) - The amplifier-limiter circuit consists of amplifier stages Q1 through Q4, and the diode limiter CR1, CR2. A 5 mc signal from the second i-f amplifier (A1) module (p/o A1A2A6), goes to the base of Q1 via input transformer T1. L2 and C6 form a 5 mc tuned circuit at the collector of Q1, and the stage output is coupled to Q2 through capacitor C7. Amplifier Q2 is similar to amplifier Q1 with L4 and C10 forming the tuned circuit. Resistors R3 and R10, respectively, damp the tuned circuits. Amplifier Q3 applies the 5 mc signal through coupling capacitor C14 to the diode limiting circuit. CR1 and CR2 remove unwanted amplitude modulation and noise from the signal. The limited or clipped signal is amplified by Q4 and applied to the phase detector circuit which follows through capacitor C19. L5 and C17 form the tuned circuit at the collector of Q4, resistor R19 performing the damping function.

(b) **PHASE DETECTOR.** (See figure 4-21.) - The phase detector circuit converts the audio fsk signals into a differential dc output voltage. The circuit consists of phase inverter Q5; phase-shift network C22, C23, C24, C25, and R31; two crystal phase-discriminator circuits, one for each sideband, employing transformers T2 and T3, and crystals Y1 and Y2; and an additional amplifier-limiter circuit using Q6 and Q7, with diode limiter CR5 and CR6.

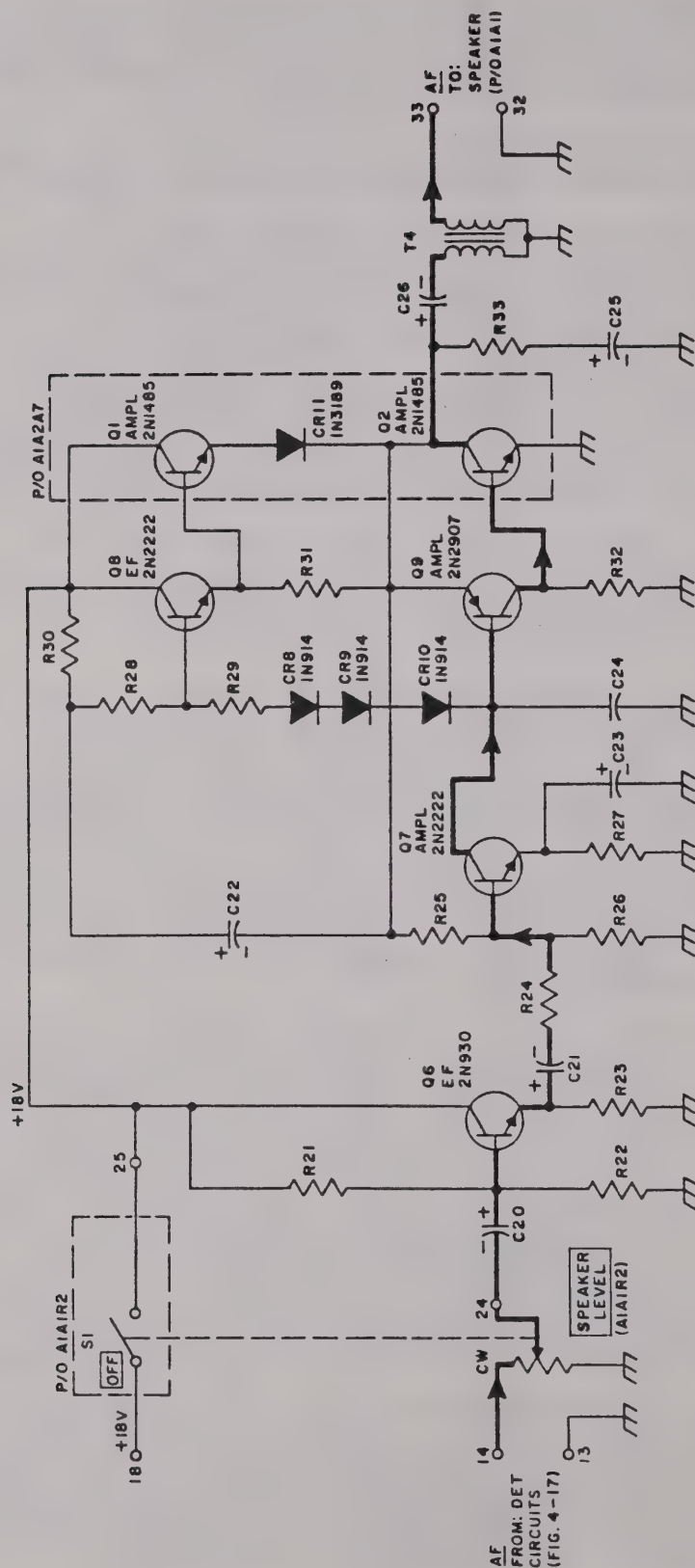


Figure 4-19. Detector/AF Amplifier ALA2A7; Speaker Amplifier (p/o A1),
Simplified Schematic Diagram

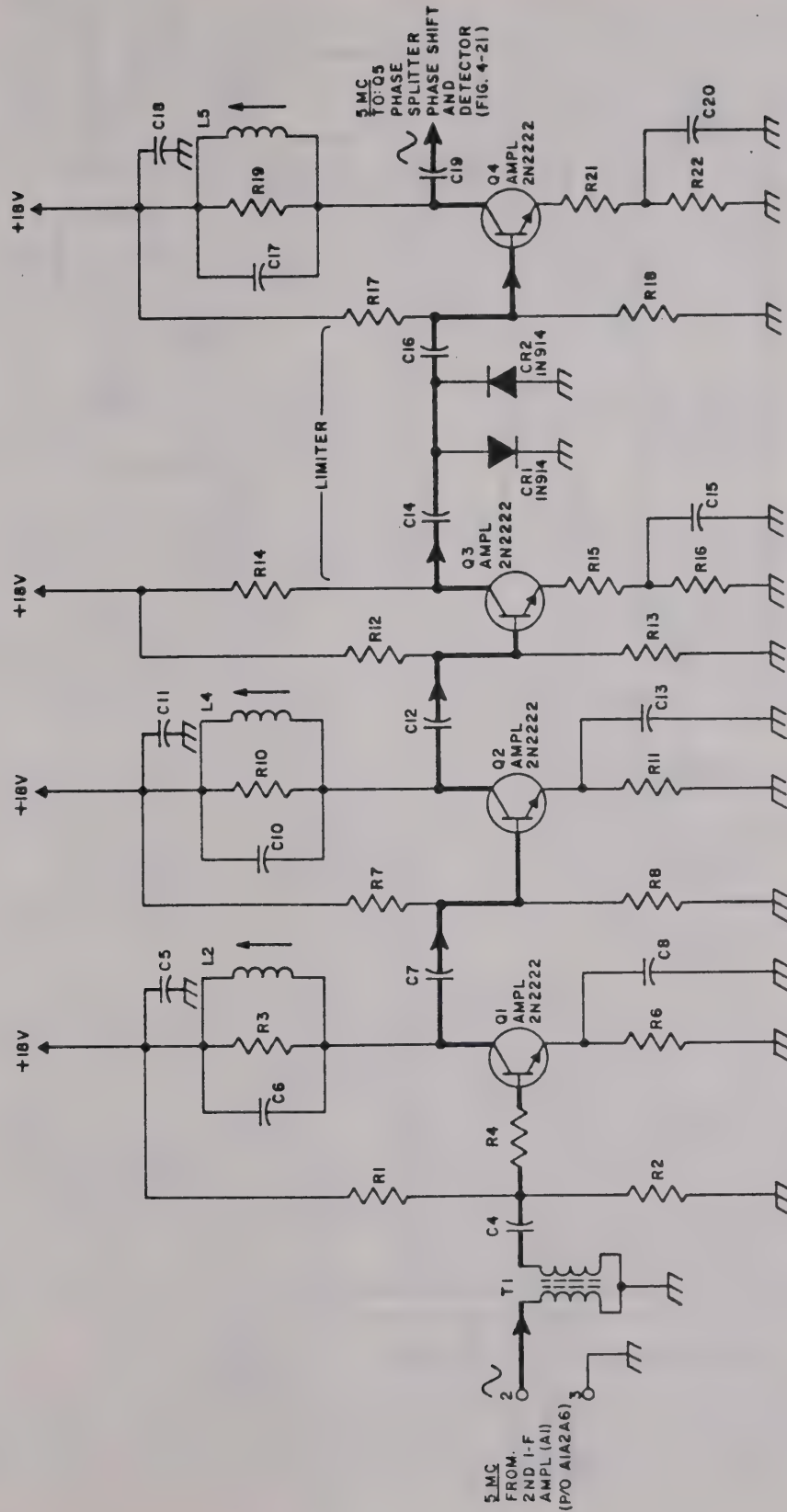


Figure 4-20. Detector/AF Amplifier ALA2A7; Amplifier-Limiter (p/o A2),
Simplified Schematic Diagram

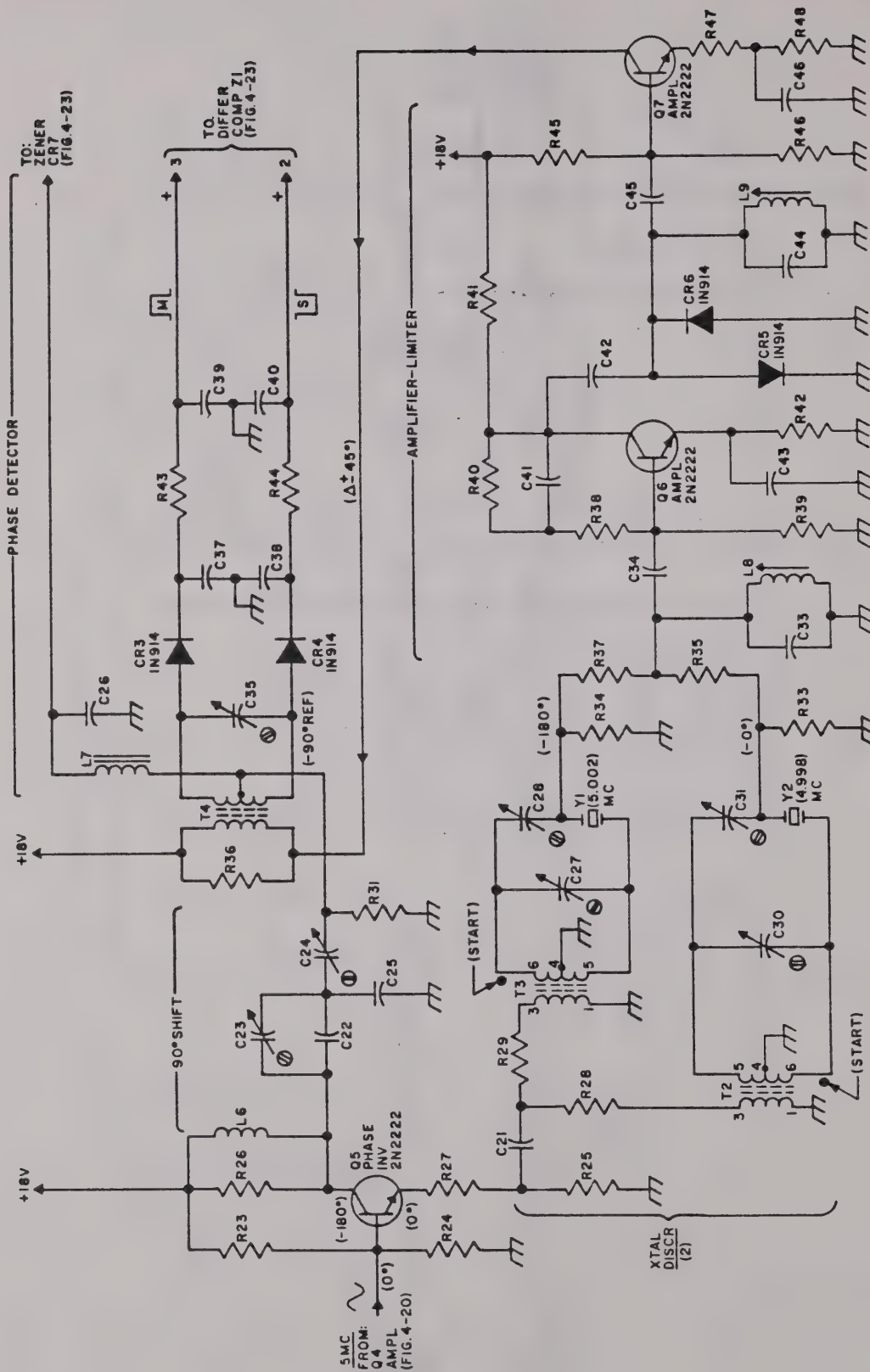


Figure 4-21. Detector/AF Amplifier A1A2A7; Phase Detector (p/o A2), Simplified Schematic Diagram

Phase inverter Q5 receives the clipped 5 mc signal from the amplifier-limiter circuit previously described, and supplies two output signals having a 180 degree phase difference. From the collector Q5, a reference signal is supplied to the phase detector CR3 and CR4 via a phase-shift network consisting of C22, C23, C24, C25, and R31. Variable capacitors C23 and C24 provide a phase adjustment. The collector tuned circuit L6, with damping resistor R26, is actually tuned by the network through resistor R31 to ground. The "leading" capacitor current through R31 supplies a voltage drop, shifted from the reference signal source by +90 degrees, which is applied to the tapped secondary of transformer T4. Zener diode CR7, located in the switching circuit section, supplies a fixed dc voltage to the tapped winding via the decoupling network of L7 and C26. This voltage combines with the R31 signal to obtain an "above ground" reference level for detector operation.

The other output signal, from the emitter of Q5, is applied to the two crystal phase-discriminator circuits at the primaries of transformers T2 and T3. Capacitor C21 blocks the dc emitter current from the transformer windings and resistors R28 and R29 provide circuit isolation.

The individual usb and lsb crystal phase-discriminator circuits are identical except for the crystal frequencies employed. Selecting the usb discriminator circuit as an example, the secondary of transformer T3 is tuned to 5.002 mc by capacitors C27, C28, and C29 in series with crystal Y1. Discriminator output at resistor R34 is zero for a signal at the crystal frequency, and appears when the frequency changes. A signal frequency shift of ± 425 cycles, occurring when the 5.002 mc two-tone fsk modulation appears at 1575 and 2425 cycles, produces a phase detector output which shifts ± 45 degrees in relation to the input signals phase.

Discriminator output, from either the usb or the lsb circuit, is applied to the amplifier-limiter circuit of Q6 and Q7, via isolation resistors R35 and R37. Tuned circuit L8 and C33 provides a high-impedance at the Q6 input, and the diode limiters CR5 and CR6 remove amplitude modulation components contributed by the discriminator circuits. Tuned circuit L9 and C44 provides a high-impedance output termination for the limiting diodes and the clipped signal is amplified by Q7. Output from Q7 is applied to the primary of transformer T4 at the phase detector.

Phase detector CR3 and CR4 produces a differential dc output voltage which is proportional to the phase difference between the two input signals, the reference signal contributed by the +90 degree phase-shift network and the discriminator signal supplied from either the usb or the lsb phase-discriminator circuits. When these input signals are precisely 90 degrees apart in phase, the phase detector output is effectively zero. Although an output voltage is present at diodes CR3 and CR4, the diode currents are of equal amplitude but opposite phase and the algebraic sum is zero. The phase detector output is a balanced dc signal voltage without a ground return circuit at this point. When the discriminator input signal shifts ± 45 degrees with respect to the reference signal input, the phase detector output becomes unbalanced producing a signal pulse for each swing of the signal phase. Resistors R43, and R44, and capacitors C37 through C40 form a low-pass filter to reduce high frequency noise components present in the circuit.

(c) PHASE DETECTOR OPERATION. (See figure 4-22.) - To simplify a description of phase detector operation, it is assumed that the receiver is tuned to an audio two-toned fsk signal employing the upper sideband. Consequently, the 4.998 mc signal at the base of phase inverter Q5 represents the center

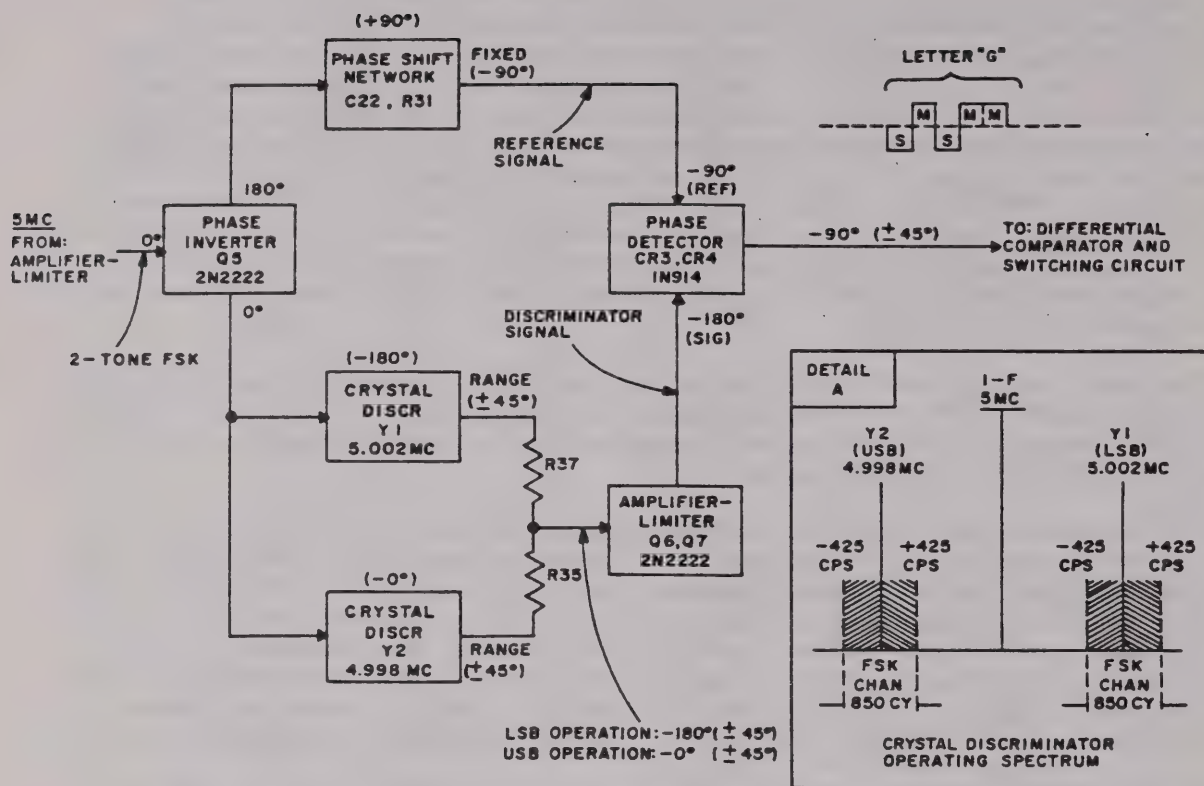


Figure 4-22. Detector/AF Amplifier A1A2A7; Phase Detector (p/o A2),
Functional Block Diagram

frequency of the usb fsk channel, and the usb crystal phase-discriminator is employed. A lower sideband transmission would use the 5.002 mc lsb phase discriminator circuit. Otherwise, circuit operation is identical for either sideband. Figure 4-22, a functional block diagram of the phase detector circuit, identifies the various signal paths and their phase relation during reception of the fsk signal.

The input signal at the base of phase inverter Q5 appears at the collector with a phase shift of -180 degrees, referred to the input. Phase shift network C22, C23, C24, C25, and R31 provides a $+90$ degree phase shift and the reference signal at T4 of the phase detector has a phase relation of -90 degrees to the input signal (-180° and $+90^\circ = -90^\circ$). The emitter output from Q5 is in phase with the base signal. Therefore, the secondary winding of T3 at the 5.002 mc phase discriminator is reverse connected to obtain a -180 degree phase shift at the discriminator output, with reference to the Q5 base signal. Consequently, the discriminator output applied to transformer T4, via amplifier-limiter circuit Q6 and Q7, is -180 degrees out-of-phase. The two phase-detector input signals now have the required 90 degree phase relation, prior to keying of the received signal, for phase detector operation (-180° and $-90^\circ = +90^\circ$), a condition of zero phase-detector output.

When the received lsb fsk signal is two-tone modulated, the 1575 and 2425 cycle modulation generates ± 425 cycle sidebands at the 5.002 mc center frequency

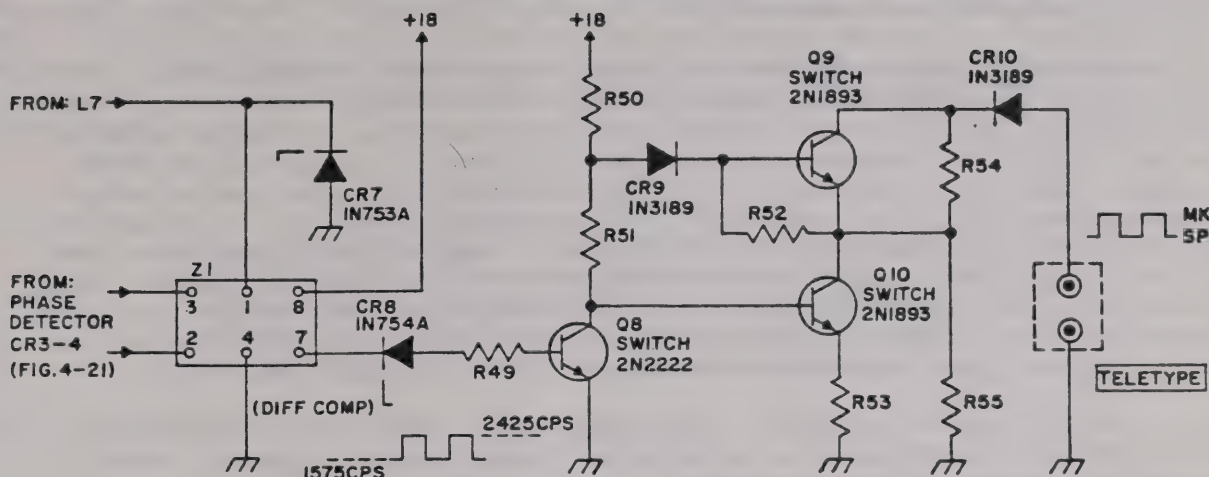


Figure 4-23. Detector/AF Amplifier A1A2A7; Switching Circuit (p/o A2), Simplified Schematic Diagram

for a total channel width of 850 cycles. These sidebands appear at the phase detector input as the reference and discriminator signals. The reference signal has a fixed -90 degree relation to the Q5 input signal, but the discriminator signal-phase shifts ± 45 degrees in response to the two-tone signal keying. An unbalanced output occurs at the phase detector, duplicating the two-tone keying. This output is applied to a binary (IC) differential comparator (Z1) in the switching circuit section to obtain the detected "mark" and "space" teletype code contained in the received signal.

When the received fsk signal employs a usb transmission, the channel center frequency is 4.998 mc and the usb crystal phase-discriminator is used. Note that the transformer T2 windings are not reversed. Output from the Y2 discriminator, in the absence of a two-tone signal modulation, is in phase with the Q5 base signal. The 90 degree phase relation between the two phase detector input signals is fulfilled as a function of the $+90$ degree phase shift network (-90° and $0^\circ = -90^\circ$). The 180 degree shift from $+90$ degrees to -90 degrees is compatible with the shift from upper to lower sideband reception, and phase detector operation continues as before.

(d) SWITCHING CIRCUIT. (See figure 4-23.) - The fsk converter switching circuit contains the differential comparator Z1, and the fsk switch circuit employing Q8, Q9, and Q10. An external collector potential, supplied by the external teletype equipment or TTY power supply, depending on battery mode, is necessary for the operation of switch stages Q9 and Q10. This potential required can vary from 26.0 to 105.0 volts dc, and the switching current from 5.0 to 100.0 milliamperes dc.

The differential dc output signal from the phase detector is applied to a high-speed differential comparator Z1 for conversion to a conventional "mark" and "space" binary teletype-code signal. The integrated circuit contained in Z1 operates in saturation modes to process the dc differential signal and obtain clean, square-wave, binary-type output signal, devoid of reception noise components and ambiguity. Zener diode CR7 supplies a dc above-ground operating level for the

comparator output signal, and also provides a similar function in the phase detector circuit previously described.

Dc switch Q8 triggers the fsk switching circuit formed by Q9 and Q10 in series. Zener diode CR8 at the base of Q8 sets the threshold of operation when the TELETYPE MODE switch is in the EXT BAT position. A "mark" pulse at the output TELETYPE terminals appears when Q9 and Q10, in series, become saturated. This occurs when Q8 is cut off by the application of a "space" pulse from comparator Z1. The comparator input terminals 2 and 3 are connected to compensate for this apparent reverse in operation, and a "mark" appears at the output of Q9 and Q10 whenever a "mark" occurs in the received fsk signal. Diode CR10 functions as a gate to protect the switching circuit in the event of a polarity reversal occurring at the TELETYPE output terminals. Diode CR9 assures the presence of bias at the base of Q9 during the period when Q8 is saturated.

b. PRELIMINARY CHECK. (See figure 4-56.) - With power off, make a preliminary check of the detector/af amplifier module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in module in its socket.
- (2) Cable connections (if any) attached to module.
- (3) Operation of the SPEAKER LEVEL and PHONE LEVEL controls.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D, Multimeter AN/USM-116, and Frequency Counter 5245L, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the MODE, SPEAKER LEVEL, and PHONE LEVEL controls as directed.

e. TEST DATA. (See figures 5-30, 5-31, and 5-32.) - Trouble shooting the detector/af amplifier module consists of checking the detector and af amplifiers (A1), and the fsk converter (A2) circuits, using a test signal supplied by the signal generator. Perform the following:

(1) Connect signal generator to test point A1J1(TP) at the second i-f/agc amplifier module (A1A2A6). Adjust generator for a 5.0 mc, 100 millivolt, test signal, modulated 30 per cent at 400 cycles.

(2) Rotate the SPEAKER LEVEL control clockwise and note the presence of the 400 cycle test signal modulation at the panel speaker. Return control to the OFF position.

(3) Connect a headset to the PHONES jack and rotate the PHONE LEVEL control clockwise, noting the presence of the 400 cycle test signal in the headset. Return control to a fully counterclockwise position.

(4) Set the MODE switch at CW, and repeat steps (2) and (3). Note the double audio tone produced by the bfo combined with the test signal modulation.

(5) Place the MODE switch at FSK. Connect the multimeter to the front panel TELETYPE terminals and select the low-ohm range. Remove the 400-cycle

modulation from the test signal and slowly tune the generator above 5.0 mc to simulate reception of a two-tone fsk signal. Note the change in the ohmmeter reading. A "mark" element will be simulated at a generator frequency of 5.002425 mc and cause a low ohmmeter reading. A "space" element, at a generator frequency of 5.001575 mc, will produce a relatively high ohmmeter reading in the vicinity of 80,000 ohms.

Note

For the above test, the ohmmeter lead at the positive (plus) TELETYPE terminal must be the positive lead of the internal ohmmeter battery. This battery will supply the external signal-line potential to the fsk converter switching-circuit for test purposes.

4-14. BFO MODULE A1A1A2. (See figure 4-24.)

The bfo (beat-frequency-oscillator) module, located on the front panel section (A1A1), contains the oscillator (A2) and the buffer amplifier (A1) circuits. Faulty operation of this module will affect and can prevent completely the reception of cw and ssb signals.

a. DESCRIPTION. - The bfo circuit containing A1Q1 and A2Q1 performs two distinct operating functions, determined by the position of switch S1 (large knob) on the concentric BFO ± 3 KC control. When S1 is at the VAR position A2Q1 functions as an oscillator, generating a 5 mc frequency which is tuned ± 3 kc by tuning capacitor A1A1A1C1, adjusted by the small control knob. Oscillator output is amplified by A1Q1 and applied to the detector/af amplifier module (A1A2A7). When S1 is at the FIXED position, both A1Q1 and A2Q1 function as amplifiers for the 5 mc frequency supplied from the digital #3 card (A1A3A1A6).

(1) OSCILLATOR (A2). - Oscillator Q1, a modified Colpitts, oscillates when the base is grounded via capacitor C9 and CR2 by setting switch S1 at VAR. This also effectively opens the 5 mc frequency circuit to the base through R2, CR1, and C2. Inductor L2 and capacitors C4 and C5, in series, form the oscillator tank circuit. Capacitor C7 and the oscillator tuning capacitor A1A1A1C1, in series, shunt the tank circuit through by-pass capacitor C3 to ground. Oscillator output is coupled to the amplifier A1Q1 through coupling capacitor C8. When switch S1 is at the FIXED position, the base is not grounded through C1 and oscillation ceases, diode CR1 is switched on via R1 providing the required circuitry to ground for the 5 mc from the synthesizer. Now, Q1 functions as an amplifier stage to amplify the fixed 5 mc frequency.

(2) AMPLIFIER (A1). - The 5 mc frequency from oscillator A1Q1, whether locally derived or supplied by the digital #3 card (A1A3A1A6), is amplified by Q1. The primary of output transformer T1 is tuned to 5 mc by capacitor C4, and the transformer secondary supplies the amplified 5 mc frequency to the detector/af amplifier module (A1A2A7).

Note

When the receiver MODE switch is at SSB, the switch S1 circuit is grounded to assure use of a fixed 5 mc injection frequency for this mode of operation.

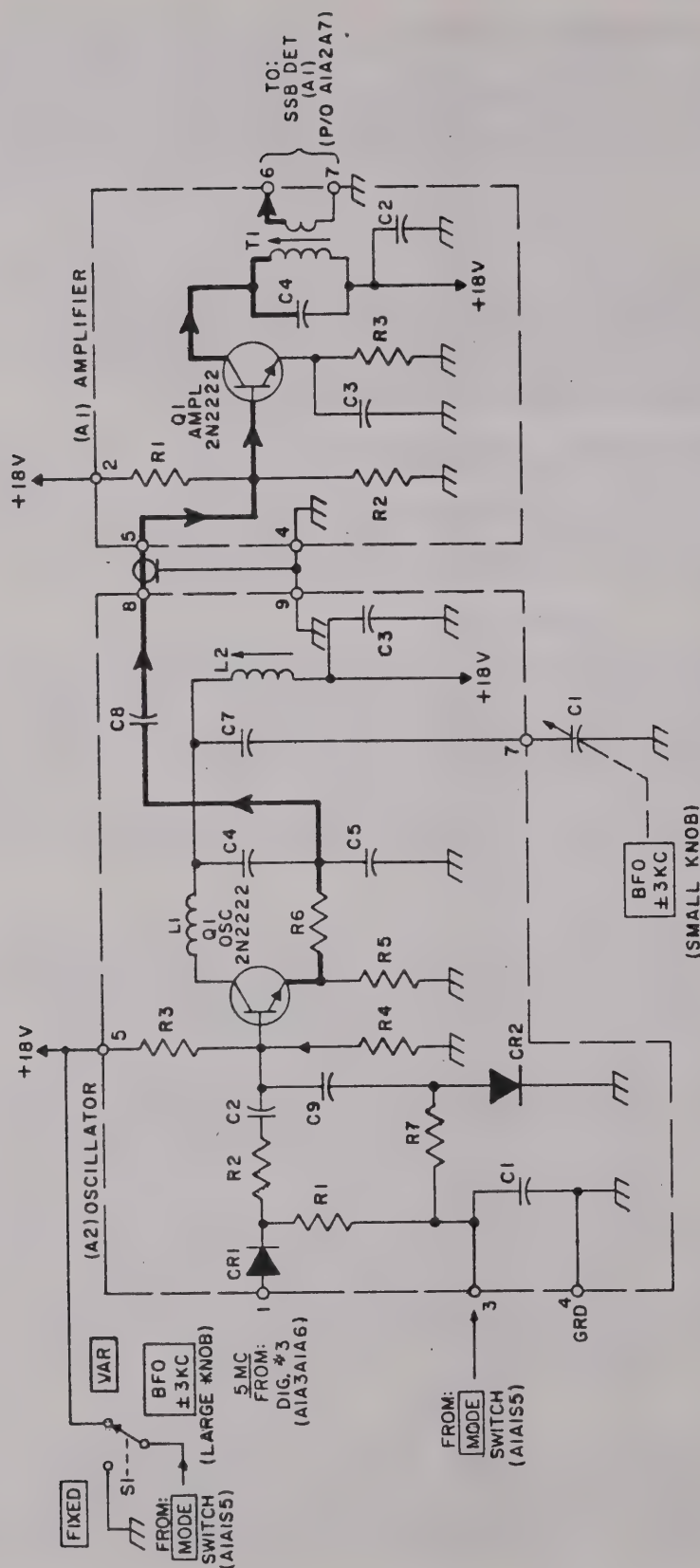


Figure 4-24. BFO A1A1A2, Simplified Schematic Diagram

b. PRELIMINARY CHECK. (See figure 4-57.) - With power off, make a preliminary check of the bfo module before trouble shooting, with emphasis on the following:

- (1) Cable connections (if any) attached to module.
- (2) Operation of the BFO ± 3 KC control.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedures, set the MODE and BFO ± 3 KC controls as directed.

e. TEST DATA. (See figures 5-11, 5-12, and 5-13.) - Trouble shooting the bfo circuit consists of checking the separate variable-oscillator and amplifier functions using a test signal supplied by the signal generator.

(1) Connect signal generator to test point A1J3(TP) at the second i-f/agg amplifier module (A1A2A6). Adjust the generator for a 5 mc, 30 mv, unmodulated test signal.

(2) Set the MODE switch at SSB. Slowly tune the generator in the vicinity of 5 mc and note the beat-note at the speaker, produced by a combination of the test signal and the fixed 5 mc third (receiver) injection frequency.

(3) Set the BFO ± 3 KC control large knob at VAR, and adjust the small knob. This adjustment should have no effect on the beat-note.

(4) Set the MODE switch at CW. Now, adjust the small control knob. A 3000 cycle (approximately) beat-note should occur at the speaker for each extreme position of the small control knob. Zero-beat should occur at a central position.

4-15. FREQUENCY STANDARD A1A1A1.

The 3 mc frequency standard module, located on the front panel section (A1A1), contains a sealed, temperature-compensated, solid state oscillator circuit. Faulty operation of this module will affect the receiver tuning accuracy and can prevent reception completely.

a. DESCRIPTION. - The frequency standard module requires a +18 volt dc supply voltage for operation and the total operating power is approximately 100 milliwatts. Standard output is 3 mc and stability is 1 part in 10^7 per day or 5 parts in 10^7 per 30 days. The minimum output level is 1 milliwatt across 50 ohms.

b. PRELIMINARY CHECK. (See figure 5-3.) - With power off, make a preliminary check of the frequency standard module before trouble shooting, with emphasis on the following:

- (1) Soldered and cable connections at the module.

c. TEST EQUIPMENT. - Use VTVM ME-286/U, or equivalent. No special tools are required.

d. TEST DATA. (See figure 5-3.) - Trouble shooting the frequency standard module consists of measuring the 3 mc output level, at a convenient test point.

(1) Connect the VTVM to test point J1(TP) at the mixer/multiplier module (A1A3A2).

(2) The measured 3 mc level should be 20 millivolts rms, or more.

4-16. VFO MODULE A1A1A3. (See figure 4-25.)

The 3 mc vfo (variable-frequency-oscillator) located on the front panel section (A1A1), contains the oscillator (A1), and the switching circuit and frequency vernier tuning-capacitor. Faulty operation of this module will prevent completely the continuous tuning of the receiver. Incremental receiver tuning can also be affected.

a. DESCRIPTION. - The vfo or frequency vernier tuning-circuit contains the 3.0 mc crystal oscillator Q1, controlled by the dual (concentric) FREQ VERNIER ± 150 CPS control. When S1 and S2 (large knob) are at FIXED, the +18 volt supply voltage is removed from the collector of Q1, and a fixed 3.0 mc frequency from the frequency standard module (A1A1A1) is applied to the mixer/multiplier module

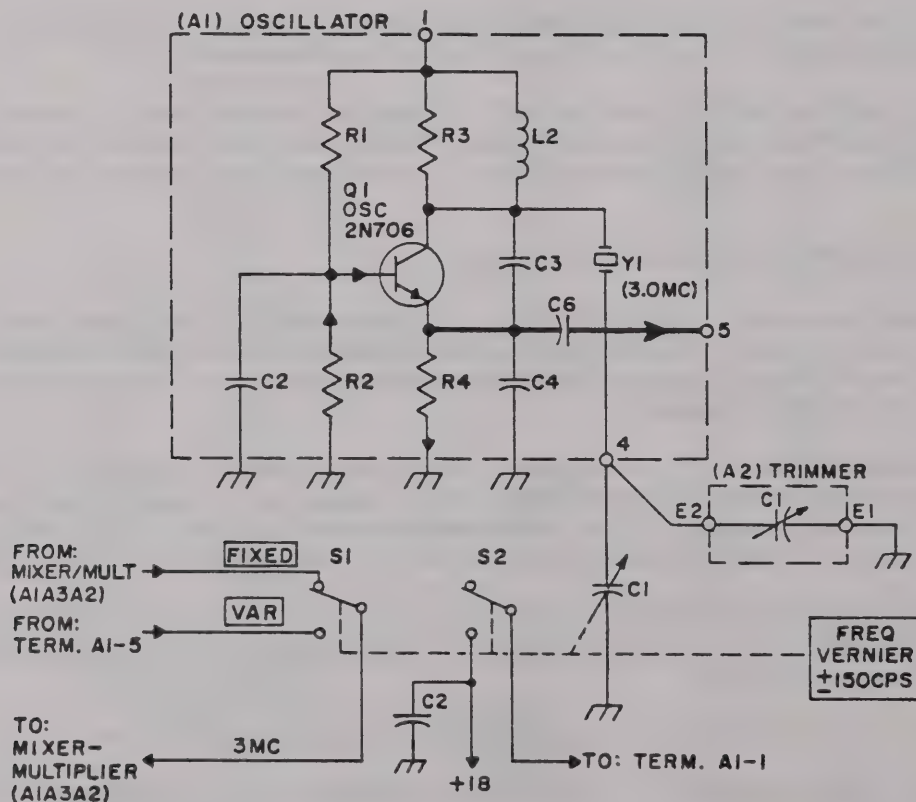


Figure 4-25. VFO A1A1A3, Simplified Schematic Diagram

(AlA3A2), via switch S1. When S1 and S2 are at VAR, operating power is supplied to Q1 and an adjustable 3.0 mc, ± 150 cycles, frequency is substituted for the frequency standard signal. The small control knob controls variable capacitor A2C1 to tune the oscillator.

Oscillator Q1 is arranged in a modified Colpitts circuit with the 3.0 mc crystal Y1 and the series tuning-capacitor A2C1 in shunt to tank capacitors C3 and C4. The Q1 base is effectively returned to ground via capacitor C2. Oscillator output is obtained from the Q1 emitter circuit via C6. Although Q1 is a crystal controlled oscillator, the output frequency can be varied within narrow limits by adjusting tuning capacitor C1 to "pull" the crystal frequency.

b. PRELIMINARY CHECK. (See figure 4-25.) - With power off, make a preliminary check of the vfo module before trouble shooting, with emphasis on the following:

- (1) Cable connections (if any) to the module.
- (2) Operation of the FREQ VERNIER ± 150 CPS control knobs.

c. TEST EQUIPMENT. - Use VTVM ME-286/U and Electronic Counter AN/USM-26, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the FREQ VERNIER ± 150 CPS control as directed.

e. TEST DATA. (See figures 5-8, 5-9, and 5-10.) - Trouble shooting the vfo circuit consists of checking the oscillator output level and measuring the range of frequency control.

(1) Connect VTVM to the vfo module OUTPUT terminal. Set the FREQ VERNIER ± 150 CPS (large) knob at VAR. Vfo output level should be 0.6 volt rms, or greater.

(2) Connect the frequency counter to the module OUTPUT terminal. Set the (small) control knob fully clockwise, and then fully counterclockwise. The control range should be ± 150 cycles or more.

4-17. SYNTHESIZER CIRCUITS AlA3A1. (See figure 4-26.)

The all solid-state synthesizer circuits employ digital circuit techniques to supply a large number of precise injection frequencies to the various receiver circuits. Although the receiver first injection frequency is supplied by the vhf oscillator A1 (p/o module AlA2A2), the oscillator is phase-locked by an 82 to 110 mc range of frequencies developed by the synthesizer. The receiver 117 mc second injection frequency, applied to the second mixer stage (p/o module AlA2A3), and the third injection frequency of 5 mc supplied to the ssb detector stage (p/o module AlA2A7) are also provided by the synthesizer circuits. In addition, the synthesizer supplies a 12.5 kc "sync" pulse to the solid-state regulating circuits in the power supply module (AlA3PS1). Because these synthesized frequencies are derived from the 3.0 mc frequency standard module (AlA1A1), they exhibit the same degree of accuracy and stability as the standard frequency.

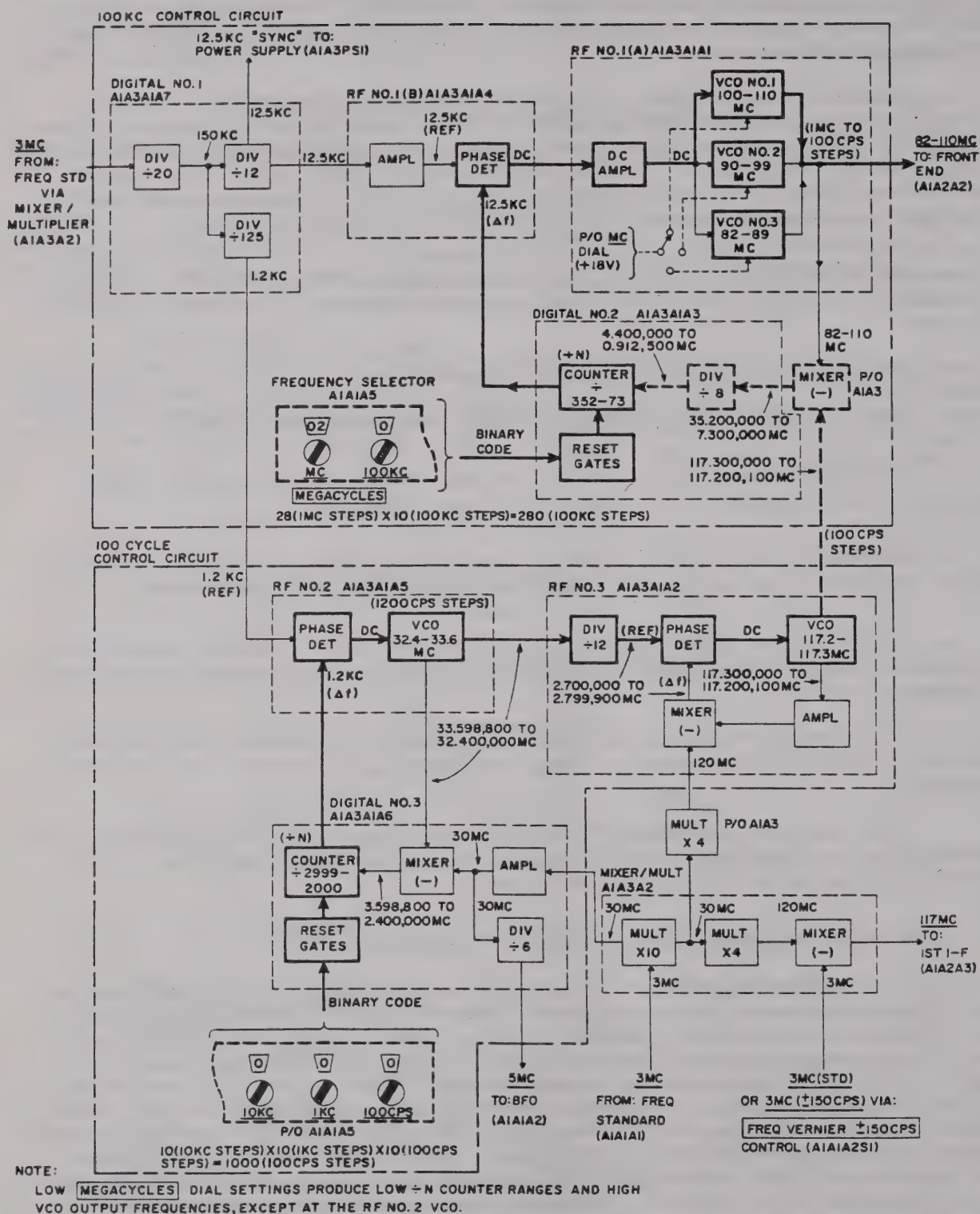


Figure 4-26. Synthesizer A1A3A1, Simplified Block Diagram

The following paragraphs contain a basic description of synthesizer circuit operation following the synthesizer simplified block diagram shown in figure 4-26. Although the circuits are more complex than the block diagram indicates, their basic functions are accurately portrayed. Detailed descriptions of the individual synthesizer cards with their operating characteristics are provided immediately following this basic circuit description.

a. SYNTHESIZER OUTPUT. - The 82 to 110 mc synthesizer output frequency range is generated, in three steps, by the three voltage controlled oscillators (vco) in the rf #1(A) card (A1A3A1A1). The vco frequency is phase-locked to a 12.5 kc reference frequency, supplied by the digital #1(B) card (A1A3A1A7A2) by a phase detector located in the rf #1(B) card (A1A3A1A4). Synthesizer frequencies within this range are supplied in precise 100-cycle increments when the MEGACYCLES tuning dials (module A1A1A5) are set in 100-cycle steps from 02.0000 to 29.9999 mc.

The 117 mc synthesized frequency is derived from the 3.0 mc frequency standard module (A1A1A1) by the mixer/multiplier module (A1A3A2), or from the vfo module (A1A1A3), depending upon the switch setting at the FREQ VERNIER ± 150 CPS control at the receiver panel. When the control switch (large knob) is at FIXED, a fixed 117 mc frequency is supplied. With the switch at VAR, the 117 mc frequency can be adjusted ± 150 cycles for continuous receiver tuning of each of 100-cycle increment.

The 5.0 mc synthesized frequency is obtained from the 30.0 mc output at mixer/multiplier module (A1A3A2) via the divide-by-six frequency divider in the digital #3 card (A1A3A1A6), and therefore is derived from the 3.0 mc frequency standard.

The 12.5 kc "sync" pulse for power supply card (A1A3PS1) is obtained from the frequency dividing circuits in the digital #1(B) card (A1A3A1A7A2), and is also derived from the 3.0 mc frequency standard. The "sync" pulse is used to control solid-state regulating circuits in the power supply 5.0 volt and 18.0 volt dc supply circuits.

b. SYNTHESIZER COMPONENTS. - The synthesizer circuits, in addition to employing conventional frequency dividing, multiplying, and mixing circuits, contain a number of vhf voltage-controlled oscillators (vco), phase-locked loop circuits, and digital-type pulse counting circuits functioning as variable frequency-dividers, to synthesize literally thousands of frequencies from the frequency standard source. Digital circuits techniques are employed using solid-state integrated circuits (IC) to obtain a small, light weight, highly reliable frequency synthesizer.

(1) VOLTAGE-CONTROLLED OSCILLATORS. - Voltage-controlled oscillators are used in the rf #1(A) card (A1A3A1A1), the rf #2 card (A1A3A1A5), and in the rf #3 card (A1A3A1A2). Varactor tuning is employed and the vco output frequency is determined by a dc varactor control voltage. Although the oscillators operate in the vhf band, the controlled range is limited to a nominal 10 per cent of the operating frequency and oscillator linearity is maintained. Dc varactor control voltages are supplied by a phase detector, located with the oscillator or in an adjoining circuit. The oscillators are tuned over their frequency range by a phase-locked loop circuit containing the phase detector, and locked with crystal accuracy to a reference frequency derived from the 3.0 mc frequency standard.

(2) PHASE-LOCKED LOOP. - A phase-locked loop circuit maintaining a digital-type phase detector supplies the vco control voltage. The phase detector for the three vco circuits in the rf #1(A) card (A1A3A1A1) is located in the rf #1(B) card (A1A3A1A4), and the remainder of the phase-locked loop is located in the digital #2 card (A1A3A1A3). Card rf #3 (A1A3A1A2) contains a fourth vco circuit and its associated phase-locked loop circuit. The fifth and last vco with its phase detector is contained in the rf #2 card (A1A3A5), and the remainder of the phase-locked loop circuit in the digital #3 card (A1A3A1A6). Note that the digital #2 and digital #3 cards contain a digital counter ($\div N$) as a part of the phase-locked loop circuit.

When a vco is in operation, its output frequency is sampled by the phase-locked loop, processed, and applied to the vco phase detector. When the processed sample frequency coincides with the phase detector reference frequency, the vco is "locked" at that operating frequency. The phase-locked loop circuits in the rf #1(B) and the rf #2 cards are not as simple as the block diagram of figure 4-26 would indicate. Actually, a ramp generator is included to quickly sweep the vco through its frequency range, and a frequency discriminator circuit performs a vco coarse-tuning function. The complete circuits are described in the individual module descriptions. For the purpose of a basic description, it can be assumed that the phase detector circuit performs all the necessary vco control functions.

(3) VARIABLE FREQUENCY DIVIDERS ($\div N$). - A divide-by-N digital-type pulse counter is used as a variable-rate frequency divider in the digital #2 card (A1A3A1A3) and the digital #3 card (A1A3A1A6), which are the phase-locked loop circuits for the vco's in the rf #1(A) and the rf #2 cards. The counters are arranged to count down, in decimal digits, with the counting length controlled by reset gates. Once a vco is "locked" by the phase-locked loop circuit, it would seem that vco operation at other frequencies is prohibited by the loop. Fortunately, the vco can be "locked" at any part of its frequency range simply by processing the loop frequency. To raise the vco locking frequency by 1 kc, the loop frequency is decreased by 1 kc, and to lower the vco locking frequency, the loop frequency is increased a like degree. In this manner, the divide-by-N counting circuits are programmed by the reset gates to "lock" the associated vco at predetermined points in its frequency range. The reset gates at each of the divide-by-N counters are controlled by a digital switching code, developed by setting the five dials on the MEGACYCLES frequency selector (A1A1A5). Consequently, the frequency generated by the vco circuits in the rf #1(A) and the rf #2 cards is controlled by the tuning dials.

c. SYNTHESIZER CONTROL. - The 82 to 110 mc synthesizer output frequency range is selected, in a series of 280,000 increments, 100 cycles apart, by setting the MEGACYCLES tuning dials in digital steps from 02.0000 to 29.9999 mc. The binary code developed by the mc and 100 kc tuning dials controls the reset gates for the divide-by-N counter in the digital #2 card (A1A3A1A3), and therefore its counting range from 352 to 73 counts. The binary code developed by the 10 kc, 1 kc, and 100 cps tuning dials controls the reset gates for the divide-by-N counter in the digital #3 card (A1A3A1A6), and therefore its counting range from 2999 to 2000 counts. In addition, the mc tuning dial selects the appropriate vco circuit in the rf #1(A) card (A1A3A1A1).

To facilitate the description of synthesizer control methods, the synthesizer circuit is separated into two functional areas. One area contains the cards under direct control of the mc and 100 kc tuning dials, and the other area contains cards

directly controlled by the 10 kc, 1 kc, and 100 cps tuning dials. The circuit division has a functional basis because the synthesizing process originating in these two areas are combined at the digital #2 card. Frequency synthesizing in 1 mc and 100 kc steps, controlled by the mc and 100 kc tuning dials, is combined with synthesizing in 10 kc, 1 kc, and 100-cycle steps, controlled by the 10 kc, 1 kc, and 100 cps tuning dials, each circuit area employing a divide-by-N counter. For simplicity, these two circuit areas are named the 100 kc control circuit, and the 100-cycle control circuit, respectively.

(1) 100 KC CONTROL CIRCUIT. - The synthesizer 100 kc control circuit consists of the mc and 100 kc MEGACYCLES tuning dials and their circuits, the digital #2 card, and the rf #1(A) and rf #1(B) cards. When the mc and 100 kc tuning dials are set, in digital steps, over their range from 02.0 to 29.9 mc, the synthesized frequency at the output of the rf #1(A) card changes from 110.0 mc to 82.1 mc in a series of 280 (100 kc) steps. The mc dial controls the output frequency in steps of 1 mc, and the 100 kc dial controls ten 100 kc increments for each setting of the mc dial. For the purpose of this description, the remaining tuning dials are set at zero (0).

When the five tuning dials are set to a signal frequency of 02.0000 mc, the synthesizer output frequency from the rf #1(A) is 110.0000 mc, the frequency difference between the signal frequency and the receiver first i-f frequency of 112 mc. This output frequency is generated by vco #1 in the rf #1(A) card. The vco is phase-locked by the phase detector in the rf #1(B) card to a 12.5 kc reference frequency supplied by the digital #1 card. A sample of the 110.0000 mc synthesized frequency is processed by the phase-locked loop circuit in the digital #2 card to obtain a 12.5 kc vco derived frequency for phase detector operation. The digital #2 mixer stage combines the 110.0000 mc sample frequency with a 117.3000 mc frequency supplied from the rf #3 card, a part of the 100-cycle control circuit, developed by setting the 10 kc, 1 kc, and 100 cps dials at zero (0). Mixer output is a 7.3000 mc difference frequency, reduced to 0.91250 mc by the divide-by-8 frequency divider. The divide-by-N counter is programmed for a count length of 73 by the mc and 100 kc dials, and functions as a divide-by-73 frequency divider to reduce the 0.91250 mc frequency to the required 12.5 kc phase-locked loop frequency.

When the five tuning dials are reset to a 29.9000 mc signal frequency, the setting limit for the mc and 100 kc dials, a synthesized 82.1000 mc frequency is produced at the rf #1(A) card output. Vco #3 generates the output frequency and is phase-locked by the rf #1(B) phase detector. This time, the digital #2 card mixer combines a 82.100 mc vco sample with the 117.3000 mc frequency from the rf #3 card to obtain a 35.2000 mc difference frequency. The divide-by-8 frequency divider reduces the frequency to 4.4000 mc and it is applied to the divide-by-N counter. With the mc and 100 kc tuning dials set at 29.9 mc, the counter is programmed for a frequency division by 352, reducing 4.4000 mc to the 12.5 kc frequency necessary to phase-lock the vco.

The divide-by-N counter in the digital #2 card can be programmed to perform a series of 280 different frequency divisions, from divide-by-352 to divide-by-73. Consequently, 280 different vco frequencies from the three vco's in the rf #1(A) card can be converted to 12.5 kc to lock the vco. In this manner, the 280 synthesized frequencies selected by the mc and 100 kc tuning dials are locked to the 12.5 kc reference frequency derived from the 3.0 mc frequency standard.

(2) 100-CYCLE CONTROL CIRCUIT. - The synthesizer 100-cycle control circuit consists of the 10 kc, 1 kc, and 100 cps MEGACYCLES tuning dials and their switch circuits, the digital #3 card, and the rf #2 and rf #3 cards. When these three tuning dials are set over their range from 000 to 999, in digital steps, the synthesized output from the rf #1(A) card is changed in steps of 10 kc, 1 kc, and 100 cycles, in a series of 1000 (100 cps) steps. These frequency steps are combined with the 280 (100 kc) steps contributed by the 100 kc control circuit at the digital #2 card for a total of 280,000 selectable, synthesizer output frequencies.

Two separate vco circuits, located in the rf #2 and rf #3 cards, are employed to supply synthesized frequencies from 117.300,000 mc to 117.200,100 mc to the digital #2 mixer stage. This range of frequencies contains the tuning information, in 10 kc, 1 kc, and 100-cycle steps, contributed by setting the three 100-cycle circuit tuning dials.

The rf #2 card vco has an operating range from 33.598,800 to 32.400,000 mc, controlled by the divide-by-N counter in its phase-locked loop, located in the digital #3 card. The counter is programmed by setting the 10 kc, 1 kc, and 100 cps tuning dials. When the three dials are set at 000, the counter functions as a divide-by-2000 frequency divider. For a 999 dial setting, the counter functions as a divide-by-2999 frequency divider. A mixer stage combines the vco output with a fixed 30 mc frequency derived from the 3 mc frequency standard, and the difference frequencies from 3.598,800 to 2.400,000 mc are applied to the counter input. The resultant 1.2 kc counter output frequency is compared with a 1.2 kc reference frequency, supplied by the digital #1 card, at the phase detector to lock the vco.

The rf #3 card vco operates over a range from 117.300,000 to 117.200,100 mc, phase-locked to a frequency derived from the rf #2 card vco circuit. The phase-locked loop is contained in the rf #3 card. The loop mixer stage combines the vco output frequency with a fixed 120 mc frequency, derived from the 3 mc frequency standard, to lock the vco over a phase detector frequency range from 2.799,900 to 2.700,000 mc, determined by the vco frequency from the rf #2 card.

When the 10 kc, 1 kc, and 100 cps tuning dials are set, in turn, over their range from 000 to 999 digits, the rf #2 card vco output appears in a series of 1000 frequency steps, 1200 cycles apart. The rf #3 card circuits process the step frequencies for application at the digital #2 card mixer, and also reduce the step separations to the required 100-cycle steps.

When the MEGACYCLES tuning dials are set to a signal frequency of 02.0000 mc, for a synthesizer output frequency of 110.0000 mc, the 100-cycle control circuit supplies a 117.300,000 mc frequency to the digital #2 mixer stage. If the 10 kc, 1 kc, and 100 cps dials are reset to 999, for a signal frequency of 02.0999 mc, the following frequency processing occurs in the synthesizer circuits. The divide-by-N counter in the digital #3 card is programmed to divide-by-2999, and the rf #2 vco is locked at an output frequency of 33.598,800 mc. The divide-by-12 frequency divider in the rf #3 card reduces this frequency to 2.799,900 mc, locking the rf #3 card vco at a frequency of 117.200,100 mc. The digital #2 mixer stage combines this frequency with the 110.000,000 mc output from vco #1 in the rf #1(A) card, to produce a 7.200,100 mc difference frequency. The divide-by-8 frequency divider at the mixer output produces a 0.900,012.5 mc frequency which is applied to the divide-by-N counter. The counter, programmed to divide-by-73 by the mc and 100 kc tuning dials, supplies a 12.328,93 kc frequency to the

phase detector instead of the required 12.5 kc vco "locking" frequency. Unlocked, vco #1 sweeps to a frequency of 109.900,100 mc, corresponding to the MEGACYCLES dials 02.0999 mc setting, and is "locked" at this frequency. The mixer stage output frequency is now 7.300,000 mc, and the divide-by-N counter supplies a 12.5 kc vco "locking" frequency.

The frequency processing procedure described in the previous paragraph occurs immediately following the change in the 10 kc, 1 kc, and 100 cps dial setting from 000 to 999, but has been presented as a series of occurrences to show the function of each circuit involved, in a step-by-step sequence. It is evident that, for each change in the 100-cycle control-dial settings, singly or jointly, the vco circuit (in use) in the rf #1(A) card will shift frequency to correspond with the new signal frequency. For an increase in the signal frequency dial setting, the rf #1(A) synthesizer output frequency decreases proportionally, and for a signal frequency decrease, the synthesizer output frequency increases.

d. STANDARD-FREQUENCY DIVIDERS AND MULTIPLIERS. - The synthesizer also contains frequency dividing and multiplying circuits to supply the reference and mixer injection frequencies for synthesizer circuit operation. The digital #1 card (A1A3A1A7) supplies the 12.5 kc and 1.2 kc reference frequencies, derived from the 3.0 mc frequency standard module (A1A1A1) output via the mixer/multiplier (A1A3A2), to the rf #1(B) and rf #2 cards, respectively. The mixer/multiplier module (A1A3A2) supplies a 30 mc frequency to the digital #3 card (A1A3A1A6), and to frequency multiplier (X4) Z2 (p/o A1A3A1), derived also from the 3.0 mc frequency standard. It also supplies the 117 mc injection frequency for the receiver signal path circuits, and a 3 mc frequency to digital #1 (A1A3A1A7).

e. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the synthesizer module containing the seven printed-circuit cards, with emphasis on the following:

- (1) Seating of the plug-in module in its socket.
- (2) Cable connections (if any) attached to the module.
- (3) Seating of the individual cards in the module pockets.

f. TEST EQUIPMENT. - Use Frequency Counter 5245L with head 5253B or equivalent. No special tools are required.

g. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the MEGACYCLES frequency selector controls as directed.

h. TEST DATA. (See figures 5-34 and 5-35.) - The following trouble shooting steps can be performed, prior to trouble shooting the individual synthesizer module circuits, to verify normal over-all synthesizer operation by measuring the 82 to 110 mc synthesizer output frequencies at various MEGACYCLES tuning dial settings. The test steps have been selected to verify normal operation of the three voltage-controlled oscillators, in the rf #1(A) card (A1A3A1A1), at a central point in their ranges.

(1) Connect frequency counter to the rf #1(A) output connector J2, following removal of shielded cable and connector P1.

(2) Set the MEGACYCLES dials to read 07.0000 mc. Note the counter frequency; it should be 105.0000 mc.

(3) Set the MEGACYCLES dials to read 17.5000 mc. Note the counter frequency; it should be 94.5000 mc.

(4) Set the MEGACYCLES dials to read 26.5000 mc. Note the counter frequency; it should be 85.5000 mc.

i. TROUBLE SHOOTING SUGGESTIONS. - The following trouble shooting suggestions pertain to the synthesizer module circuits and are provided as an aid to the technician for tracing faulty synthesizer operation to a particular circuit card.

(1) VCO OPERATION. - Operation of the three vco's in the rf #1(A) card can usually be verified by changing the position of the mc or 100 kc tuning dials and noting the tuning effect by listening at the panel speaker. For each change in tuning dial position, at these dials, a characteristic thump will be heard as the vco sweeps and locks to the new frequency selection. Continual sweeping (or sweep failure) at a rate of approximately 3 cycles, occurs when the vco does not lock and is indicative of faulty synthesizer operation.

The tuning range of vco #1 is 101 to 110 mc, the range of vco #2 is 91 to 100 mc, and that of vco #3 is 82 to 90 mc. The performance steps described in the previous paragraph can be repeated for the complete tuning range of each of the three vco's, if faulty vco operation in the rf #1(A) card is suspected. Determine the MEGACYCLES dials setting by subtracting the desired vco frequency, in megacycles, from 112.0 mc, the receiver first i-f conversion frequency.

The dc varactor-control voltages for all five vco circuits in the synthesizer can be checked at the test points provided. Refer to the test data provided for the individual synthesizer cards in subsequent paragraphs.

(2) DIVIDE-BY-N COUNTERS. - For a given MEGACYCLES dial setting, the two divide-by-N digital counters, one in the digital #2 and the other in the digital #3 card, must provide a frequency division by a predetermined factor for normal synthesizer operation. Although it is not practical to attempt to measure the count length during receiver operation, the division factor for either counter can be determined by noting the MEGACYCLES dials positions. To establish the count rate for the digital #2 card counter, simply add the digits 53 to the mc and 100 kc dial readings. For example, a dial reading of 02.0 indicates a count factor of 73, and a dial reading of 29.9 a count factor of 352, the counter range limits. To determine the count rate of the digital #3 counter, simply add the digits 2000 to the 10 kc, 1 kc, and 100 cps dial readings. A reading of 000 is a count rate of 2000.

(3) REFERENCE AND STANDARD FREQUENCIES. - Basic synthesizer operation is dependent upon the 12.5 and 1.2 kc reference frequencies supplied by the digital #1 card (A1A3A1A7) and the fixed 3 and 30 mc standard frequencies provided by the mixer/multiplier module (A1A3A2). The absence of any one of these frequencies can completely prevent synthesizer operation by preventing locking of the five vco circuits in their respective cards. Locking of the three vco's in the rf #1(A) card is dependent upon the presence of tuning frequencies from the 100-cycle tuning circuit cards, applied to digital #2 via mixer Z1 (p/o A1A3A1). Consequently, the absence of a tuning frequency or standard frequency at any synthesizer card, or a vco sweep failure can prevent normal synthesizer

operation and will usually be indicated by a continuous sweeping of the three vco's in the rf #1(A) card or no sweep at all.

(4) SYNTHESIZER OPERATING TEST. - Performance of the following test steps will evaluate performance of the complete synthesizer module for all settings of the MEGACYCLES tuning dials, at any point in the receiver frequency range. Although the test is limited to an adjustment of the 1 kc and 100 cps tuning dials, this adjustment influences the operation of all digital tuning circuits.

(a) Set the MEGACYCLES tuning dials to the selected test frequency.

(b) Connect a signal generator to the 50Ω ANT connector (AlA1J1) on the panel. Adjust generator for a 10 uv, unmodulated, test signal, at the selected test frequency.

(c) Place the MODE switch at CW, and the (large) BFO ±3 KC control knob at VAR. Adjust the (small) control knob for a low-pitched beat-note, monitored at the panel speaker.

(d) Adjust the 100 cps tuning dial and note the change in the beat-note, in 100-cycle steps, as the dial is rotated.

(e) Adjust the 1 kc tuning dial and note the change in the beat-note, in 1000-cycle steps, as the dial is rotated.

4-18. MEGACYCLES FREQUENCY SELECTOR AlA1A5. (See figure 4-27.)

The MEGACYCLES frequency selector assembly, located on the receiver front panel, contains the five tuning dials and switches, the dial indicating scales and counter mechanism, and a belt drive mechanism to control frequency selector switch S9 (p/o AlA1) located on the front panel. The assembly includes a shaft extension and coupling to drive the filter selector switch at the input filter module (AlA2A1). Dial lamps are provided for each tuning dial window, controlled by the PUSH FOR DIAL LIGHTS panel switch (AlA1S3). Faulty operation of the frequency selector assembly can affect a portion of the receiver tuning range, or prevent reception completely.

a. DESCRIPTION. - The five tuning dials on the MEGACYCLES assembly select the receiver tuning frequencies, from 2.0 to 29.9999 mc in increments of 100 cycles, by controlling the 82 to 110 mc "locking" frequency applied to the vhf oscillator phase-locked loop circuit in the front-end module (AlA2A2). Setting the tuning dials to the signal frequency, in megacycles, controls the synthesizer (AlA3A1) circuits and selects the corresponding vhf oscillator "locking" frequency for signal reception at the dialed frequency. The five tuning dials develop a binary code which controls a number of integrated circuit (IC) reset gates, which in turn control the counting rates of two IC digital-type pulse counters functioning as variable frequency-dividing circuits. The two divide-by-N counters are located, together with their control gates, in the digital #2 card (AlA3A1A3) and the digital #3 card (AlA3A1A6), respectively.

(1) DIGITAL SWITCHES. - The five tuning dials, mc, 100 kc, 10 kc, 1 kc, and 100 cps, control the rotary switches S1 through S5, respectively. The mc dial, via a toothed belt drive mechanism, also controls rotary switch S9 (p/o AlA1). The rotary switch contracts are arranged to provide either a ground or open circuit connection at the various switch positions, and in this manner

develop a binary code to control the reset gate circuits. Switches S3, S4, and S5 control reset gates Z17, Z12, and Z11 at the digital #3 card. Switches S9 (p/o A1A1), S1, and S2 control reset gates Z8, Z13, and Z12 in the digital #2 module. Note that a section of switch S9 (p/o A1A1) selects the voltage controlled oscillator (vco) in the rf #1(A) card to be used at various positions of the mc tuning dial.

(2) DIAL SCALES. - The 100 kc, 10 kc, 1 kc, and 100 cps tuning dials are equipped with rotary dial scales bearing the digits 0 to 9 for the ten digital switch positions. The mc dial employs a two-drum counter, driven by the dial shaft. The counter drums present a reading from 02 to 29 for a total of 28 mc switch positions, to represent the receiver tuning frequency in whole megacycles. The receiver panel bears a decimal point, midway between the mc and 100 kc tuning dial positions, to facilitate setting and reading the scale indicators in megacycles.

(3) VCO SELECTION. - Section A of switch S9 (p/o A1A1) selects the voltage-controlled oscillator to be used at the rf #1(A) card by controlling the +15 volt dc operating potential to the three vco circuits. The following list identifies the vco, its frequency range in megacycles, and the related mc dial positions.

<u>Vco</u> <u>Used</u>	<u>Frequency</u> <u>Range (Mc)</u>	<u>Mc</u> <u>Dial</u>
#1	101 to 110	02 to 11
#2	91 to 100	12 to 21
#3	82 to 90	22 to 29

(4) ANTENNA FILTER SELECTION. - The extension shaft and coupling driven by the mc tuning dial mechanism controls the position of selector switch S1 at the input filter module (A1A2A1). In this manner, setting the mc tuning dial also selects the appropriate bandpass filter at the receiver antenna input circuit. The following list identifies the filter, its bandpass frequencies, and the related mc dial positions.

<u>Input</u> <u>Filter</u>	<u>Passband</u> <u>(Mc)</u>	<u>Mc</u> <u>Dial</u>
FL2	2 to 3	02
FL3	3 to 5	03 to 04
FL4	5 to 8	05 to 07
FL5	8 to 12	08 to 11
FL6	12 to 19	12 to 18
FL7	19 to 30	19 to 29

(5) BINARY SWITCHING CODE. - Table 4-1 lists the binary code employed by the MEGACYCLES dials switch-circuits to control the reset gates in the digital #2 and digital #3 cards, and in turn control the count length of the associated divide-by-N digital counters. The reset gates function as positive logic NAND gates. An open switch contact is a logical one (1), and a grounded contact a logical zero (0). The binary code derived from the tuning dial positions is similar to a digital ABCD code but has been modified to accommodate the synthesizer control requirements. Note that the tuning dials have a decimal relation to the divide-by-N counters they control. For the digital #3 card divide-by-N counter (counting range 2999 to 2000), the 100 cps dial controls counting in "units", the 1 kc dial in "tens", and the 10 kc dial in "hundreds". The digital #2 card

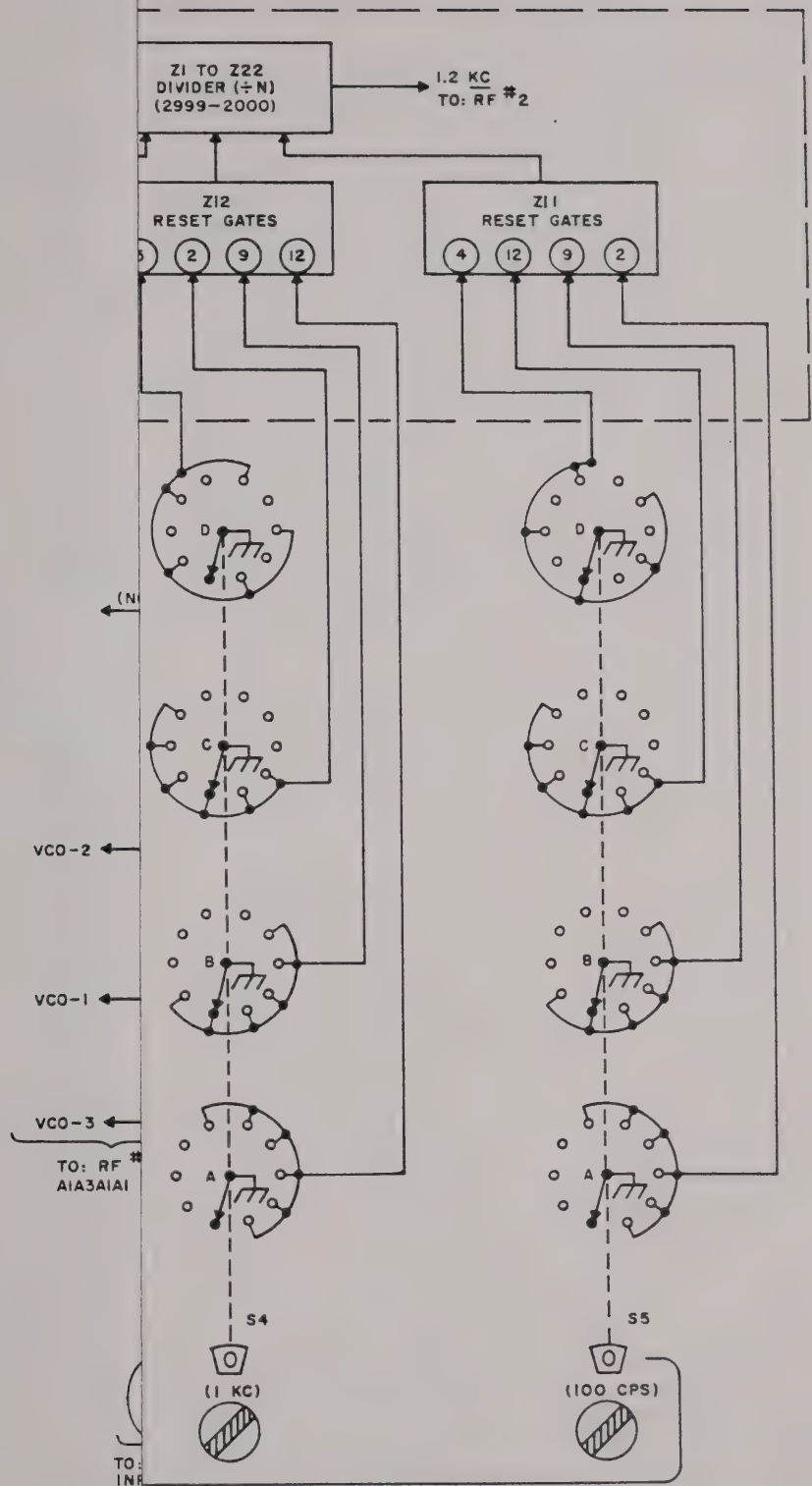


Figure 4-27. MEGACYCLES Frequency Selector A1A1A5, Functional Diagram

develop a binary code to control the reset gate circuits. Switches S3, S4, and S5 control reset gates Z17, Z12, and Z11 at the digital #3 card. Switches S9 (p/o A1A1), S1, and S2 control reset gates Z8, Z13, and Z12 in the digital #2 module. Note that a section of switch S9 (p/o A1A1) selects the voltage controlled oscillator (vco) in the rf #1(A) card to be used at various positions of the mc tuning dial.

(2) DIAL SCALES. - The 100 kc, 10 kc, 1 kc, and 100 cps tuning dials are equipped with rotary dial scales bearing the digits 0 to 9 for the ten digital switch positions. The mc dial employs a two-drum counter, driven by the dial shaft. The counter drums present a reading from 02 to 29 for a total of 28 mc switch positions, to represent the receiver tuning frequency in whole megacycles. The receiver panel bears a decimal point, midway between the mc and 100 kc tuning dial positions, to facilitate setting and reading the scale indicators in megacycles.

(3) VCO SELECTION. - Section A of switch S9 (p/o A1A1) selects the voltage-controlled oscillator to be used at the rf #1(A) card by controlling the +15 volt dc operating potential to the three vco circuits. The following list identifies the vco, its frequency range in megacycles, and the related mc dial positions.

<u>Vco</u> <u>Used</u>	<u>Frequency</u> <u>Range (Mc)</u>	<u>Mc</u> <u>Dial</u>
#1	101 to 110	02 to 11
#2	91 to 100	12 to 21
#3	82 to 90	22 to 29

(4) ANTENNA FILTER SELECTION. - The extension shaft and coupling driven by the mc tuning dial mechanism controls the position of selector switch S1 at the input filter module (A1A2A1). In this manner, setting the mc tuning dial also selects the appropriate bandpass filter at the receiver antenna input circuit. The following list identifies the filter, its bandpass frequencies, and the related mc dial positions.

<u>Input</u> <u>Filter</u>	<u>Passband</u> <u>(Mc)</u>	<u>Mc</u> <u>Dial</u>
FL2	2 to 3	02
FL3	3 to 5	03 to 04
FL4	5 to 8	05 to 07
FL5	8 to 12	08 to 11
FL6	12 to 19	12 to 18
FL7	19 to 30	19 to 29

(5) BINARY SWITCHING CODE. - Table 4-1 lists the binary code employed by the MEGACYCLES dials switch-circuits to control the reset gates in the digital #2 and digital #3 cards, and in turn control the count length of the associated divide-by-N digital counters. The reset gates function as positive logic NAND gates. An open switch contact is a logical one (1), and a grounded contact a logical zero (0). The binary code derived from the tuning dial positions is similar to a digital ABCD code but has been modified to accommodate the synthesizer control requirements. Note that the tuning dials have a decimal relation to the divide-by-N counters they control. For the digital #3 card divide-by-N counter (counting range 2999 to 2000), the 100 cps dial controls counting in "units", the 1 kc dial in "tens", and the 10 kc dial in "hundreds". The digital #2 card

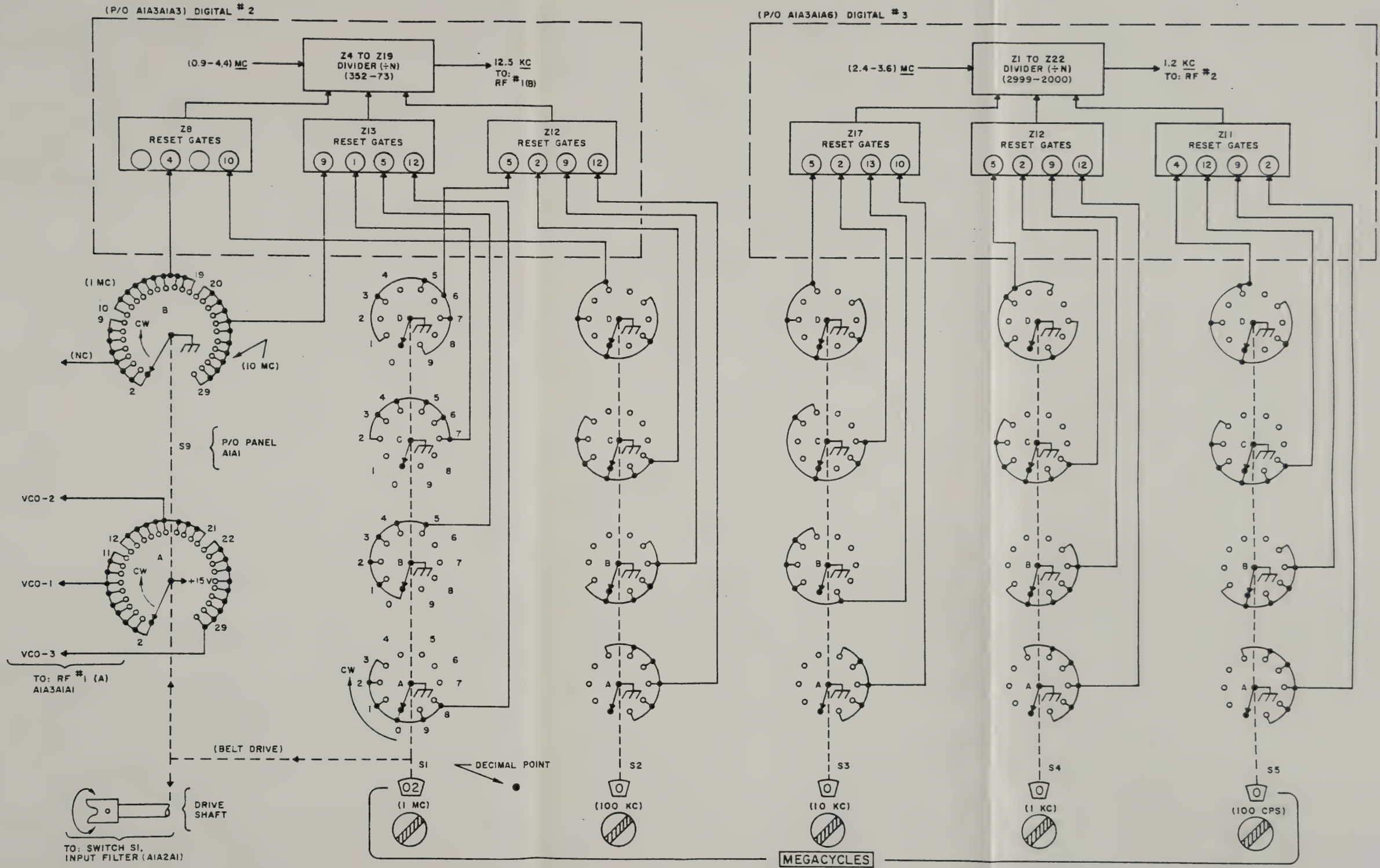


Figure 4-27. MEGACYCLES Frequency
Selector A1A1A5, Functional Diagram

TABLE 4-1. MEGACYCLES-DIALS BINARY CODE

100 CPS DIAL						10 KC DIAL (Cont)							
SET	S5D	S5C	S5B	S5A	÷N	SET	S3D	S3C	S3B	S3A	÷N		
0	0	0	0	1	2000	5	1	1	1	0	2500		
1	1	0	0	1	2001	6	0	1	1	0	2600		
2	0	0	1	1	2002	7	1	0	1	0	2700		
3	1	0	1	1	2003	8	0	0	1	0	2800		
4	0	1	1	0	2004	9	1	1	0	0	2900		
5	1	1	1	0	2005	100 KC DIAL							
6	0	1	0	0	2006	SET	S2D	S2C	S2B	S2A	÷N		
7	1	1	0	0	2007	0	0	0	0	1	73		
8	0	0	0	0	2008	1	1	0	0	1	74		
9	1	0	0	0	2009	2	0	0	1	1	75		
1 KC DIAL						3	1	0	1	1	76		
SET	S4D	S4C	S4B	S4A	÷N	4	0	1	1	0	77		
0	1	0	0	1	2000	5	1	1	1	0	78		
1	0	0	0	1	2010	6	0	1	0	0	79		
2	1	0	1	1	2020	7	1	1	0	0	80		
3	0	0	1	1	2030	8	0	0	0	0	81		
4	1	1	1	0	2040	9	1	0	0	0	82		
5	0	1	1	0	2050	1 AND 10 MC DIAL							
6	1	1	0	0	2060	SET	S1D	S1C	S1B	S1A	S9 10-19	S9 20-29	÷N
7	0	1	0	0	2070	02	1	0	0	0	1	1	73
8	1	0	0	0	2080	03	0	0	0	0	1	1	83
9	0	0	0	0	2090	04	1	0	0	1	1	1	93
10 KC DIAL						05	0	0	0	1	1	1	103
SET	S3D	S3C	S3B	S3A	÷N	06	1	0	1	1	1	1	113
0	0	0	1	1	2000	07	0	0	1	1	1	1	123
1	1	1	0	1	2100	08	1	1	1	0	1	1	133
2	0	1	0	1	2200	09	0	1	1	0	1	1	143
3	1	0	0	1	2300	10	1	1	0	0	0	1	153
4	0	0	0	1	2400	11	0	1	0	0	0	1	163

TABLE 4-1. MEGACYCLES-DIALS BINARY CODE (Cont)

1 AND 10 MC DIAL (Cont)								1 AND 10 MC DIAL (Cont)							
SET	S1D	S1C	S1B	S1A	S9 10-19	S9 20-29	÷N	SET	S1D	S1C	S1B	S1A	S9 10-19	S9 20-29	÷N
12	1	0	0	0	0	1	173	21	0	1	0	0	1	0	263
13	0	0	0	0	0	1	183	22	1	0	0	0	1	0	273
14	1	0	0	1	0	1	193	23	0	0	0	0	1	0	283
15	0	0	0	1	0	1	203	24	1	0	0	1	1	0	293
16	1	0	1	1	0	1	213	25	0	0	0	1	1	0	303
17	0	0	1	1	0	1	223	26	1	0	1	1	1	0	313
18	1	1	1	0	0	1	233	27	0	0	1	1	1	0	323
19	0	1	1	0	0	1	243	28	1	1	1	0	1	0	333
20	1	1	0	0	1	0	253	29	0	1	1	0	1	0	343
Ground = logical 0, open circuit = logical 1.															

divide-by-N counter (counting range 352 to 73), has a total of 280 frequency-count selections, the 100-kc dial counting in "units", and the mc dial counting in "tens" and in "hundreds".

b. PRELIMINARY CHECK. (See figure 4-27.) - With power off, make a preliminary check of the MEGACYCLES frequency selector assembly before trouble shooting, with emphasis on the following:

- (1) Cable connections to the assembly.
- (2) Mechanical operation of the tuning dials.

c. TEST EQUIPMENT. - Use Multimeter AN/USM-116. No special tools are required.

d. TEST DATA. (See figures 5-2 and 5-3.) - Trouble shooting the MEGACYCLES frequency selector assembly consists of checking the tuning dial switching-circuits by connecting the multimeter between the assembly frame (ground) and the circuit terminals at cable connectors P1 and P2. A ground (zero ohms) measurement should occur at the various switch positions which designate a logical zero (see table 4-1), and an open circuit should occur at all other switch positions. The switch section S9A (p/o A1A1) measurements are an exception to this rule. A measurement of +15 volts dc will be found at the related cable terminals; the operating voltage for the vco circuits in the rf #1(A) card (A1A3A1A1).

(1) For all continuity measurements, connect the multimeter to the connector terminals listed in table 4-2. Use the low-ohm range.

(2) For all voltage measurements, connect the multimeter to the connector terminals listed in table 4-2 (P1-K, P1-L, and P1-M only). Use an appropriate dc range.

TABLE 4-2. MEGACYCLES-DIALS TEST DATA

CONN	TERM.	SWITCH	DIAL	DIAL TEST POSITIONS	TEST
P1	L	S9A	<u>MC</u>	02 thru 11	+15V
	M			12 thru 21	+15V
	K			22 thru 29	+15V
	N	S9B		10 thru 19	GRD
	P			20 thru 29	GRD
P2	H	S1A	<u>MC</u>	02, 03, 08 thru 13, 18 thru 23, 28, 29	GRD
	J	S1B		02 thru 05, 10 thru 15, 20 thru 25	GRD
	K	S1C		02 thru 07, 12 thru 17, 22 thru 27	GRD
	L	S1D		03, 05, 07, 09, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29	GRD
P2	M	S2A	<u>100</u> <u>KC</u>	4 thru 9	GRD
	N	S2B		0, 1, 6 thru 9	GRD
	P	S2C		0 thru 3, 8, 9	GRD
	R	S2D		0, 2, 4, 6, 8	GRD
P2	S	S3A	<u>10</u> <u>KC</u>	5 thru 9	GRD
	T	S3B		1 thru 4, 9	GRD
	U	S3C		0, 3, 4, 7, 8	GRD
	V	S3D		0, 2, 4, 6, 8	GRD
P2	W	S4A	<u>1</u> <u>KC</u>	4 thru 9	GRD
	X	S4B		0, 1, 6 thru 9	GRD
	Y	S4C		0 thru 3, 8, 9	GRD
	Z	S4D		1, 3, 5, 7, 9	GRD
P2	a	S5D	<u>100</u> <u>CPS</u>	0, 2, 4, 6, 8	GRD
	b	S5C		0 thru 3, 8, 9	GRD
	c	S5B		0, 1, 6 thru 9	GRD
	d	S5A		4 thru 9	GRD

4-19. RF #1(A), A1A3A1A1. (See figures 4-28, 4-29, and 4-30.)

The rf #1(A) card contains a dc amplifier, three voltage-controlled oscillators (vco), an output amplifier, and a vco supply-voltage distribution circuit. Faulty operation of this card can prevent reception completely.

a. DESCRIPTION. - The rf #1(A) card generates the 82 to 110 mc synthesizer output frequencies applied to the front-end module (A1A2A2) to obtain receiver tuning, in increments of 100 cycles, over the 2.0 to 29.9999 mc frequency range. The remaining synthesizer (A1A3) circuits serve to control and direct this process, with minor exceptions.

The dc amplifier provides a dc varactor-control voltage, supplied from the rf #1(B) card (A1A3A1A4), to the three varactor tuned vco's to control their frequencies. Vco operation is not simultaneous; only one vco is in operation at any given time. The supply-voltage distribution circuit, controlled by the mc tuning dial (p/o A1A1A5), supplies an operating voltage to the vco selected for operation and disables the other two vco's. Vco output frequencies are supplied directly to the front-end module, and after amplification by the output amplifier, to the digital #2 card (A1A3A1A3), via mixer Z1 (p/o A1A3A1).

(1) FILTER AMPLIFIER. (See figure 4-28.) - The filter amplifier consisting of Q1 through Q4 amplifies the dc control voltage prior to application at the vco varactors. A 12.5 kc twin "T" filter at the amplifier input rejects this frequency component which is contributed by a phase detector in the rf #1(B) card. The filter network comprises capacitors C1 through C3 and C5, and resistors R2, R3, R4, and R6. The input stages Q1 and Q2 are directly coupled to emitter-follower Q3. Dc output from Q3 is applied to the output via an "active" low-pass filter formed by C7 and C8, Q4, and R12 and R15. The filter has a 3 kc "roll-off" point and normal attenuation would be -6 db/octave. Capacitor C7 forms a feedback loop to the base of Q4 to make the filter an "active" network and increase the attenuation factor to -12 db/octave. Harmonics of the 12.5 kc frequency component are removed by this filter.

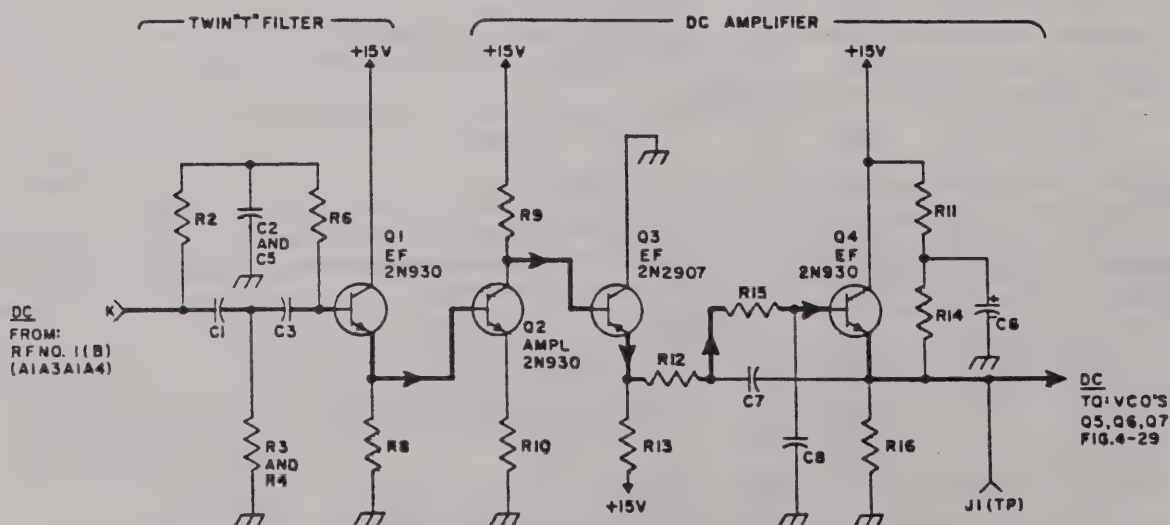


Figure 4-28. RF #1(A) A1A3A1A1; Filter-Amplifier, Simplified Schematic Diagram

(2) VCO #1, #2, and #3. (See figure 4-29.) - The three voltage-controlled oscillators, connected in parallel, are identical except for their individual frequency ranges. Vco #1 generates frequencies from 101 to 110 mc, vco #2 generates from 91 to 100 mc, and vco #3 from 82 to 90 mc, covering the synthesizer frequency range of 82 to 110 mc in three steps. The circuit description to follow for vco #1 also applies to the other vco circuits, with exception of the frequency range.

The vhf voltage-controlled oscillator vco #1 employs Q5 in a modified Colpitts circuit. The tank circuit is formed by inductor L1 tuned by capacitor C15 and varactor CR1 in series, and feedback capacitors C13 and C14. Oscillator output is obtained at the junction of resistors R23 and R24 in the feedback circuit. Dc varactor control voltage is applied to CR1 through isolation resistor R25. The control voltage ranges from approximately 4.5 volts dc, for an oscillator frequency of 101 mc, to approximately 10.5 volts dc for a frequency of 110 mc.

The low end of the oscillator tank circuit is grounded; therefore, the collector supply-voltage polarity has been inverted and applied to the Q5 emitter via resistor R22 with decoupling capacitor C12. The vco supply-voltage distribution circuit provides a vco #1 operating potential only when the mc tuning dial (p/o A1A1A5) is set at positions 02 through 11 mc; the vco #1 is disabled for other mc dial positions (see paragraph 4-18a(3) list for vco operating sequences).

(3) OUTPUT AMPLIFIER. (See figure 4-30.) - The output amplifier for the three vco's consists of Q8 and Q9. The vhf output frequency, from the vco in operation, is amplified prior to application at the digital #2 card (A1A3A1A3). Self-tuned inductor L4 at the collector of Q9 functions as a tuned circuit. Operating voltage for the output amplifier is obtained directly from decoupling stage Q10 in the supply-voltage distribution circuit.

(4) SUPPLY-VOLTAGE DISTRIBUTION CIRCUIT. (See figure 4-30.) - The supply-voltage distribution circuit for card rf #1(A) consists of the decoupling stage Q10 and switch stages Q11 through Q13. Gate diodes CR4 through CR6 control application of the +12 volt supply voltage at the emitter of Q10 to the three vco circuits, in response to switch stage operation.

Depending upon the mc tuning dial position (A1A1S9-A), a +15 volt potential is applied to one of the three switch stages, Q11 through Q13. For example: When the mc dial is set from 02 to 11 mc, +15 volts is applied to the emitter of switch Q11 and Q11 saturates, forward-biasing diode CR4 to apply +12 volts to vco #1. In the absence of saturation at Q12 and Q13, diodes CR5 and CR6 remain reverse-biased blocking an application of +12 volts to vco #2 and vco #3. In this manner, each vco in turn is provided with an operating voltage controlled by the position of the mc tuning dial.

Stage Q10 is cut off in the absence of a collector potential, until a switch stage becomes saturated to provide the collector a return path to ground. Q10 then functions as an emitter-follower, and also performs a circuit decoupling function. Capacitor C32, in conjunction with resistor R50, performs an initial supply-circuit decoupling function to isolate the vco and output amplifier. Q10 multiplies the effective capacitance of C32 (15 uf) by the current gain factor (beta) to obtain a capacitance effect approximately 50 times larger (75 uf) at the emitter circuit, thus improving the degree of decoupling.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the rf #1(A) card before beginning trouble shooting, with emphasis on the following:

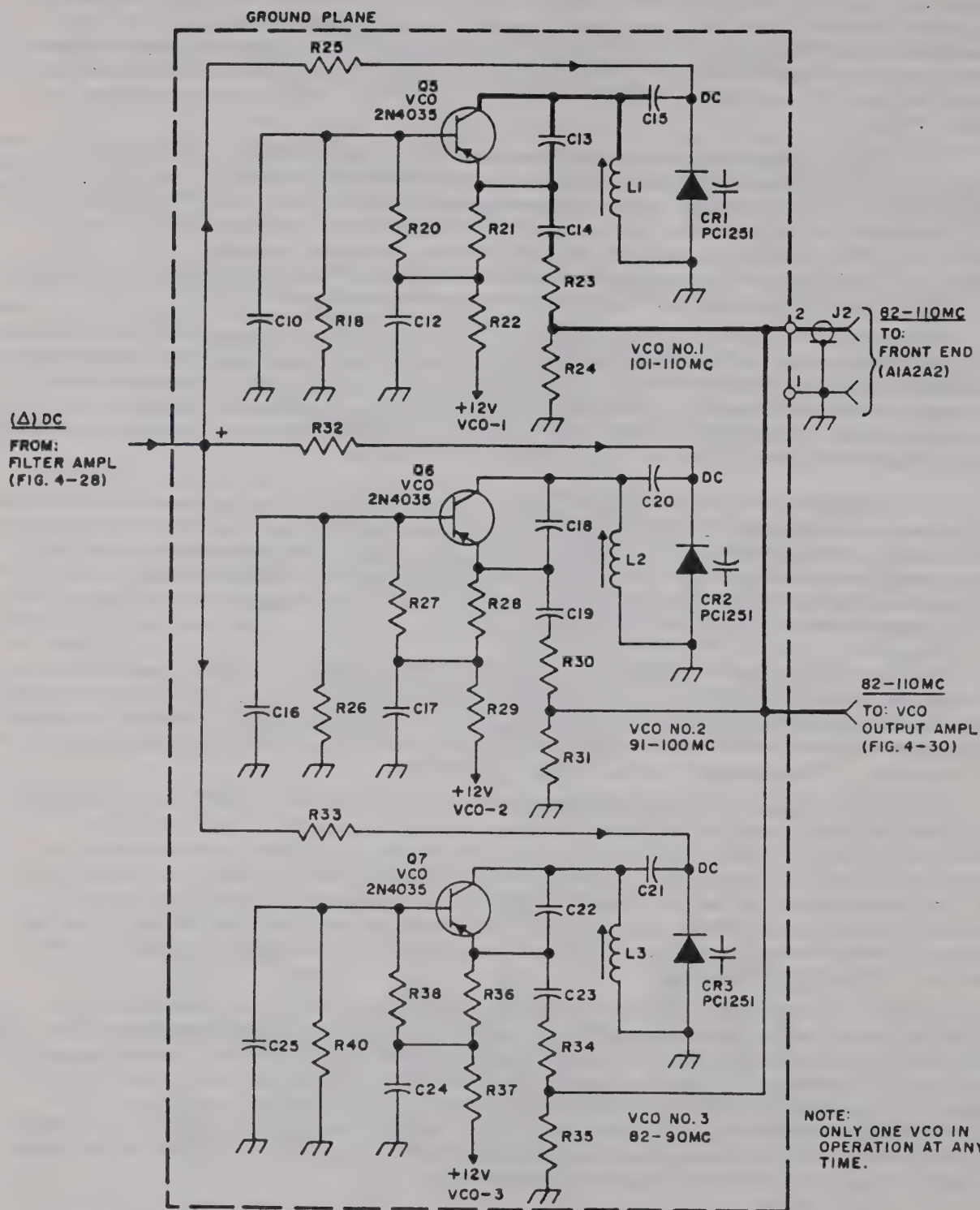


Figure 4-29. RF #1(A) A1A3A1A1; VCO Circuits, Simplified Schematic Diagram

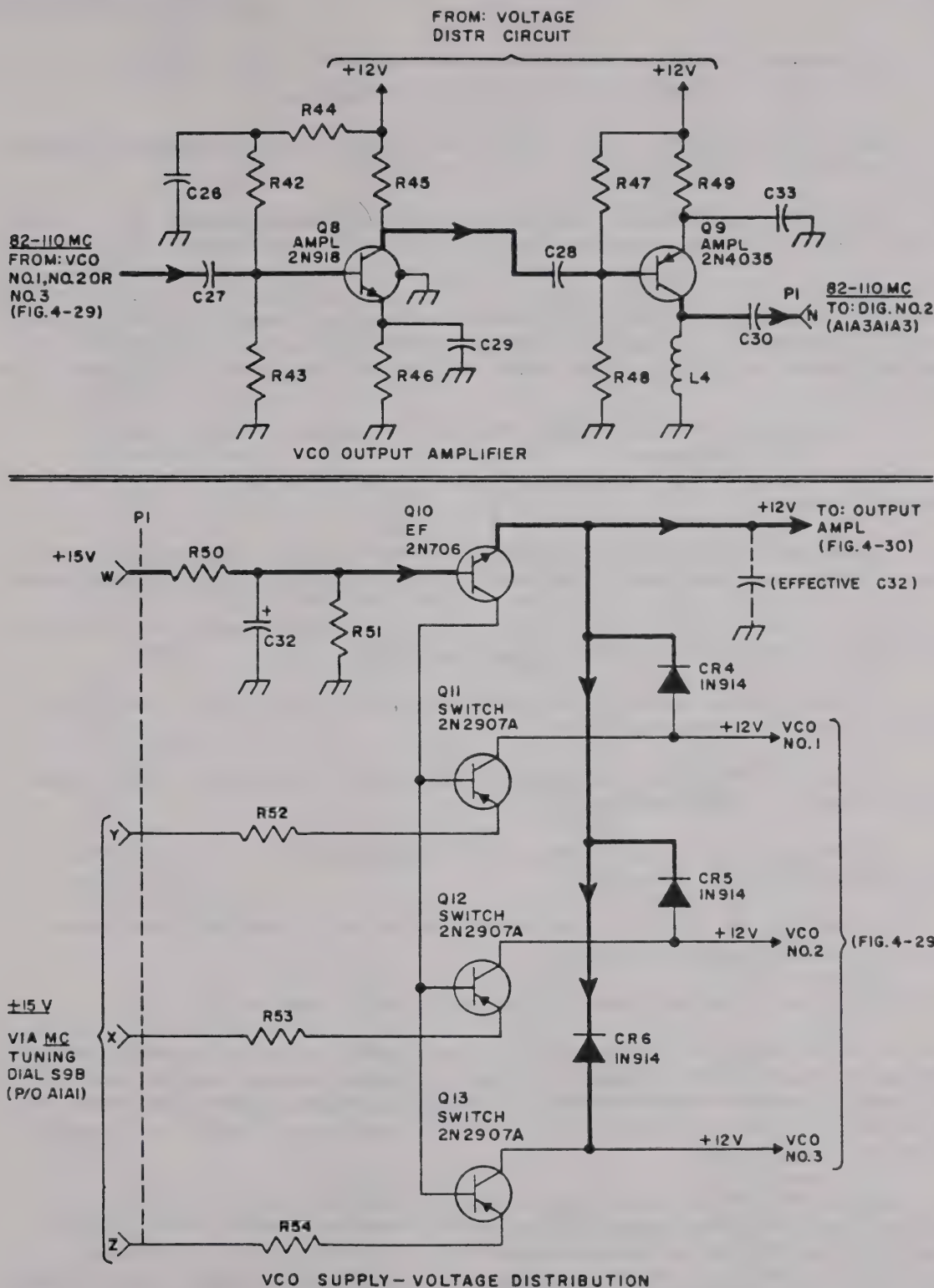


Figure 4-30. RF #1(A) A1A3A1A1; VCO Output Amplifier and VCO Supply-Voltage Distribution Circuit, Simplified Schematic Diagrams

- (1) Seating of plug-in card in its compartment.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use VTVM AN/USM-116 and Frequency Counter 5245L, or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the mc tuning dial (p/o A1A1A5) as directed.

e. TEST DATA. (See figure 5-36.) - Trouble shooting the rf #1(A) card consists of measuring the dc varactor-control voltage and monitoring the synthesizer output frequency. Voltage and frequency measurements are performed at the upper and lower frequency range limits for each of the three vco circuits. Perform the following:

- (1) Connect dc VTVM to test point J1(TP) at the rf #1(A) card.
- (2) Disconnect the synthesizer output cable at connector J2 and attach the frequency counter.
- (3) Set the MEGACYCLES dials to 02.0000 mc. The output frequency should be 110.0000 mc, and the VTVM should indicate +10 volts dc, approximately.
- (4) Set the mc tuning dial (only) to 11. Frequency should be 101.0000 mc, and control voltage +4.5 volts dc, approximately.
- (5) Set mc dial to 12. Frequency should be 100.0000 mc, and control voltage +10 volts dc, approximately.
- (6) Set mc dial to 21. Frequency should be 91.0000 mc, and control voltage -4.5 volts dc, approximately.
- (7) Set mc dial to 22. Frequency should be 90.0000 mc, and control voltage +10 volts dc, approximately.
- (8) Set mc dial to 29. Frequency should be 83.0000 mc, and control voltage -4.5 volts dc, approximately.

4-20. RF #1(B), A1A3A1A4. (See figures 4-31, 4-32, and 4-33.)

The rf #1(B) card contains a dc ramp generator, a digital phase-detector, and a digital frequency-discriminator. These circuits develop and process the dc varactor-control voltage which governs the frequency generated by the three vco circuits in the rf #1(A) card A1A3A1A1. Faulty operation of this card can prevent reception completely.

a. DESCRIPTION. - The rf #1(B) card develops a dc varactor-control voltage as a function of the frequency and phase relation between two input frequencies. A fixed 12.5 kc (reference) frequency from the digital #1 circuit A1A3A1A7, in the form of a negative-going pulse train, is supplied for one input frequency. A variable 12.5 kc (Δf) frequency from the digital #2 card A1A3A1A3, also a negative-going pulse train, is supplied as the other input frequency. The latter frequency originates as a sample of the rf #1(A) card synthesizer-output frequency, and following frequency division performed in the digital #2 card, is compared with the fixed 12.5 kc frequency to obtain a corrective varactor-control

AN/GRR-17
TROUBLE SHOOTING

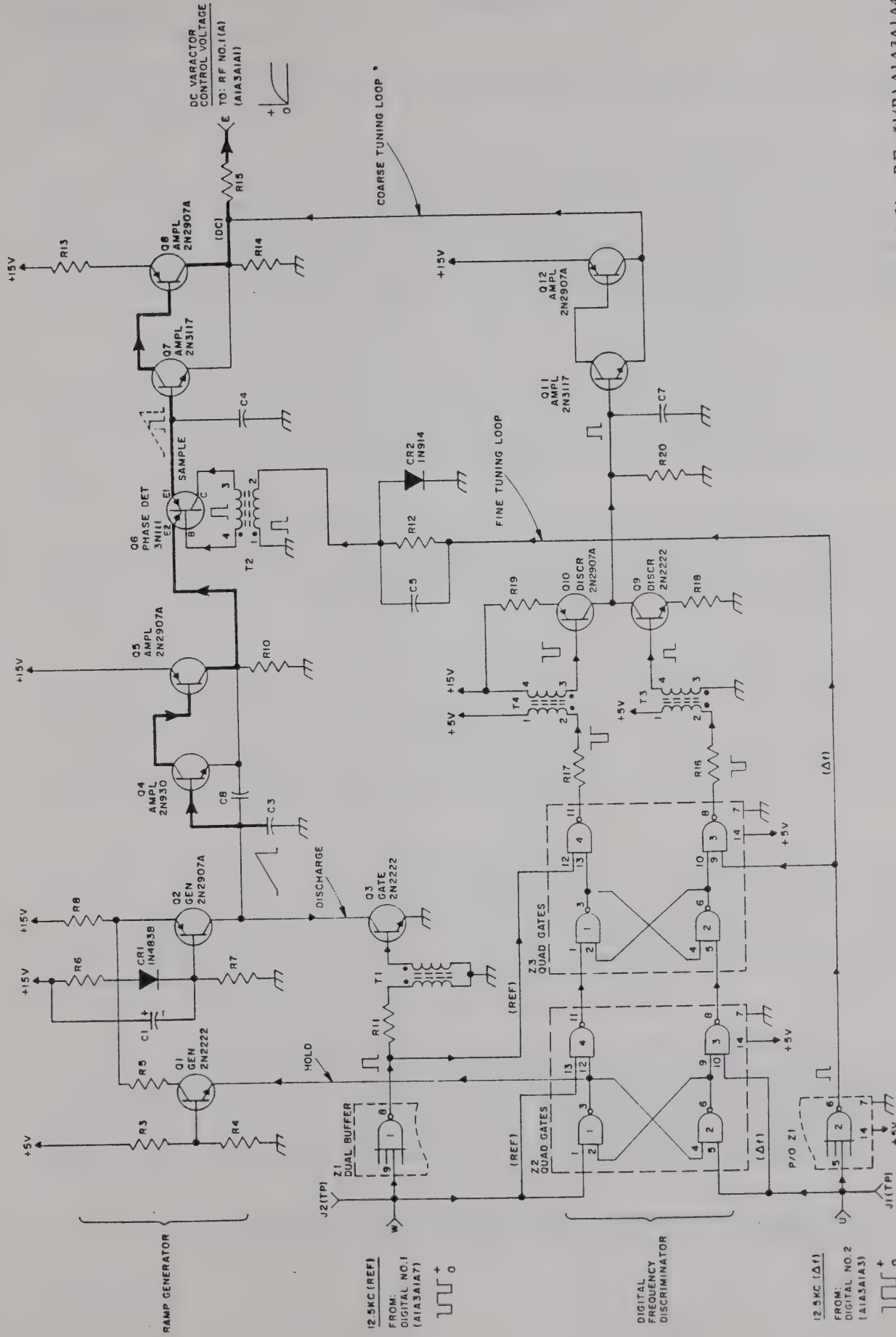


Figure 4-31. RF #1(B) ALA3A1A4;
Simplified Schematic Diagram

voltage which is applied to the vco circuits in the rf #1(A) card. In this manner, the synthesizer output frequency generated by the vco circuits is directly controlled by the rf #1(B) card.

The dc varactor-control voltage is developed by two functional circuits, usually operating in sequence. A coarse-tuning circuit consisting of a digital frequency-discriminator (Q9 and Q10), supplies the control voltage when a relatively large difference in frequency exists between the 12.5 kc reference frequency and the (nominal) 12.5 kc Δf frequency. A fine-tuning circuit employing a dc ramp generator (Q1 and Q2) and a digital phase-detector (Q6), supplies the control voltage when the 12.5 kc reference and Δf frequencies are in close agreement. When frequency coincidence is reached, the control voltage "locks" the related vco circuit.

Because the vco circuits located in the rf #1(A) card cover the 82 to 110 mc synthesizer output range in three steps with only one vco circuit in operation at a given time, a particular dc control voltage will represent any one of three synthesizer output frequencies (see paragraph 4-19a(2)). For each of the three vco circuits, the dc control voltage ranges from approximately +4.5 volts (corresponding to the vco low-frequency limit) to approximately +10 volts (corresponding to the vco high-frequency limit).

(1) COARSE-TUNING CIRCUIT. - The coarse-tuning circuit consists of the digital dual buffer Z1, the two digital dual-input quad gates Z2 and Z3, the digital discriminator stages Q9 and Q10, and the complementary dc amplifier Q11 and Q12. In addition to developing the coarse-tuning varactor control voltage, this circuit also supplies a timing function from Z2 and Z3 to the fine-tuning circuit.

Dual buffer Z1 provides circuit isolation for the two input pulse trains and also inverts the pulses, negative-going input pulse appearing as positive-going output pulses. The dual-input quad gates Z2 and Z3 function as a digital discriminator to control the operation of discriminator stages Q9 and Q10. The individual gates function as a NAND gate and output occurs only when both inputs are present, simultaneously. Operation is similar to an AND gate except that an inversion occurs at the gate output. The first two gates in Z2 and Z3 are connected to form a cross-coupled circuit similar to that of a flip-flop circuit.

Discriminator stages Q9 and Q10 function as a switching circuit, controlled by output pulses from Z3 which are applied via pulse transformers T3 and T4. When Q9 is saturated, it forms a low-impedance quick-discharge path for capacitor C7. When Q10 is saturated, capacitor C7 becomes charged from the +15 volt supply terminal. In this manner, the charge at capacitor C7 is determined by the digital discriminator output supplied from Z3. The charge stored at capacitor C7 passes through the complementary emitter-follower Q11 and Q12 and appears as a dc varactor control voltage at the output of card rf #1(B).

A more detailed description of circuit operation will be given for three typical operating conditions in the following paragraphs. These are: a discriminator "null" condition when the reference frequency (f_r) and the variable frequency (Δf) coincide to "lock" the vco circuits in the rf #1(A) card; a condition where Δf is greater than f_r ; and a condition where Δf is less than f_r . Figure 4-32, the coarse-tuning circuit timing diagram, shows the signal relation at major circuit points for each of the three examples of circuit operation.

(a) Coarse Tuning When $\Delta f = f_r$. - Detail "A" of figure 4-32 shows the timing relation at major points in the coarse-tuning circuit when the two input

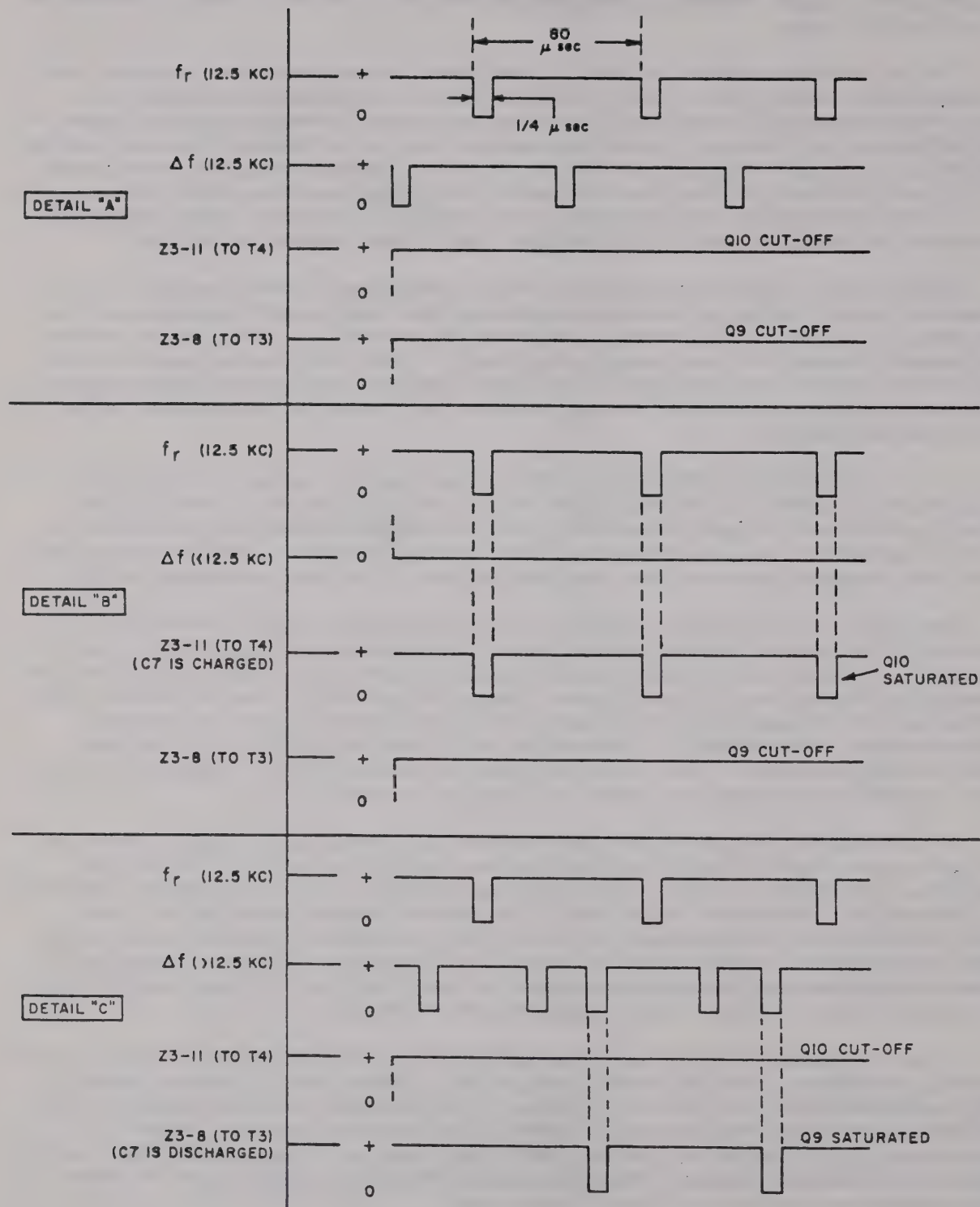


Figure 4-32. Coarse-Tuning Circuit, Timing Diagram

frequencies coincide and a coarse-tuning "null" occurs. A frequency coincidence of 600 cycles or less, well within the operating range of the fine-tuning circuit, will cut off discriminator stages Q9 and Q10 and terminate production of the varactor-control voltage by this circuit. At a coarse-tuning "null" the cross-coupled NAND gates in Z2 and Z3, in conjunction with the direct coupled NAND gates, function to produce a "one" or positive-going output voltage at terminals Z3-11 and Z3-8, simultaneously. The Z3 output gates remain in this operating condition as long as a coarse-tuning "null" exists between Δf and f_r .

The steady dc voltage at the primaries of pulse transformers T3 and T4 does not permit transformer operation, and in the absence of an induced secondary voltage, discriminator stages Q9 and Q10 remain in a cut-off condition. No discriminator output occurs to charge capacitor C7 and the previous charge, obtained prior to the "null", is retained subject to a slow discharge via resistor R20. The transistors selected for the Q9 and Q10 discriminator stages are intended for a switch-circuit operation. Consequently, in the absence of an input signal the two stages are cut off.

(b) Coarse Tuning When $\Delta f < f_r$. - Detail "B" of figure 4-32 shows the circuit timing relation when Δf is less than f_r . To facilitate a description of coarse-tuning circuit operation for this condition, it is assumed that Δf is lower than f_r by several kilocycles. When a frequency coincidence does not exist, the NAND gates in Z2 and Z3 produce a differential output. The lower input frequency provided by Δf continue to appear as a "one" or positive-going dc voltage at terminal Z3-8. The higher input frequency f_r causes production of negative-going pulses at terminal Z3-11, a direct result of the frequency non-coincidence. When a single pulse of frequency coincidence does occur occasionally, no pulse is produced at terminal Z3-11. This occurrence is a normal functional relation between two dissimilar frequencies, but does not affect discriminator operation because the negative-going pulses at terminal Z3-11 are predominant.

When the Δf frequency is less than f_r frequency, the steady dc voltage from terminal Z3-8 remains at the primary of T3 to cut off discriminator stage Q9. The negative-going pulse train from terminal Z3-11 is applied to the primary of transformer T4, inducing a similar pulse in the secondary to drive the base of Q11 and cause saturation. During saturation, capacitor C7 becomes charged from the +15 volt dc supply. This charge is applied to the output of card rf #1(B) via amplifier Q11 and Q12 to form a varactor-control voltage. During coarse-tuning circuit operation, in this phase, the control voltage developed will increase the vco frequency at the rf #1(A) card and thereby increase the Δf frequency until a coarse-tuning circuit "null" is obtained. As the "null" condition is approached, the number of negative-going pulses from Z3-11 diminishes, per unit time, and therefore the rate of charge at capacitor C7 diminishes.

(c) Coarse Tuning When $\Delta f > f_r$. - Detail "C" of figure 4-32 shows the circuit timing relation when Δf is greater than f_r . Again, it is assumed that Δf is greater than f_r by several kilocycles to facilitate a circuit description. The NAND gates in Z2 and Z3 produce a differential output, but now f_r is the lower of the two frequencies and terminal Z3-11 provides a continuous "one" or positive-going pulse. Consequently, the higher frequency of Δf produces a negative-going pulse train at terminal Z3-8 as a direct result of frequency non-coincidence.

The steady dc voltage at Z3-11 causes discriminator stage Q10 to cut off, preventing the charging of capacitor C7 from the +15 volt supply. The negative-going pulse train from terminal Z3-8 causes stage Q9 to saturate and discharge

capacitor C7. In this phase of coarse-tuning circuit operation, the discharge of C7 intermittently by the saturation of Q9 reduces the varactor-control voltage and lowers the frequency of the vco circuit in card rf #1(A). The Δf frequency therefore decreases, and as a coarse-tuning "null" is approached, the number of negative-going pulses at Z3-8 decreases, per unit time, and the C7 rate of discharge is diminished.

It is apparent that discriminator stages Q9 and Q10 function as a switch circuit to either charge capacitor C7 via Q10, or discharge C7 via Q9, depending upon whether the Δf frequency is higher or lower than the f_r frequency. This charge or discharge action is a direct function of the negative-going pulses obtained from the digital discriminator gate circuits in Z2 and Z3, and therefore directly related to the Δf and f_r frequencies. As a "null" condition is approached, the two frequencies approach coincidence and the number of negative-going pulses, per unit time, is reduced causing a "tapering-off" circuit action. When the coarse-tuning circuit "null" occurs and discriminator stages Q9 and Q10 are cut off, the fine-tuning circuit starts operating to bring the Δf and f_r frequencies into an exact coincidence.

(d) Z1 and Z2 Timing Function. - In addition to operating as a part of the coarse-tuning circuit digital discriminator, the dual-input quad gate Z2 and buffer Z1 also supply a timing function to the rf #1(B) card fine-tuning circuit.

A "hold" function obtained at terminal Z2-3 is applied to the emitter of Q1, part of the ramp generator circuit, to stop or "hold" the dc ramp voltage at a rise-point determined by the frequency relation of Δf and f_r during the coarse-tuning "null". The "hold" function is in the form of a negative-going pulse which grounds the Q1 emitter each time a Δf pulse appears. Figure 4-32, the coarse-tuning circuit digital-analysis diagram, shows the derivation of this pulse during gate operation.

A "dump" function developed at terminal Z1-8 of the dual buffer consists of the positive-going f_r pulse train, inverted by the Z1 buffer. This pulse is applied to gate Q3 in the fine-tuning circuit via transformer T1, to saturate Q3 and discharge C3 in the ramp generation circuit and "dump" the dc ramp.

(2) FINE-TUNING CIRCUIT. - The fine-tuning circuit consists of the dc ramp generator Q1 and Q2, a "dump" gate Q3, a dc complementary amplifier Q4 and Q5, a digital phase-detector Q6, and a second dc complementary amplifier Q7 and Q8. The fine-tuning circuit, following development of a "null" condition by the coarse tuning circuit, provides a final tuning adjustment for the rf #1(A) card vco circuits by developing a dc varactor-control voltage which brings the Δf and f_r frequencies into exact coincidence, locking the vco.

(a) Ramp Generator and "Dump" Circuit. - The ramp generator Q1 and Q2 develops a dc ramp voltage by charging capacitor C3. When the Q1 emitter receives a positive-going pulse from terminal Z2-3 of the dual-input quad gate, Q1 becomes cut off permitting capacitor C3 to charge from the +15 volt supply, via Q2. When Q1 receives "zero" (ground) signal from terminal Z2-3, it becomes saturated and the large value of collector current passing through resistor R8, with the accompanying large voltage-drop, disables Q2 and stops the charging process. The charge received by C3 is retained or stored, and the Z2-3 (ground) signal is called the "hold" function because the dc ramp voltage, at that rise point, is held or retained.

Dump gate Q3 becomes saturated and discharges capacitor C3 each time a positive-going "dump" pulse is received from section one of dual-buffer Z1. The pulse is applied to the Q3 base via pulse transformer T1. Consequently, the dc ramp voltage appearing at capacitor C3 is "dumped" by each pulse of the 12.5 kc f_r pulse train, and allowed to rise between pulses, subject to the "hold" action performed by the Z2-3 signal applied at the Q1 emitter.

(b) Digital Phase-Detector Circuit. - Although the dc ramp voltage derived at capacitor C3 is applied to the E2 input of phase-detector Q6 via the dc complementary amplifier Q4 and Q5, detector output will not occur until a corresponding "sampling" pulse is applied via pulse transformer T2. Diode CR2 serves as a dc restorer to hold the "sampling" pulse level constant relative to ground, and R12 with C5 remove switching transients. Detection is essentially a digital circuit process because output at E1 of detector Q6 occurs only for the duration of the "sampling" pulse. The detector output level is determined by the dc ramp level during the "sampling" pulse interval, and will occur over the upper ramp portion from approximately +4.5 volts to the maximum ramp level of +7 volts, relating to the lower and upper frequency limits of the controlled vco in the rf #1(A) card, respectively. Phase detector output charges the storage capacitor C4, and passes through complementary amplifier Q7 and Q8 to be combined with the coarse-tuning output circuit.

(c) Fine-Tuning Circuit Operation. - Figure 4-33, the fine-tuning circuit timing diagram, shows the timing relation at major circuit points during operation of the fine-tuning circuit.

Detail "A" illustrates the dc ramp and the "dump" function, relative to the 12.5 kc f_r pulse train, in the absence of a "hold" signal from terminal Z2-3 of the dual-input quad gates. Dc ramp generation is a continuing function and completely independent of the coarse-tuning circuit function. Note that the "dump" pulse is coincidental with the f_r pulse train.

Detail "B" shows the introduction of a "hold" signal and the retention of the dc ramp level at the point of application. The phase detector "sampling" pulse occurs only during the hold portion of the ramp. "Holding" and "sampling" by the fine-tuning circuit can only occur when the Δf and f_r frequencies are brought to near coincidence by operation of the coarse-tuning circuit. The fine-tuning circuit capture range is approximately 1000 cycles wide, and the coarse-tuning circuit must fulfill this requirement before the fine-tuning circuit will operate.

Detail "C" shows the phase detector "sampled" output and the resultant charge level at storage capacitor C4. Complementary amplifier Q7 and Q8 does not provide voltage amplification, being essentially an emitter-follower circuit, but it does provide circuit isolation between the two tuning circuits.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the rf #1(B) card before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in card in its compartment.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use Oscilloscope Tektronix 545A, or equivalent. No special tools are required.

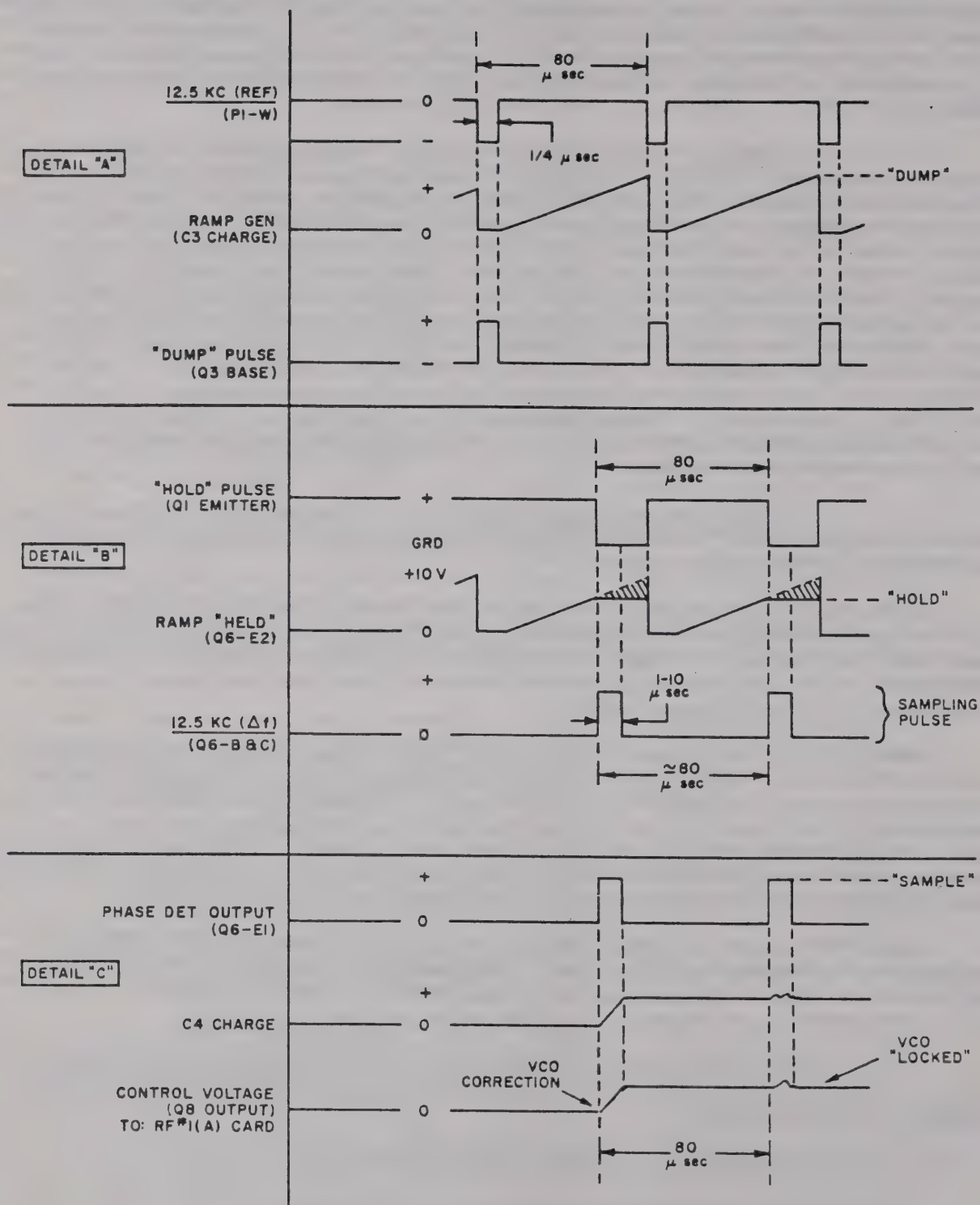


Figure 4-33. Fine-Tuning Circuit, Timing Diagram

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the mc tuning dial (p/o A1A1A5) as directed.

e. TEST DATA. (See figure 5-37.) - Trouble shooting the rf #1(B) card consists of measuring the Δf and f_r input pulse trains at test points provided. The coarse and fine-tuning circuit operation is verified by changing the receiver MEGACYCLES tuning dial position and noting the response of the Δf pulse train. Perform the following:

- (1) Connect oscilloscope to test point J2(TP) on the rf #1(B) card.
- (2) Measure the 12.5 kc f_r pulse train. Amplitude should be approximately +5 volts peak-to-peak. Pulses should be sharp and evenly spaced.
- (3) Connect oscilloscope to test point J1(TP) on the rf #1(B) card.
- (4) Measure the 12.5 kc Δf pulse train. Amplitude should be approximately +5 volts peak-to-peak. Pulses should be sharp and evenly spaced.
- (5) Change the setting of the mc tuning dial on the receiver panel and note the Δf pulse train response several times.
- (6) During step (5), the Δf pulse train should shift its frequency and then return to normal for each position change of the mc tuning dial. The frequency shift is an indication of the coarse and fine-tuning circuit response, and the return to 12.5 kc occurs when the vco circuit in card rf #1(A) is locked at its new operating frequency.

4-21. DIGITAL #2, A1A3A1A3. (See figures 4-34 thru 4-37.)

The digital #2 card contains an input amplifier circuit, a divide-by-eight frequency divider circuit, a divide-by-N digital counter with a variable division range from 352 to 73, and control gates to select the divide-by-N counter range via the mc and 100 kc tuning dials of the MEGACYCLES frequency selector A1A1A5. These circuits form the phase-locked loop for the vco circuits in the rf #1(A) card A1A3A1A1. Faulty operation of this card can prevent reception, partially or completely, over the entire receiver tuning range.

a. DESCRIPTION. (See figure 4-34.) - The digital #2 card indirectly controls the vco operating frequencies at the rf #1(A) card, and therefore controls receiver tuning. A 35.200,000 to 7.300,000 mc frequency from mixer Z1 (p/o A1A3A1) is applied to input amplifier Q1. The divide-by-eight frequency divider circuit (Q5, Q6, Z2, and Z3) reduces this range to 4.400,000 to 0.912,500 mc. The divide-by-N counter (Z4 thru Z7, Z9 thru Z11, and Z14 thru Z19) provides the final frequency reduction to 12.5 kc when set (by the control gates) for frequency division by factors from 352 to 73, respectively. Control gates (Z8, Z12, and Z13), in response to the mc and 100 kc tuning dial settings, govern the divide-by-N counter operation. The mc dial counting (frequency division) by "hundreds" and "tens", and the 100 kc dial controls counting in "units", in a decimal sequence.

The 12.5 kc output from the divide-by-N circuit occurs only when the rf #1(A) vco circuit is phase-locked. When the mc and 100 kc tuning dials are reset, changing the divide-by-N division factor, the initial output frequency is considerably higher (or lower) than 12.5 kc until vco phase-locking has been accomplished. The rf #1(B) card A1A3A1A4 contains both a coarse and fine "tuning" circuit to

accommodate the 12.5 kc Δf range supplied by the digital #2 (see paragraph 4-20).

(1) BINARY LOGIC CIRCUITS. - The following circuit descriptions relate to the digital binary-logic circuits employed in the digital #2 card. They are provided to supplement the functional circuit descriptions. Refer to figure 4-34, the digital #2 simplified block diagram, for identity with the module circuits.

(a) Pulse-Triggered Binaries. - Figure 4-35 provides a comparison, using logic symbols, between a simple triggered flip-flop binary such as the Q5 and Q6 multivibrator stage (divide-by-two) and the dual gated-input binary used extensively in the divide-by-N counter circuit. Each binary employs a basic flip-flop circuit having two outputs. These outputs are termed "mutually exclusive" because when the logical "1" output is on, the logical "0" output is off and vice versa. A flip-flop circuit always remembers its last logical state. For example: the simple flip-flop binary reverses its output state each time a trigger input-pulse is applied, very similar to the operation of pull-chain light switch. The lamp will light every other time the chain is pulled. Consequently, the binary can be used for frequency division by a factor of two because it operates in a similar manner.

The dual gated-input binary, a micro-logic component, contains two dual-input NAND gates which permit control of the two binary states in a particular manner. The gates allow a change in logical state to occur only when both inputs to a gate occur simultaneously. The two inputs, for operation, consist of a fixed dc level representing a logical "0" at the dc input and a negative going pulse at the clock or ac input. For example, with a logical "0" or dc input at S gate, an incoming negative clock pulse will "turn on" or "set" the flip-flop to a "1" at output terminal 3. With a logical "0" or dc input at C gate, an incoming negative clock pulse will "turn off" or "clear" the flip-flop to a "0" at output terminal 3. These conditions assume that the dc input at the "other" gate is a logical "1" during this period. Otherwise, the outputs would be ambiguous. Output terminal 11 is always the complement or opposite level of terminal 3.

The dual gated-input binary flip-flops employed in the digital #2 card are arranged in several configurations. By virtue of the individual ac and dc gate input circuits, the ac terminals 5 and 6 can be paralleled and a timing or clock pulse applied to fix the time and rate of operation. Then, the separate application of dc pulses at terminals 4 and 10 can change the binary logical states. When the output terminals 3 and 11 are connected to the input terminals 4 and 10, respectively, a JK divide-by-two circuit is formed. With this connection, an output logical "1" occurs for every two clock pulses at terminals 5 and 6 to obtain a frequency division by two. Flip-flops Z2, Z3, Z4, Z14, Z18, and Z19 are arranged for this method of operation.

Three dual gated-input binary flip-flops are arranged to form a Johnson counter for a frequency division-by-five by employing "short-count" interconnections. Flip-flops Z9, Z10, and Z11 are used in this circuit, and also flip-flops Z15, Z16, and Z17. Using a "short-count" connection, division-by-five is obtained rather than division-by-eight which is normally available when three flip-flops are series arranged to form a binary register.

The dual gated-input flip-flops have two additional "force" inputs at terminals 1 and 13. This term is employed because a logical "0" or "1" state can be forced, regardless of the normal input-triggered state. These "force" inputs are used to control the divide-by-N counting circuits. The NAND gates of Z8, Z12, and Z13,

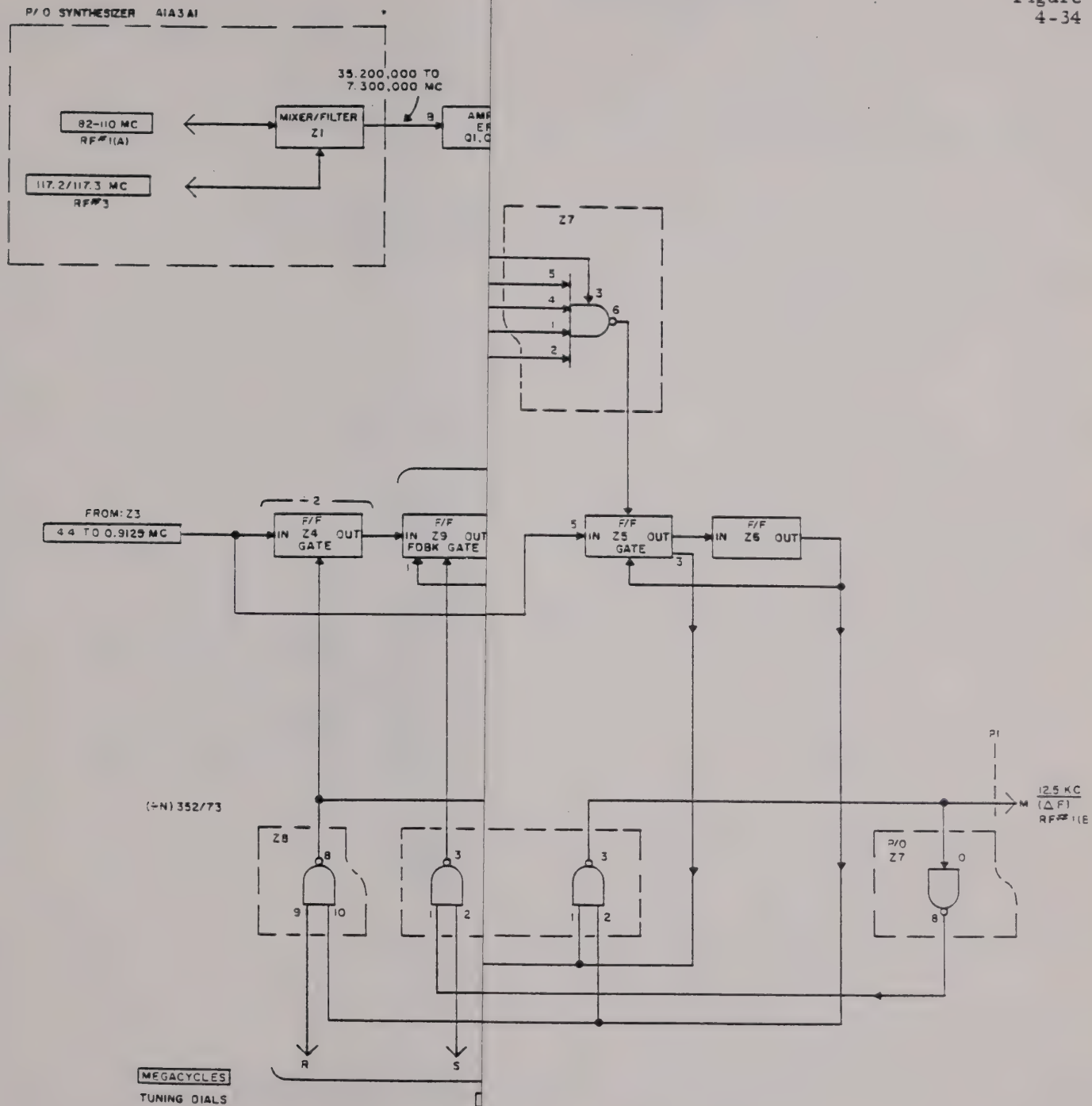


Figure 4-34. Digital #2 A1A3A1A3,
Simplified Block Diagram

accommodate the 12.5 kc Δf range supplied by the digital #2 (see paragraph 4-20).

(1) BINARY LOGIC CIRCUITS. - The following circuit descriptions relate to the digital binary-logic circuits employed in the digital #2 card. They are provided to supplement the functional circuit descriptions. Refer to figure 4-34, the digital #2 simplified block diagram, for identity with the module circuits.

(a) Pulse-Triggered Binaries. - Figure 4-35 provides a comparison, using logic symbols, between a simple triggered flip-flop binary such as the Q5 and Q6 multivibrator stage (divide-by-two) and the dual gated-input binary used extensively in the divide-by-N counter circuit. Each binary employs a basic flip-flop circuit having two outputs. These outputs are termed "mutually exclusive" because when the logical "1" output is on, the logical "0" output is off and vice versa. A flip-flop circuit always remembers its last logical state. For example: the simple flip-flop binary reverses its output state each time a trigger input-pulse is applied, very similar to the operation of pull-chain light switch. The lamp will light every other time the chain is pulled. Consequently, the binary can be used for frequency division by a factor of two because it operates in a similar manner.

The dual gated-input binary, a micro-logic component, contains two dual-input NAND gates which permit control of the two binary states in a particular manner. The gates allow a change in logical state to occur only when both inputs to a gate occur simultaneously. The two inputs, for operation, consist of a fixed dc level representing a logical "0" at the dc input and a negative going pulse at the clock or ac input. For example, with a logical "0" or dc input at S gate, an incoming negative clock pulse will "turn on" or "set" the flip-flop to a "1" at output terminal 3. With a logical "0" or dc input at C gate, an incoming negative clock pulse will "turn off" or "clear" the flip-flop to a "0" at output terminal 3. These conditions assume that the dc input at the "other" gate is a logical "1" during this period. Otherwise, the outputs would be ambiguous. Output terminal 11 is always the complement or opposite level of terminal 3.

The dual gated-input binary flip-flops employed in the digital #2 card are arranged in several configurations. By virtue of the individual ac and dc gate input circuits, the ac terminals 5 and 6 can be paralleled and a timing or clock pulse applied to fix the time and rate of operation. Then, the separate application of dc pulses at terminals 4 and 10 can change the binary logical states. When the output terminals 3 and 11 are connected to the input terminals 4 and 10, respectively, a JK divide-by-two circuit is formed. With this connection, an output logical "1" occurs for every two clock pulses at terminals 5 and 6 to obtain a frequency division by two. Flip-flops Z2, Z3, Z4, Z14, Z18, and Z19 are arranged for this method of operation.

Three dual gated-input binary flip-flops are arranged to form a Johnson counter for a frequency division-by-five by employing "short-count" interconnections. Flip-flops Z9, Z10, and Z11 are used in this circuit, and also flip-flops Z15, Z16, and Z17. Using a "short-count" connection, division-by-five is obtained rather than division-by-eight which is normally available when three flip-flops are series arranged to form a binary register.

The dual gated-input flip-flops have two additional "force" inputs at terminals 1 and 13. This term is employed because a logical "0" or "1" state can be forced, regardless of the normal input-triggered state. These "force" inputs are used to control the divide-by-N counting circuits. The NAND gates of Z8, Z12, and Z13,

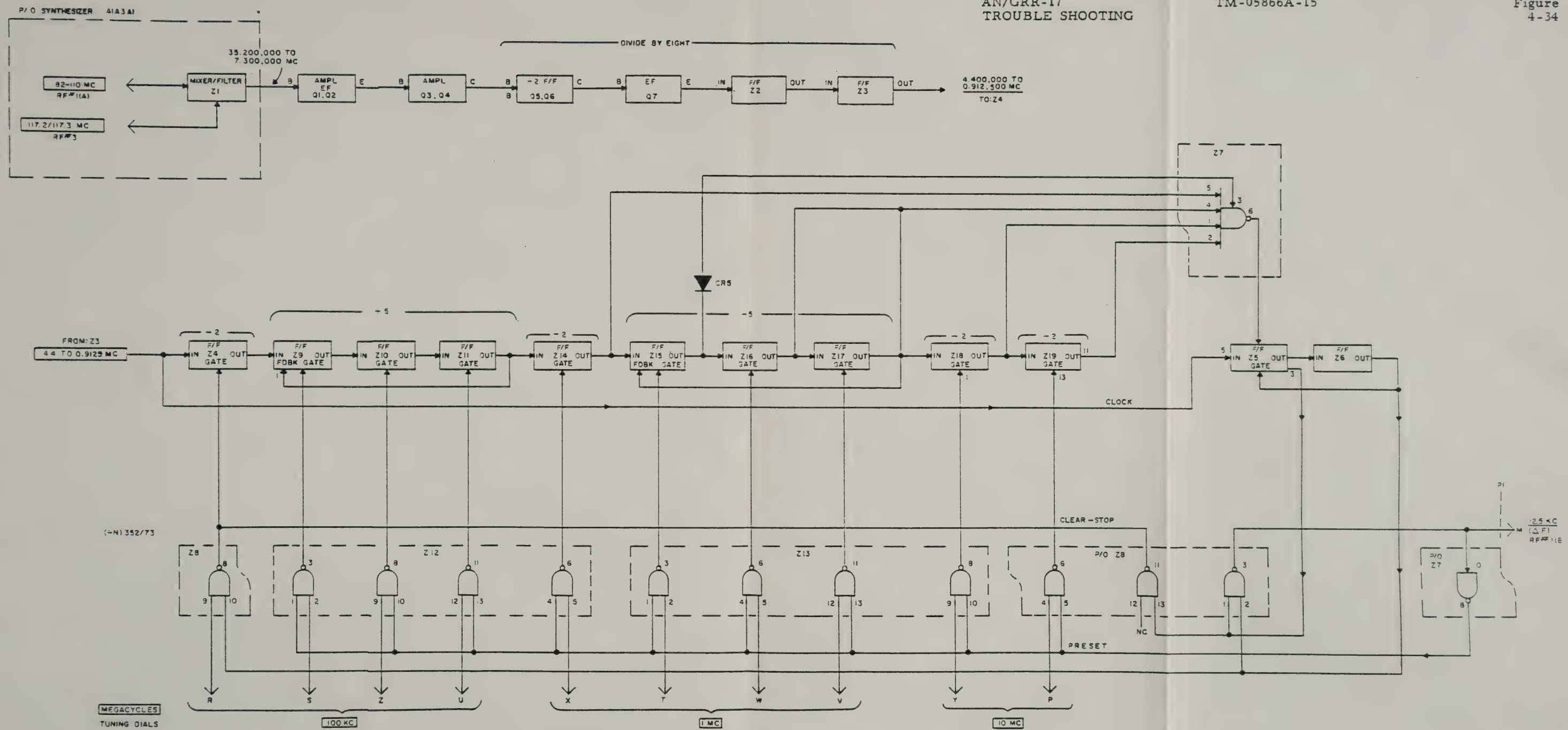


Figure 4-34. Digital #2 A1A3A1A3,
Simplified Block Diagram

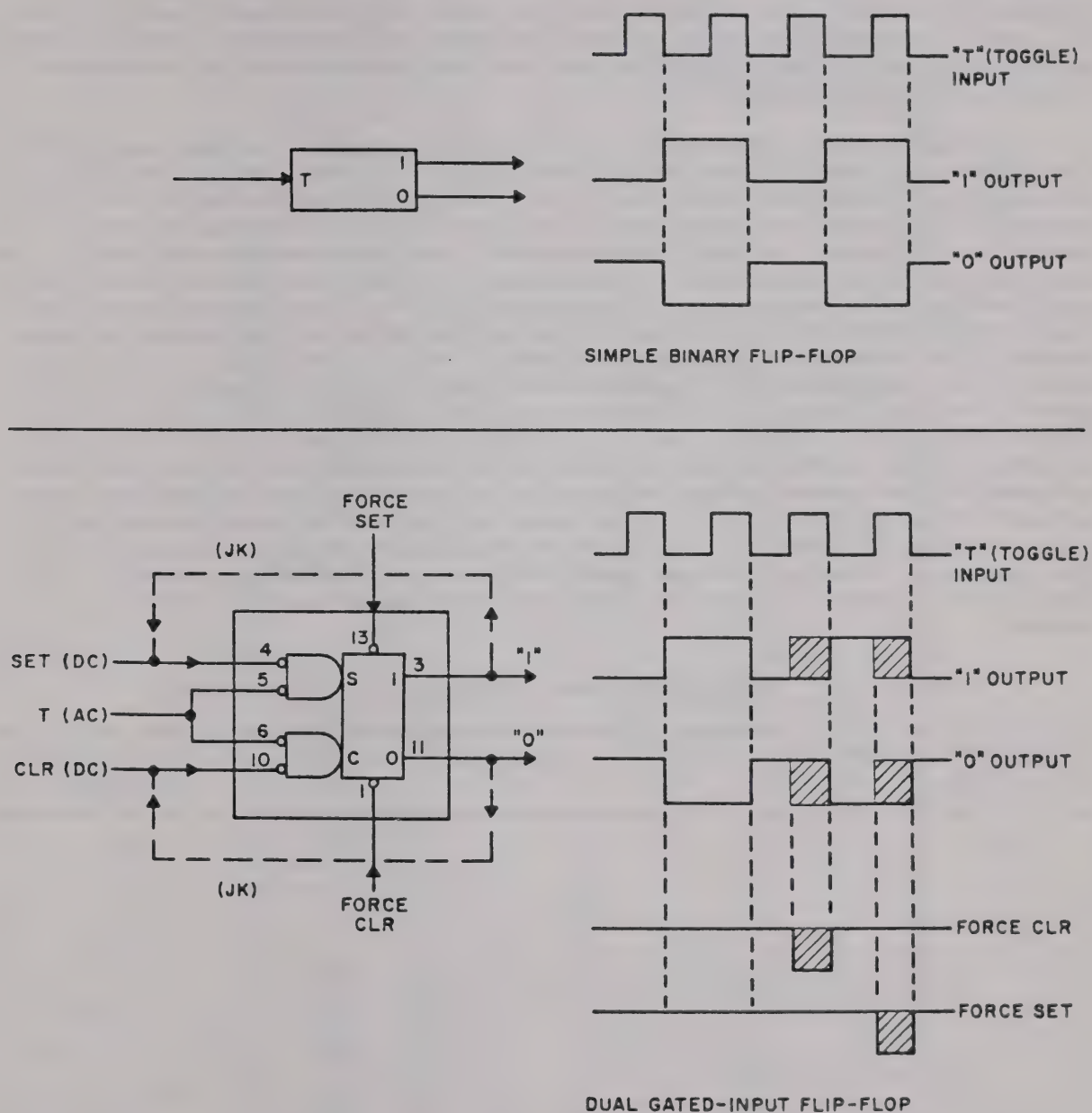


Figure 4-35. Comparison, Triggered Binary Flip-Flops

controlled by the 100 kc and mc tuning dials, "force" a counting cycle to obtain the variable division range from 352 to 73 in unit steps.

(b) Johnson Counter Operation. - Figure 4-36 shows a divide-by-five Johnson counter in combination with a JK flip-flop circuit to form a variable divide-by-ten counting circuit. This circuit configuration is used twice in the divide-by-N counter. Z4, Z9, Z10, and Z11 form the first circuit, and Z14, Z15, Z16, and Z17 the second circuit. The following circuit description applies to both circuits although it actually describes the first circuit operation and references the first circuit components.

The NAND control gates (p/o Z8 and Z12) will "force" a logical state at terminal 13 of each flip-flop when switch S5 is closed, or when a pulse simulating this condition is applied to enable the gates. When switches S1 thru S4 are closed, a logical "0" (ground) state is imposed. An open switch will "force" a logical "1" (open) at that flip-flop, but only when switch S5 is closed to enable the gates. Consequently, any or all gates can be programmed by setting switches S1 thru S4 for a preset action, to be implemented by closing switch S5. When the gates are disabled with switch S5 open, the complete circuit functions as a divide-by-ten binary counter. For every group of ten pulses applied to the input of Z4, a single pulse appears at the output of Z11. If switch S1 is opened to force a logical "1" at the output of Z4, the closing of switch S5 to enable the gates will cause division by a factor of nine instead of ten. The "forced" state at terminal 13 of Z4 has caused the divide-by-ten counter to skip a count. If the switch S5 function is performed by connecting the gate enabling circuit to the output of Z11, the counter will continuously divide-by-nine and the output pulse will preset the gates automatically. In this manner, the counting circuit can be programmed to divide by any factor from one to ten, simply by setting the appropriate gate switches S1 thru S4. The following list in table 4-3 gives the gate programming required to control the counter.

TABLE 4-3. VARIABLE ($\div 10$) COUNTER, PROGRAMMING

DIVISION FACTOR	SWITCH S1	SWITCH S2	SWITCH S3	SWITCH S4	FLIP-FLOP "FORCED"
$\div 10$	0	0	0	0	NONE
$\div 9$	1	0	0	0	Z4
$\div 8$	0	1	0	0	Z9
$\div 7$	1	1	0	0	Z4, Z9
$\div 6$	0	1	1	0	Z9, Z10
$\div 5$	1	1	1	0	Z4, Z9, Z10
$\div 4$	0	0	1	1	Z10, Z11
$\div 3$	1	0	1	1	Z4, Z10, Z11
$\div 2$	0	0	0	1	Z11
$\div 1$	1	0	0	1	Z4, Z11
Switch closed: Logical "0"; Switch open: Logical "1"					

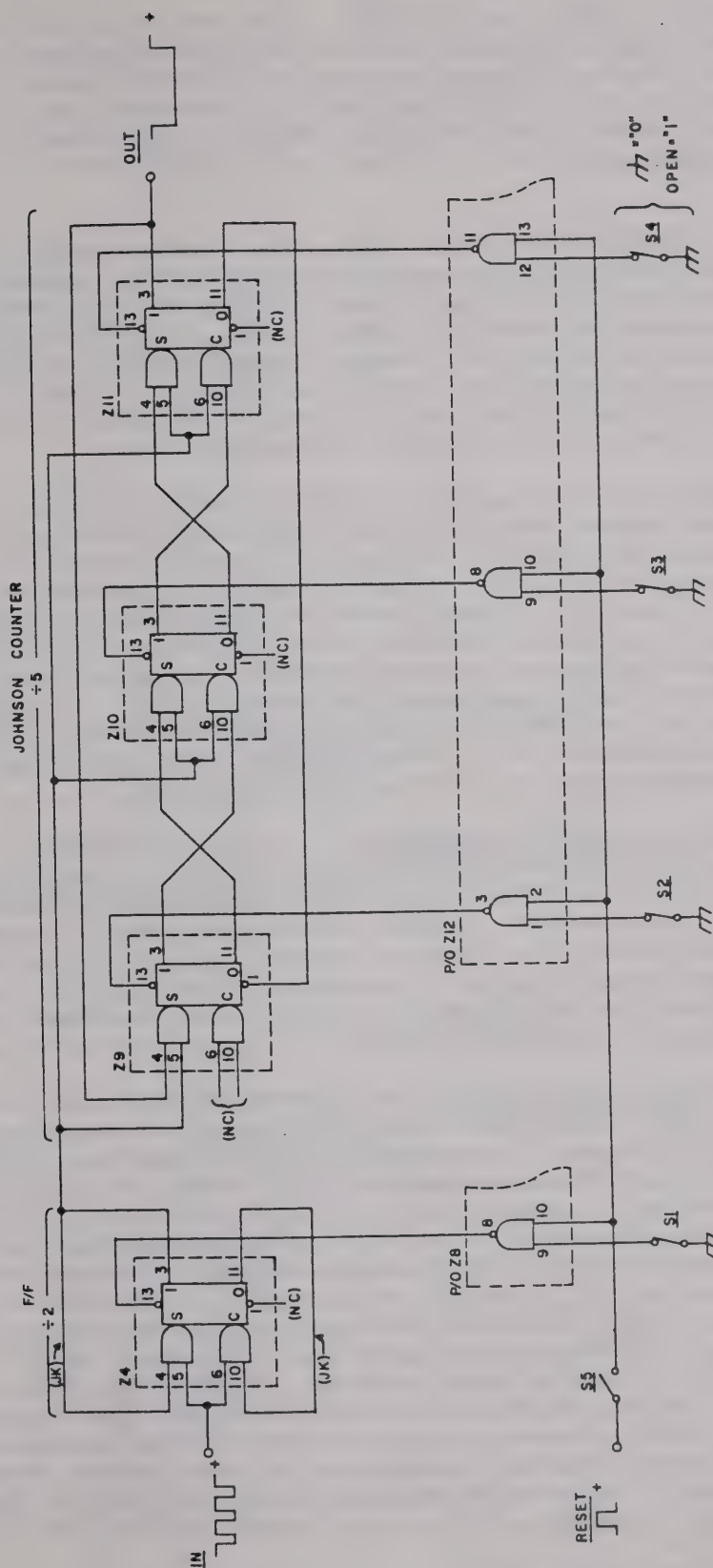


Figure 4-36. Variable Divide-by-Ten Counter, Functional Diagram

(2) INPUT VIDEO AMPLIFIER. - The input video amplifier circuit consists of direct-coupled stages Q1 and Q2, capacitively coupled to direct-coupled stages Q3 and Q4. Feedback from the emitter of Q4 to the base of Q3, via resistor R8, is incorporated to improve the amplifier high frequency response. The 35.200,000 to 7.300,000 mc input frequency, obtained from mixer Z1 (p/o A1A3A1), is derived by combining an 82 to 110 mc and a 117.300,000 to 117.200,100 mc frequency.

(3) FREQUENCY DIVIDER ($\div 8$). - The divide-by-eight frequency divider circuit consists of a high-speed flip-flop Q5 and Q6, emitter follower Q7, and two diode-transistor (micro-logic) gated flip-flop circuits contained in Z2 and Z3. An initial frequency division by a factor of two, from 17.600,000 to 3.650,000 mc, is performed by the Q5 and Q6 circuit. A final division by a factor of four for a total division factor of eight ($2 \times 4 = 8$) is performed by Z2 and Z3 to obtain a frequency of 4.400,000 to 0.912,500 mc. Z2 and Z3 are binary connected as JK flip-flop circuits to form a divide-by-two frequency divider.

(4) DIVIDE-BY-N VARIABLE FREQUENCY DIVIDER. - The divide-by-N (352 to 73) digital counter consists of the twelve diode-transistor (micro-logic) gated flip-flop circuits Z4 thru Z6, Z9 thru Z11, and Z14 thru Z19, and includes the quad-input dual gates Z7. The counter is controlled (preset) by the dual-input quad gates Z8, Z12, and Z13, which in turn are controlled by the 100 kc and mc tuning dials. Each input pulse supplied by the 4.400,000 to 0.912,500 mc pulse train to Z4 decreases the preset count factor by one count, until an output pulse is produced to reset the counter and repeat the counting cycle. For example, when the input frequency is 4.400,000 mc, a 12.5 kc output frequency represents a frequency division by a factor of 352. When the input frequency is 0.912,500 mc, a 12.5 kc output frequency represents division by a factor of 73.

(a) Description Terminology. - If the divide-by-N counter circuit employed a conventional binary register using a BCD (binary-coded-decimal) code, the circuit description could be directly related to the MEGACYCLES dials binary code given in table 4-1. Because the two divide-by-ten circuits employ a JK flip-flop followed by a divide-by-five Johnson counter ($2 \times 5 = 10$), the binary code is not conventional and cannot readily be converted to meaningful decimal numbers. Therefore, the circuit description will be related to the functional operation of the circuits concerned with a minimum reference to digital-circuit design factors.

(b) Mechanical Analogy. - Figure 4-37 is a basic block diagram of the divide-by-N counter circuit and includes a mechanical analogy which, although not identical in every respect, resembles the counting functions performed by the digital counting circuits. The two divide-by-ten blocks, followed by a single divide-by-four block, function in a manner very similar to the units, tens, and hundreds drums of the mechanical counter. The input pulse train is shown as controlling the counting rate (or speed of operation) in both instances. Whereas the control gates (governed by setting the 100 kc and mc tuning dials) set the count length for the binary dividers, the stop pawls shown in the analogy perform a similar function at the counter drums. When the control gates preset the count length or cycle, the stop pawls similarly preset the drum readings. Because the divide-by-N counter is a "count-down" device, the mechanical counter drums also "count-down" from the preset digits. Each successive input pulse of the train decreases the count by one digit, until a count is reached terminating the cycle and the counter is reset to repeat the procedure. The count termination is the equivalent of the 12.5 kc output frequency and represents division by a factor ranging from 352 to 73.

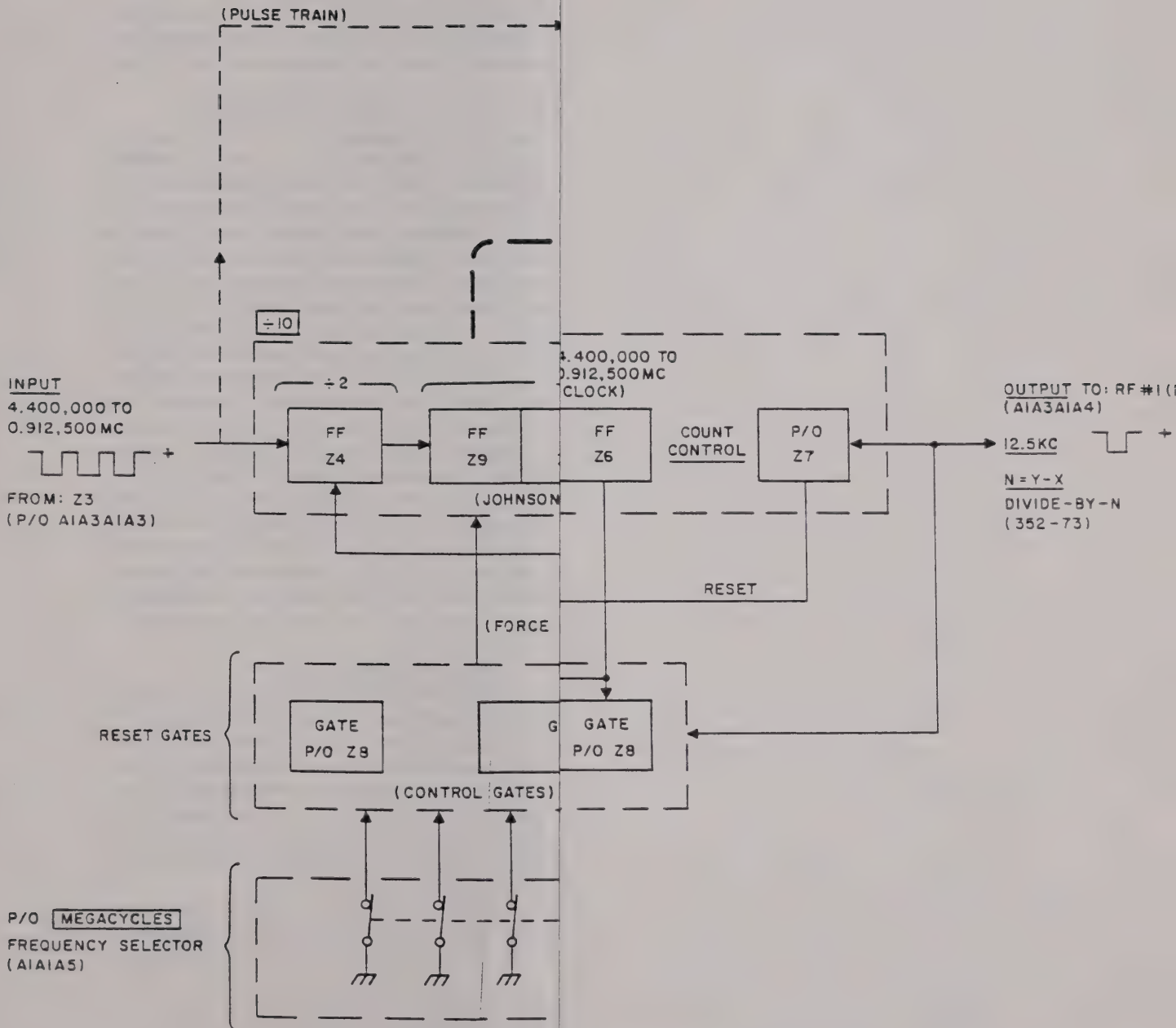


Figure 4-37. Digital #2 Divide-by-10 Counter, Mechanical Analogy

(2) INPUT VIDEO AMPLIFIER. - The input video amplifier circuit consists of direct-coupled stages Q1 and Q2, capacitively coupled to direct-coupled stages Q3 and Q4. Feedback from the emitter of Q4 to the base of Q3, via resistor R8, is incorporated to improve the amplifier high frequency response. The 35.200,000 to 7.300,000 mc input frequency, obtained from mixer Z1 (p/o A1A3A1), is derived by combining an 82 to 110 mc and a 117.300,000 to 117.200,100 mc frequency.

(3) FREQUENCY DIVIDER ($\div 8$). - The divide-by-eight frequency divider circuit consists of a high-speed flip-flop Q5 and Q6, emitter follower Q7, and two diode-transistor (micro-logic) gated flip-flop circuits contained in Z2 and Z3. An initial frequency division by a factor of two, from 17.600,000 to 3.650,000 mc, is performed by the Q5 and Q6 circuit. A final division by a factor of four for a total division factor of eight ($2 \times 4 = 8$) is performed by Z2 and Z3 to obtain a frequency of 4.400,000 to 0.912,500 mc. Z2 and Z3 are binary connected as JK flip-flop circuits to form a divide-by-two frequency divider.

(4) DIVIDE-BY-N VARIABLE FREQUENCY DIVIDER. - The divide-by-N (352 to 73) digital counter consists of the twelve diode-transistor (micro-logic) gated flip-flop circuits Z4 thru Z6, Z9 thru Z11, and Z14 thru Z19, and includes the quad-input dual gates Z7. The counter is controlled (preset) by the dual-input quad gates Z8, Z12, and Z13, which in turn are controlled by the 100 kc and mc tuning dials. Each input pulse supplied by the 4.400,000 to 0.912,500 mc pulse train to Z4 decreases the preset count factor by one count, until an output pulse is produced to reset the counter and repeat the counting cycle. For example, when the input frequency is 4.400,000 mc, a 12.5 kc output frequency represents a frequency division by a factor of 352. When the input frequency is 0.912,500 mc, a 12.5 kc output frequency represents division by a factor of 73.

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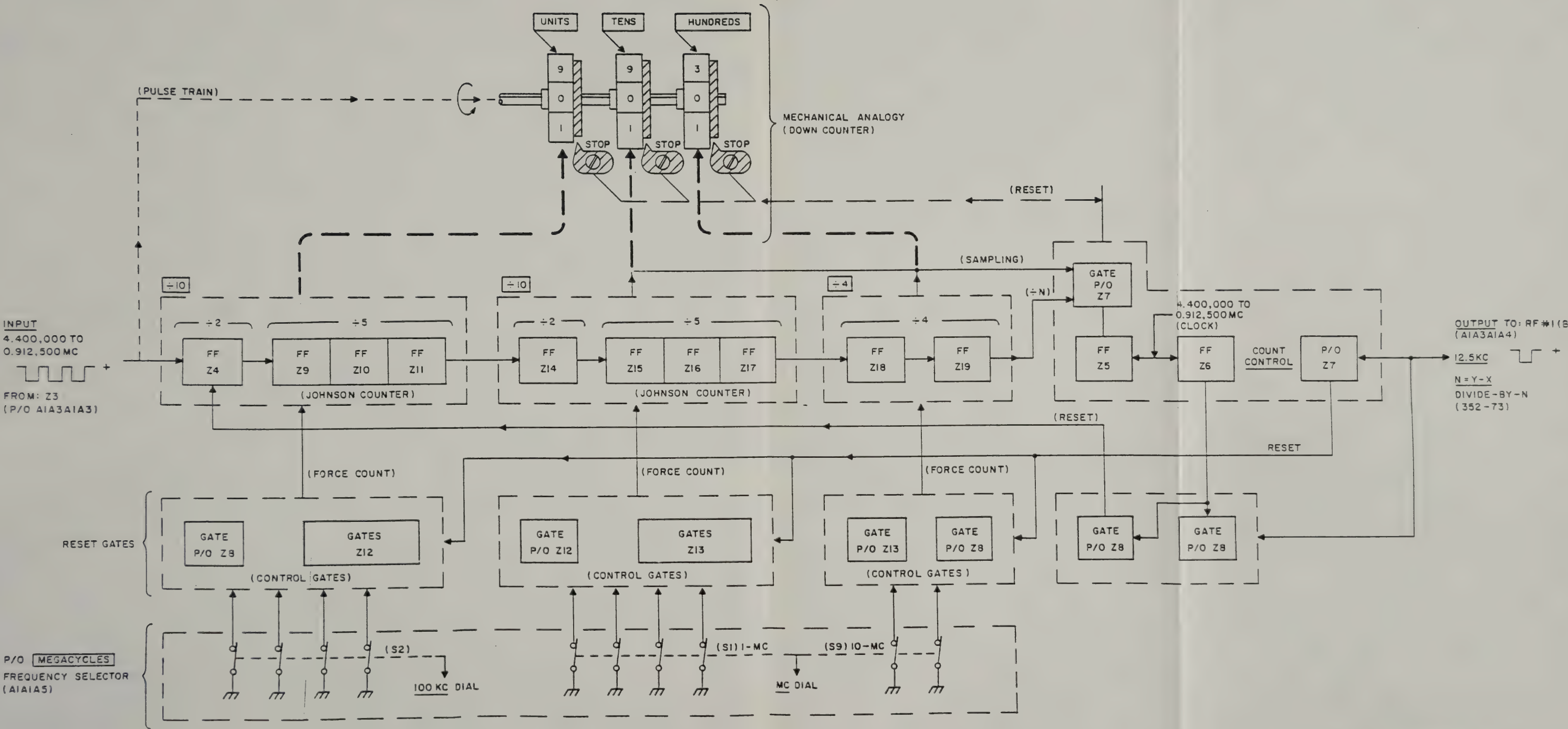


Figure 4-37. Digital #2 Divide-by-N Counter, Mechanical Analogy

(c) Counting Cycle. - The divide-by-N digital counter is a variable length "down-counter" with a counting cycle which follows the mathematical expression: $N = y - x$; where N is the count length or division factor, y is the preset (start) count determined by the tuning dial settings, and x is the end (stop) count producing a 12.5 kc output frequency. The first divide-by-ten block, controlled by the 100 kc tuning dial, counts in units. The second divide-by-ten block counts in tens and is controlled by the mc tuning dial. The divide-by-four block, also controlled by the mc tuning dials, counts in hundreds. Therefore, the tens block receives one counting pulse for each group of ten (or less) pulses applied to the units block by the input pulse train, and the hundreds block receives one pulse for every ten (or less) pulses applied to the tens block. The counter operation at this point is closely analogous to that of the mechanical three-drum counter illustrated in figure 4-37. Note that the hundreds drum contains the digits 0, 1, 2, and 3 only, corresponding to the 3 (hundreds) digits of the maximum division factor, 352.

A desired division factor is programmed by setting the 100 kc and the mc tuning dials. For example: A dial setting of 02.0 corresponds with the division factor 73 and a dial setting of 29.9 corresponds with the division factor 352. This is analogous to setting the mechanical counter drums for a reading of 370 or 253, respectively, reading from right to left. (Note that the division factor digits appear reversed at the counter drums to comply with the counting sequence of units, tens, and hundreds.) The counting cycle starts when a preset signal from the count-control block enables the control gates to insert the programmed division factor. Down-counting proceeds from the preset number until a 12.5 kc output is produced. The count control block again presets the counter and the cycle is repeated unless the tuning dials are reset for a different division factor. This action is analogous to the mechanical counter operation in the following manner: Mechanical counting starts when the preset signal from the count-control block releases the stop pawls, allowing the counter drums to operate. Down-counting progresses until the counter drums register 0, 0, 0. At this point, the count-control block signal activates the stop pawls to stop the drums and stop the counting process, preset the drums to the division factor reading, and release the drums to repeat the counting cycle. Although the mechanical counter can be described as "counting-down" to a 0, 0, 0 reading, the digital counter circuit "zero count" condition occurs when a 12.5 kc output pulse appears. At this precise point, the individual counting blocks will contain an arrangement of logical "0" and "1" states. Consequently, it is misleading to refer to a literally "zero" count state.

(d) Count Control. - The count-control block contains a five-input NAND gate (p/o Z7) and two dual gated-input flip-flops Z5 and Z6. The count control stops and resets the divide-by-N counter circuits (clears), presets the next count (division factor) by enabling the control gates, and initiates production of the 12.5 kc output pulse at the count termination. During the "count-down" cycle, the count control monitors the logical state of the counting process at the outputs of flip-flops Z14, Z15, Z16, Z18, and Z19. When the "zero-count" conditions appear at the end of a count cycle, the count control performs the stop, reset, and preset functions accompanied by the production of a 12.5 kc output pulse.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the digital #2 card before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in card in its compartment.
- (2) Cable connections (if any) attached to the module.

c. TEST EQUIPMENT. - Not applicable.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figure 5-38.) - No external test points are provided at the digital #2 card. Therefore, trouble shooting is performed by repeating the test data steps for the rf #1(A) card A1A3A1A1. Satisfactory completion of these tests assures normal performance of the digital #2 card (see paragraph 4-19e).

4-22. RF #3, A1A3A1A2. (See figures 4-38 and 4-39.)

The rf #3 card contains a divide-by-twelve digital frequency divider, a dc ramp generator and phase detector, a voltage controlled vhf oscillator (vco), and the oscillator phase-locking loop circuit. The vco output frequency ranges from 117.300,000 to 117.200,100 mc. These circuits generate and control the vhf output frequency applied to the digital #2 card A1A3A1A3, via mixer Z1 (p/o A1A3A1). Faulty operation of this circuit can prevent reception completely.

a. DESCRIPTION. - The vhf output from the rf #3 card is determined by the frequency and phase relation between two frequencies: a variable frequency range from 32.400,000 to 33.598,800 mc, reduced to a range from 2.700,000 to 2.799,900 mc by the divide-by-twelve frequency divider circuit, and a variable frequency range from 2.700,000 to 2.799,900 mc obtained by combining the vco output frequency with a fixed 120 mc frequency supplied from the X4 multiplier A1A3A1Z2. The dc varactor-control voltage governing the vco output frequency is derived from the dc ramp generator and phase detector circuits. When the vco output frequency corresponds with a particular frequency from the divide-by-twelve frequency divider, the vco is "locked" at that operating frequency.

(1) DIVIDE-BY-TWELVE FREQUENCY DIVIDER. - The divide-by-twelve frequency dividing circuit consists of a high-speed ($\div 2$) flip-flop Z1, direct coupled amplifier Q1 and Q2, a ($\div 2$) flip-flop Z2, a ($\div 3$) circuit using flip-flops Z3 and Z4, and a direct-coupled amplifier Q3. The 32.400,000 to 33.598,800 mc frequency range supplied by the rf #2 card A1A3A1A5 is reduced to a 2.700,000 to 2.799,900 mc range by this circuit prior to application at the phase detector Z5.

The high-speed flip-flop Z1, a micro-logic component, is essentially a negative logic element. Therefore, grounding certain terminal connections will provide the equivalent of a JK flip-flop circuit to be triggered as a binary frequency-divider by the "clock" pulses applied at terminals 6 and 8 (see paragraph 4-21a(1)). The frequency range from 16.200,000 to 16.799,400 mc at the output of Z1 is amplified by a direct-coupled amplifier consisting of Q1 and Q2 prior to application at the divide-by-two JK flip-flop Z2. Output from Z2, a frequency range from 8.100,000 to 8.399,700 mc, goes to a "short-count" divide-by-three frequency divider consisting of flip-flops Z3 and Z4. The "short-count" connections provide frequency division by a factor of three rather than the normal division-by-four obtained when two binary flip-flops are connected in series. Amplifier Q3 applies the resultant frequency range from 2.799,900 to 2.700,000 mc to one input of the phase detector Z5.

(2) RAMP GENERATOR AND PHASE DETECTOR. - This circuit consists of phase detector Z5, a band-rejection filter formed by L1 and C11 thru C13, and the ramp generator circuit employing Q4, Q5, and CR1. The phase detector Z5 uses a diode balanced-modulator circuit. The dc output voltage amplitude and polarity is determined by the frequency relation between the two input frequencies,

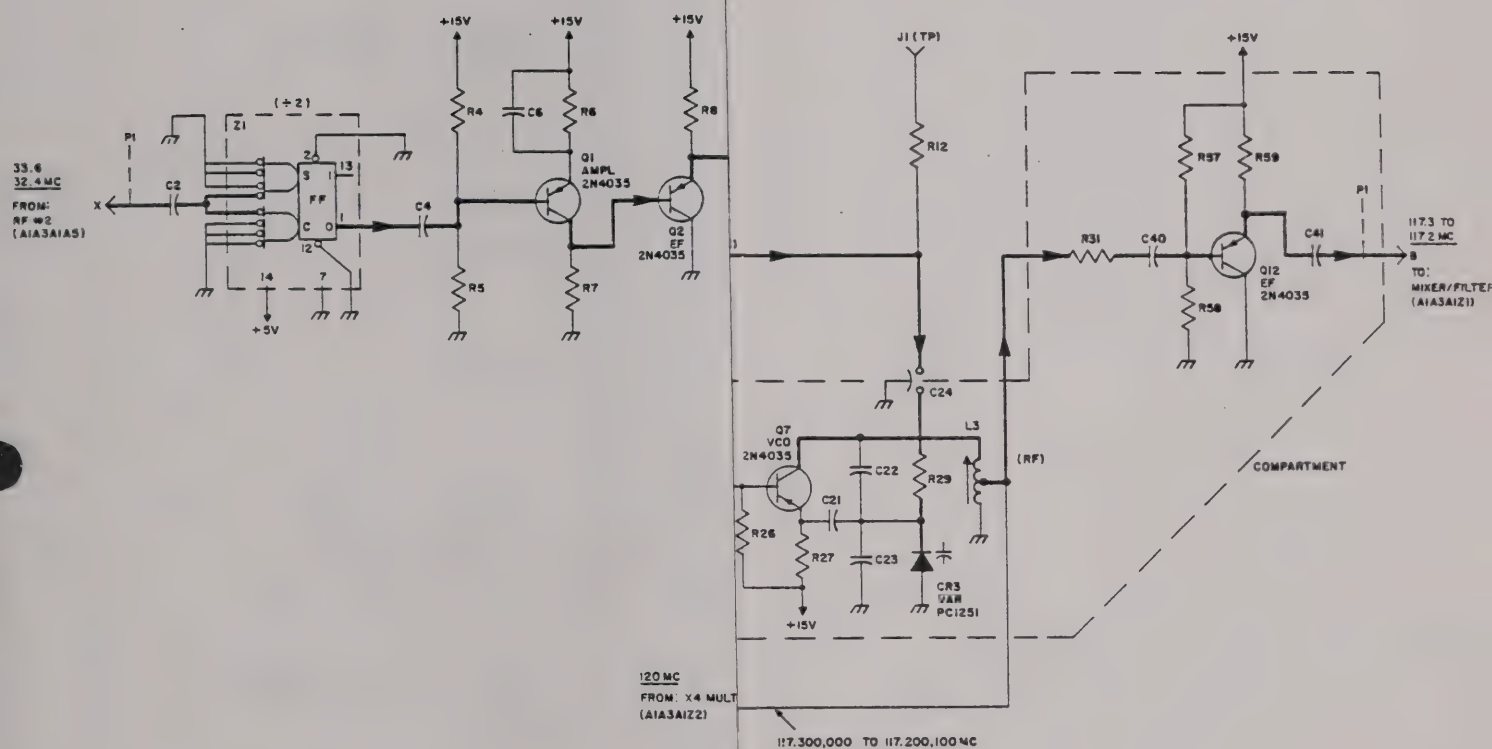


Figure 4-38. RF #3 A1A3A1A2,
Simplified Schematic Diagram

c. TEST EQUIPMENT. - Not applicable.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figure 5-38.) - No external test points are provided at the digital #2 card. Therefore, trouble shooting is performed by repeating the test data steps for the rf #1(A) card A1A3A1A1. Satisfactory completion of these tests assures normal performance of the digital #2 card (see paragraph 4-19e).

4-22. RF #3, A1A3A1A2. (See figures 4-38 and 4-39.)

The rf #3 card contains a divide-by-twelve digital frequency divider, a dc ramp generator and phase detector, a voltage controlled vhf oscillator (vco), and the oscillator phase-locking loop circuit. The vco output frequency ranges from 117.300,000 to 117.200,100 mc. These circuits generate and control the vhf output frequency applied to the digital #2 card A1A3A1A3, via mixer Z1 (p/o A1A3A1). Faulty operation of this circuit can prevent reception completely.

a. DESCRIPTION. - The vhf output from the rf #3 card is determined by the frequency and phase relation between two frequencies: a variable frequency range from 32.400,000 to 33.598,800 mc, reduced to a range from 2.700,000 to 2.799,900 mc by the divide-by-twelve frequency divider circuit, and a variable frequency range from 2.700,000 to 2.799,900 mc obtained by combining the vco output frequency with a fixed 120 mc frequency supplied from the X4 multiplier A1A3A1Z2. The dc varactor-control voltage governing the vco output frequency is derived from the dc ramp generator and phase detector circuits. When the vco output frequency corresponds with a particular frequency from the divide-by-twelve frequency divider, the vco is "locked" at that operating frequency.

(1) DIVIDE-BY-TWELVE FREQUENCY DIVIDER. - The divide-by-twelve frequency dividing circuit consists of a high-speed ($\div 2$) flip-flop Z1, direct coupled amplifier Q1 and Q2, a ($\div 2$) flip-flop Z2, a ($\div 3$) circuit using flip-flops Z3 and Z4, and a direct-coupled amplifier Q3. The 32.400,000 to 33.598,800 mc frequency range supplied by the rf #2 card A1A3A1A5 is reduced to a 2.700,000 to 2.799,900 mc range by this circuit prior to application at the phase detector Z5.

The high-speed flip-flop Z1, a micro-logic component, is essentially a negative logic element. Therefore, grounding certain terminal connections will provide the equivalent of a JK flip-flop circuit to be triggered as a binary frequency-divider by the "clock" pulses applied at terminals 6 and 8 (see paragraph 4-21a(1)). The frequency range from 16.200,000 to 16.799,400 mc at the output of Z1 is amplified by a direct-coupled amplifier consisting of Q1 and Q2 prior to application at the divide-by-two JK flip-flop Z2. Output from Z2, a frequency range from 8.100,000 to 8.399,700 mc, goes to a "short-count" divide-by-three frequency divider consisting of flip-flops Z3 and Z4. The "short-count" connections provide frequency division by a factor of three rather than the normal division-by-four obtained when two binary flip-flops are connected in series. Amplifier Q3 applies the resultant frequency range from 2.799,900 to 2.700,000 mc to one input of the phase detector Z5.

(2) RAMP GENERATOR AND PHASE DETECTOR. - This circuit consists of phase detector Z5, a band-rejection filter formed by L1 and C11 thru C13, and the ramp generator circuit employing Q4, Q5, and CR1. The phase detector Z5 uses a diode balanced-modulator circuit. The dc output voltage amplitude and polarity is determined by the frequency relation between the two input frequencies,

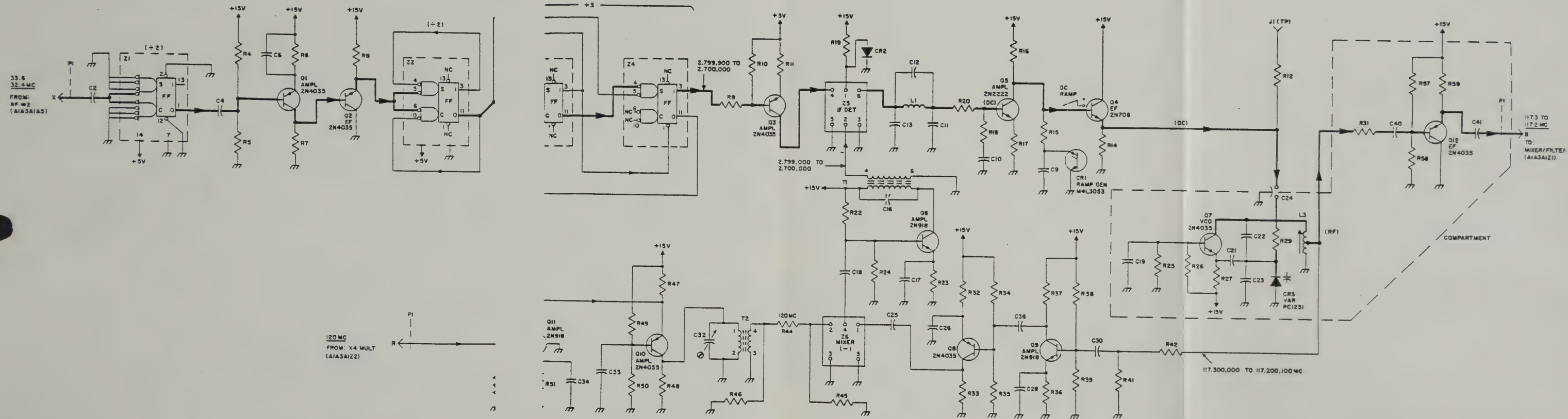


Figure 4-38. RF #3 A1A3A1A2,
Simplified Schematic Diagram

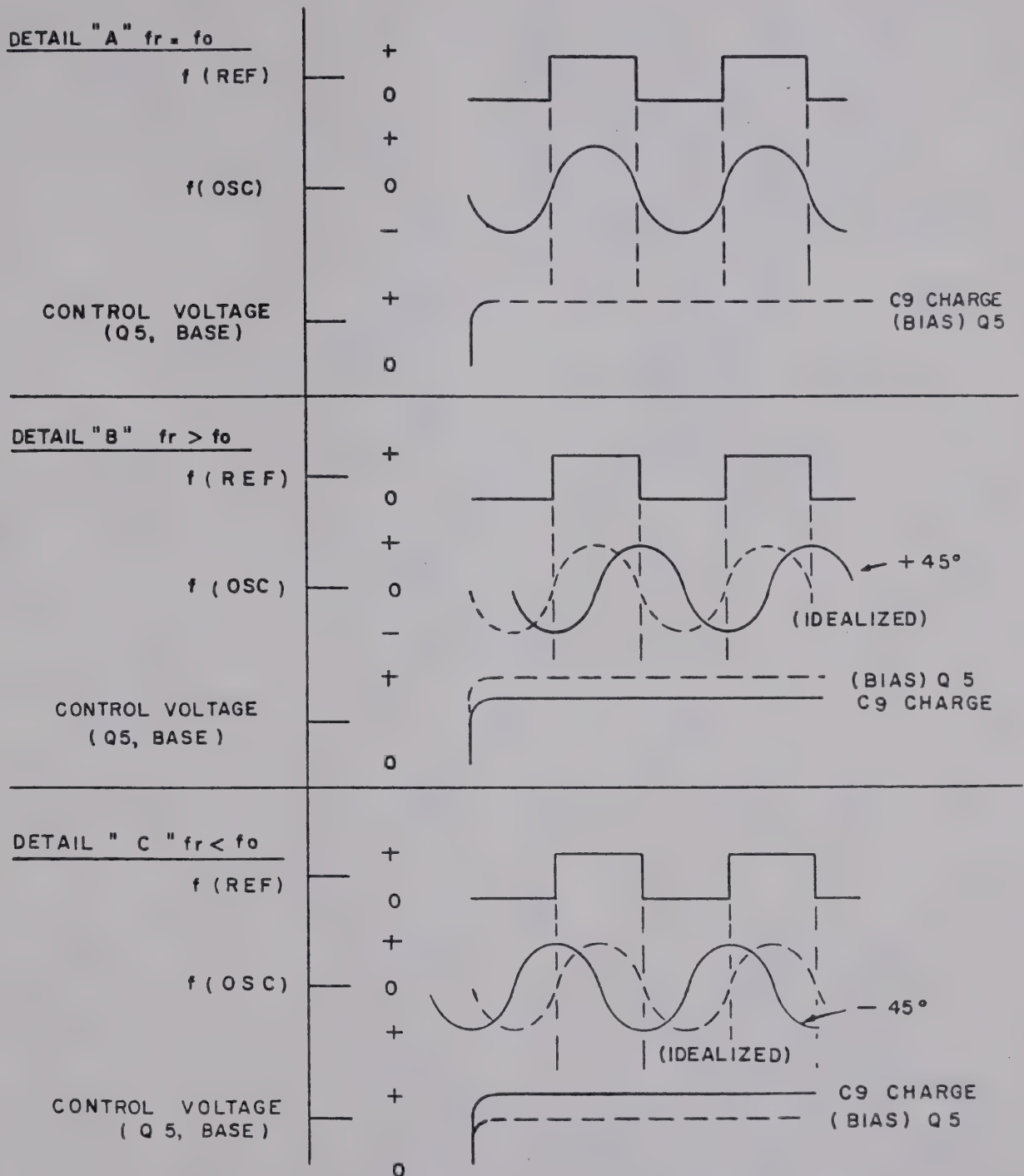


Figure 4-39. Timing Diagram, Phase Detector Operation

one from amplifier Q3 and the other from transformer T1. Phase detector output goes through the 3 mc band rejection filter to the ramp generator, the filter rejecting signal components contributed by the detection process. The base of Q5 receives the phase-detector output voltage, combined with a fixed bias voltage supplied via terminal 1 of Z5. Consequently, the Q5 input signal is the algebraic sum of these two voltages. Q5 and Q4 form a high-gain amplifier stage followed by an emitter follower with the PNP diode CR1 functioning as the actual ramp generator. When the ramp charge at capacitor C9 reaches the "break-point" of diode CR1, the diode conducts to quickly discharge C9 ending the dc ramp. Actually, the complete dc ramp voltage will not be present unless one of the two input frequencies to the rf #3 card is omitted. During normal circuit operation, the vco Q7 is controlled over its entire frequency range without reaching the varactor control-voltage "break-point" at diode CR1.

Figure 4-39 is a timing diagram showing three typical phase detector operating conditions. These are: A "null" condition when the reference frequency (f_r) from amplifier Q3, and the vco frequency (f_o) via transformer T1 (following a conversion by the fixed 120 mc frequency at mixer Z6), coincide to "lock" the vco Q7 at its operating frequency; a condition when f_r is higher and lags f_o by an instantaneous 45 degrees; and a condition when f_r is lower and leads f_o by 45 degrees. Phase detector Z5 operation can be compared to that of a switching circuit where f_r determines the switching rate, and f_o appears at the detector output only when the f_r and f_o frequencies coincide or approach coincidence. In this manner, the dc phase detector output-voltage polarity and amplitude is dependent upon the phase relation of f_r and f_o .

Detail "A" illustrates a phase detector "null" condition when the vco is "locked". The detector dc output is zero and the varactor-control voltage consists of the fixed bias at the base of Q5 which is amplified and applied to the vco circuit via resistor R29. Actually, a "null" condition occurs with a small level of phase detector output-voltage present, representing a circuit balance between the control-signal path and the phase-locking loop return path via transformer T1.

Detail "B" shows the derivation of the varactor-control voltage when $f_r > f_o$. The 45 degree (instantaneous) phase detector output-voltage which, when combined with the fixed bias voltage at the base of Q5, reduces the charge at capacitor C9 to decrease the vco operating frequency. The vco will "lock" at a new frequency with $f_r = f_o$.

Detail "C" shows the varactor-control voltage derivation when $f_r < f_o$. The phase detector now produces a positive output voltage which combines with the fixed bias at the base of Q5 to raise the varactor-control voltage and increase the vco operating frequency. It is apparent that the varactor-control voltage first appears at the base of Q5, is amplified by Q5, and occurs as a charged condition at capacitor C9. Emitter follower Q4 serves as an isolation stage to couple the control voltage to the vco circuit.

(3) PHASE-LOCKING LOOP. - The phase-locking loop circuit consists of amplifier Q10 and Q11, mixer Z6 with amplifier Q6, and amplifier Q8 and Q9. The mixer combines an amplified 120 mc fixed frequency from the mixer/multiplier module A1A3A2 with an amplified sample of the vco Q7 output frequency. The difference frequency from the mixer output is applied to phase detector Z5 via transformer T1 to supply the required f_o input frequency for phase detector operation.

A fixed 120 mc frequency from the mixer/multiplier module is amplified by cascode amplifier Q11 and Q10 and applied to one input of mixer Z6 via transformer T2. The primary of T2 is tuned to 120 mc by variable capacitor C32. A sample of the vco output frequency range of 117.200,100 to 117.300,000 mc is amplified by the video-type amplifier Q9 and Q8, and applied to the second mixer Z6 input circuit. Mixer Z6 employs a diode balanced-modulator circuit and the resultant difference frequency range from 2.700,000 to 2.799,900 mc is amplified by Q6 and applied to transformer T1 for coupling to the phase detector Z5. Because the fixed 120 mc input frequency is derived from the 3 mc frequency standard module A1A1A1 output, the phase-locking loop frequency at transformer T1 appears as a direct function of the vco Q7 operating frequency.

(4) VCO AND OUTPUT AMPLIFIER. - The vco circuit consists of the voltage-controlled oscillator Q7 and output amplifier Q12. Vco output frequencies are applied to the phase-locking loop circuit via amplifier Q9 and Q8, and to the mixer/filter A1A3A1Z1 via output amplifier Q12.

The vhf voltage-controlled oscillator Q7 employs a modified Colpitts circuit. The tank circuit is formed by inductor L3 and tuned by the series capacitors C22 and C23. Dc varactor-control voltage is applied to varactor CR3 which is in parallel with capacitor C23, and the oscillator is tuned by the control voltage which ranges from approximately 4.5 to 4.8 volts dc for an oscillator output frequency range from 117.2 to 117.3 mc, respectively. Oscillator output is obtained at a low-impedance tap on inductor L3.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the rf #3 card before beginning trouble shooting, with emphasis on the following:

- (1) Seating of plug-in card in its compartment.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use VTVM AN/USM-116, or equivalent. No special tools are required.

d. CONTROL SETTING. - Set controls according to table 3-2. During the test procedure, adjust the 10 kc tuning dial (p/o A1A1A5) as directed.

e. TEST DATA. (See figure 5-39.) - Trouble shooting the rf #3 card consists of measuring the dc varactor-control voltage at a test point provided, for several settings of the 10 kc tuning dial. Perform the following:

- (1) Connect dc VTVM to test point J1(TP) on the rf #3 card.
- (2) Set the 10 kc dial at 0 and note the VTVM reading. It should be approximately 4.5 volts dc.
- (3) Set the 10 kc dial at 9 and note the VTVM reading. It should be approximately 4.3 volts.
- (4) Note the change in VTVM reading when the 10 kc dial setting is changed. Although the dc voltage will change approximately 0.2 volt, this change may not be perceptible at the VTVM, except as a small flick of the meter pointer.

4-23. RF #2, A1A3A1A5. (See figures 4-40 thru 4-42.)

The rf #2 card contains a dc ramp generator, a digital phase-detector, a digital frequency-discriminator, and a voltage-controlled vhf oscillator with an output frequency range from 32,400,000 to 33,598,800 mc. These circuits generate and control the vhf output frequencies applied at the rf #3 card A1A3A1A2. Faulty operation of this card can prevent reception completely.

a. DESCRIPTION. - The vhf output from the rf #2 card is determined by the frequency and phase relation between two input frequencies. A fixed 1.2 kc (reference) frequency from the digital #1 card A1A3A1A7, in the form of a negative-going pulse train, and a variable 1.2 kc (Δf) frequency from the digital #3 card A1A3A1A6, also a negative-going pulse train. The vhf output frequency from the voltage-controlled oscillator (vco) is controlled by a dc varactor-control voltage developed by the digital phase-detector as a function of the frequency relation between the 1.2 kc reference frequency and the 1.2 kc Δf frequency. When these two frequencies coincide, the control voltage "locks" the vco circuit.

The vco control voltage is developed by a dc ramp generator (Q1 and Q2) and processed by a digital phase-detector (Q6) under the control of the digital frequency-discriminator (Z2 thru Z6). Direct coupled amplifier stages (Q3, Q4, and Q7, Q8) provide circuit isolation, and the dc control voltage goes through a 1.2 kc twin "T" filter followed by an emitter-follower stage (Q9) prior to application at the vco (Q12) circuit. A dc complementary amplifier (Q13 and Q14) provides amplification at the circuit output. To supply voltage, regulating circuits are incorporated: current regulator (Q5) supplies operating current for amplifier stages (Q3 and Q4), and voltage regulator (Q10 and Q11) supplies operating voltage to stages (Q12, Q13, and Q14).

(1) DIGITAL DISCRIMINATOR. - The digital discriminator circuit consists of the dual-input quad NAND gates Z2, Z3, and Z6, and the triple-input NAND gates Z4 and Z5. It supplies a "hold" pulse to ramp generator Q2, and a "sample" pulse to the digital phase detector Q6, via buffer Z1-6 and pulse transformer T2. A "dump" pulse to discharge the ramp storage capacitor C3 is supplied from one of the dual buffers (p/o Z1) via pulse transformer T1. The digital discriminator controls the application of the "hold", "sample", and "dump" pulses to obtain a vco varactor-control voltage derived from the frequency relation between the 1.2 kc reference frequency (f_r) and the 1.2 kc variable (Δf) frequency. Figure 4-41 is a timing diagram for the digital discriminator circuit showing three typical operating conditions. These are: a condition when Δf is lower in frequency than f_r , a condition when Δf is higher in frequency than f_r , and a condition when Δf and f_r are in frequency coincidence, locking the vco Q12.

Detail A shows the varactor-control voltage derived at capacitor C5 when a "sampling" pulse is applied at the phase detector Q6, sampling a portion of the dc ramp voltage originating at capacitor C3. Because $\Delta f < f_r$, the varactor-control voltage is increasing to cause the vco Q12 output frequency to increase, note that the charge at C5 is increasing for each "sampling" performed, providing a coarse tuning function.

Detail B shows the varactor-control voltage derived at capacitor C26 when $\Delta f > f_r$. For this operating condition, the "hold" and "dump" functions are shown which, although they occur prior to "sampling" at the phase detector Q6, influence the charge at capacitor C5 in the manner shown. Note that the vco varactor-control voltage is decreasing to lower the frequency generated by the vco Q12, and to perform a coarse-tuning function.

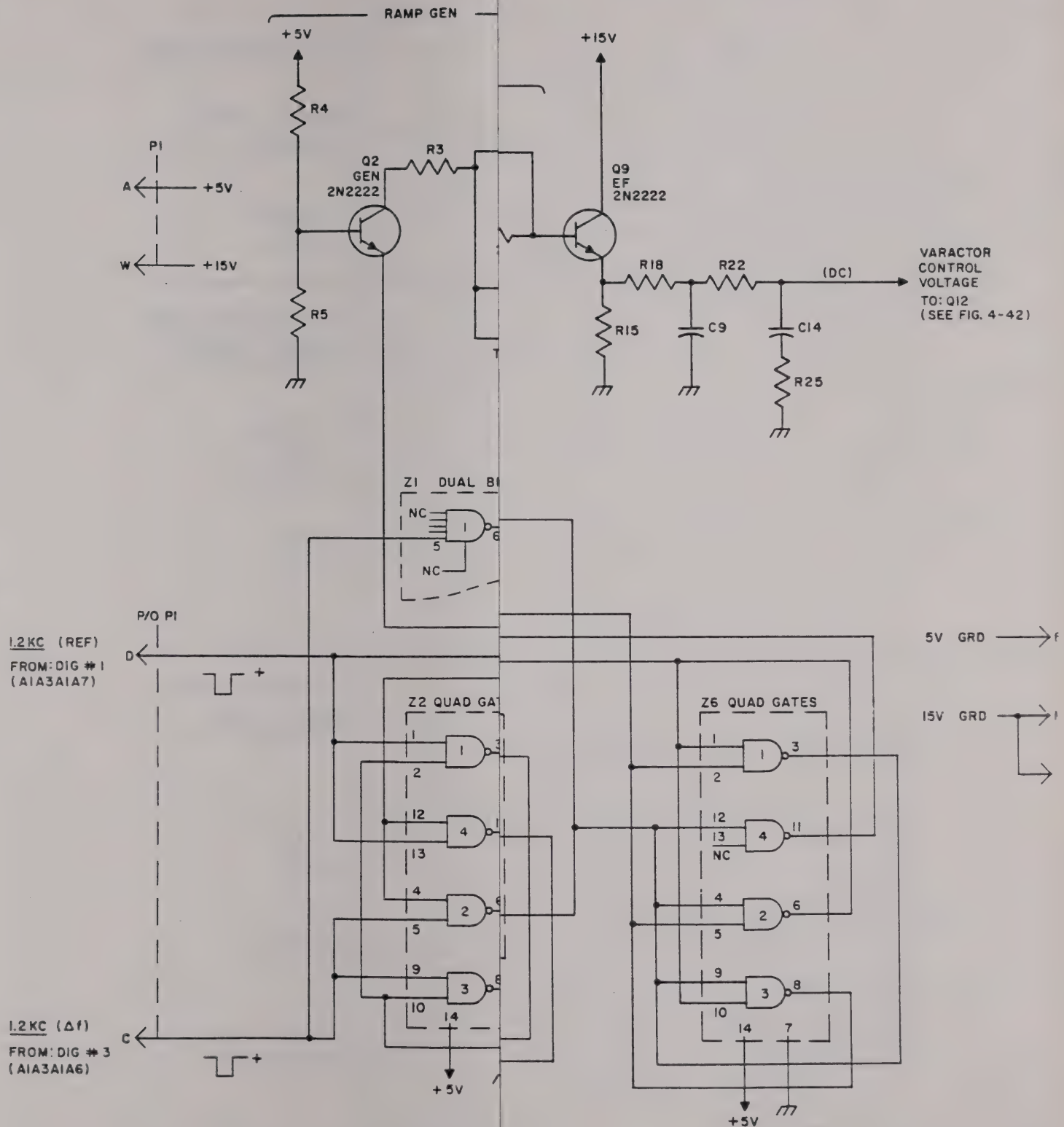


Figure 4-40. RF #2 A1A3A1A5,
Simplified Schematic Diagram

4-23. RF #2, A1A3A1A5. (See figures 4-40 thru 4-42.)

The rf #2 card contains a dc ramp generator, a digital phase-detector, a digital frequency-discriminator, and a voltage-controlled vhf oscillator with an output frequency range from 32,400,000 to 33,598,800 mc. These circuits generate and control the vhf output frequencies applied at the rf #3 card A1A3A1A2. Faulty operation of this card can prevent reception completely.

a. DESCRIPTION. - The vhf output from the rf #2 card is determined by the frequency and phase relation between two input frequencies. A fixed 1.2 kc (reference) frequency from the digital #1 card A1A3A1A7, in the form of a negative-going pulse train, and a variable 1.2 kc (Δf) frequency from the digital #3 card A1A3A1A6, also a negative-going pulse train. The vhf output frequency from the voltage-controlled oscillator (vco) is controlled by a dc varactor-control voltage developed by the digital phase-detector as a function of the frequency relation between the 1.2 kc reference frequency and the 1.2 kc Δf frequency. When these two frequencies coincide, the control voltage "locks" the vco circuit.

The vco control voltage is developed by a dc ramp generator (Q1 and Q2) and processed by a digital phase-detector (Q6) under the control of the digital frequency-discriminator (Z2 thru Z6). Direct coupled amplifier stages (Q3, Q4, and Q7, Q8) provide circuit isolation, and the dc control voltage goes through a 1.2 kc twin "T" filter followed by an emitter-follower stage (Q9) prior to application at the vco (Q12) circuit. A dc complementary amplifier (Q13 and Q14) provides amplification at the circuit output. To supply voltage, regulating circuits are incorporated: current regulator (Q5) supplies operating current for amplifier stages (Q3 and Q4), and voltage regulator (Q10 and Q11) supplies operating voltage to stages (Q12, Q13, and Q14).

(1) DIGITAL DISCRIMINATOR. - The digital discriminator circuit consists of the dual-input quad NAND gates Z2, Z3, and Z6, and the triple-input NAND gates Z4 and Z5. It supplies a "hold" pulse to ramp generator Q2, and a "sample" pulse to the digital phase detector Q6, via buffer Z1-6 and pulse transformer T2. A "dump" pulse to discharge the ramp storage capacitor C3 is supplied from one of the dual buffers (p/o Z1) via pulse transformer T1. The digital discriminator controls the application of the "hold", "sample", and "dump" pulses to obtain a vco varactor-control voltage derived from the frequency relation between the 1.2 kc reference frequency (f_r) and the 1.2 kc variable (Δf) frequency. Figure 4-41 is a timing diagram for the digital discriminator circuit showing three typical operating conditions. These are: a condition when Δf is lower in frequency than f_r , a condition when Δf is higher in frequency than f_r , and a condition when Δf and f_r are in frequency coincidence, locking the vco Q12.

Detail A shows the varactor-control voltage derived at capacitor C5 when a "sampling" pulse is applied at the phase detector Q6, sampling a portion of the dc ramp voltage originating at capacitor C3. Because $\Delta f < f_r$, the varactor-control voltage is increasing to cause the vco Q12 output frequency to increase, note that the charge at C5 is increasing for each "sampling" performed, providing a coarse vco tuning function.

Detail B shows the varactor-control voltage derived at capacitor C26 when $\Delta f > f_r$. For this operating condition, the "hold" and "dump" functions are shown which, although they occur prior to "sampling" at the phase detector Q6, influence the charge at capacitor C5 in the manner shown. Note that the vco varactor-control voltage is decreasing to lower the frequency generated by the vco Q12, and to perform a coarse-tuning function.

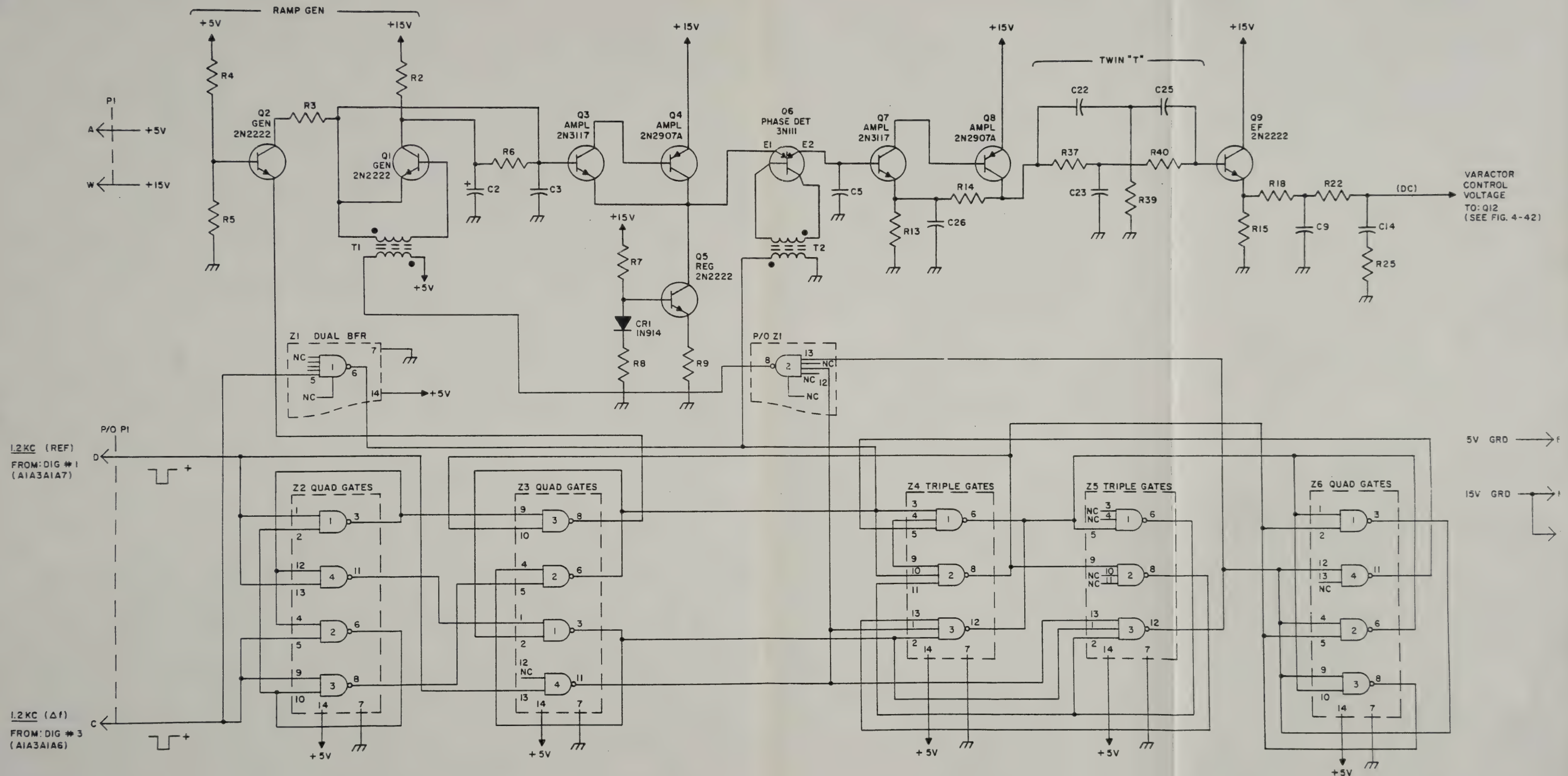


Figure 4-40. RF #2 A1A3A1A5,
Simplified Schematic Diagram

ORIGINAL

4-113/4-114

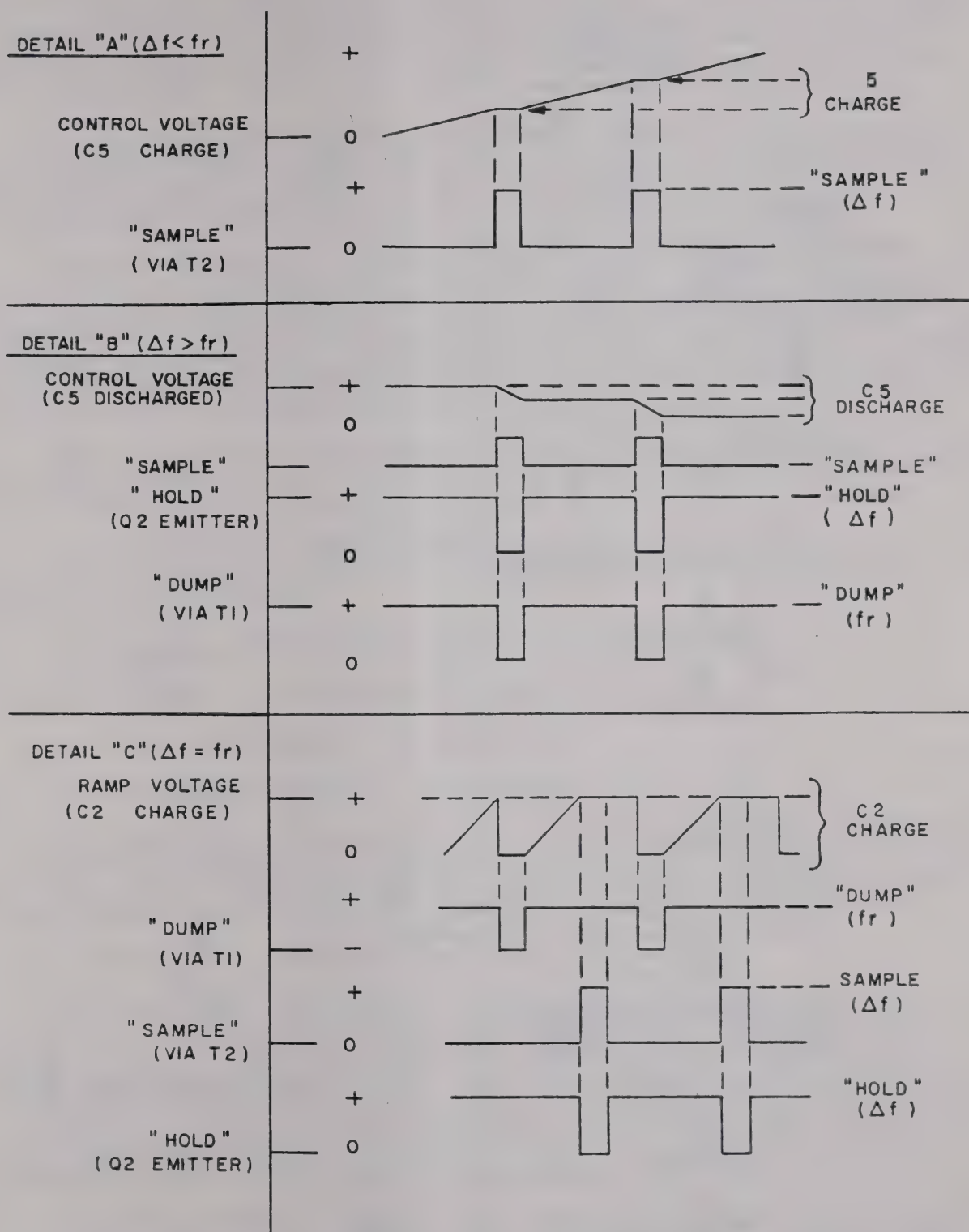


Figure 4-41. RF #2 Timing Diagram, Digital Discriminator

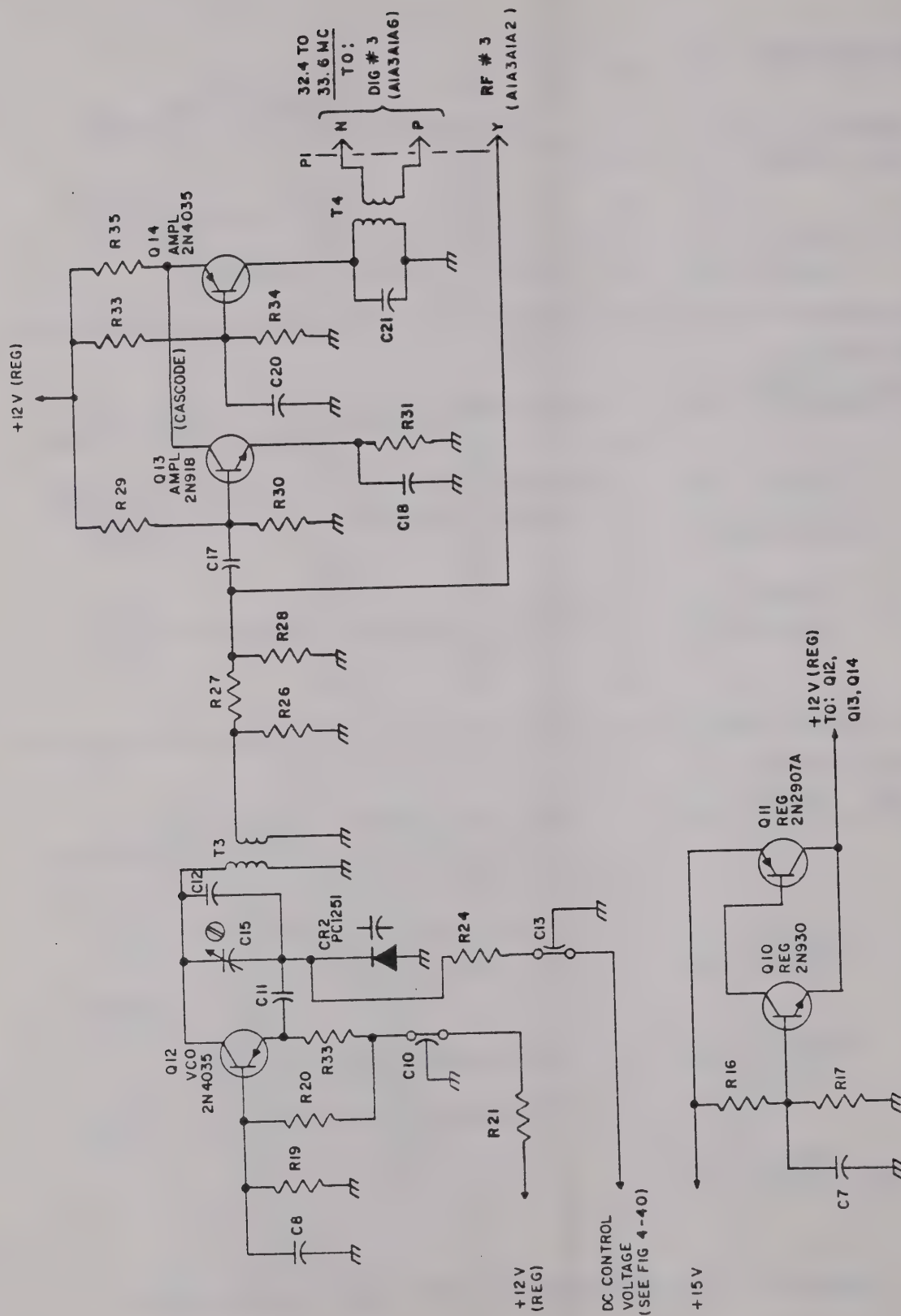


Figure 4-42. RF #2, VCO and Output Amplifier, Simplified Schematic Diagram

Detail C shows the varactor-control voltage at capacitor C5 when $\Delta f = f_r$ to "lock" the vco Q12. Again, the "hold" and "dump" functions pertain specifically to the ramp generator circuit, but the influence upon the capacitor C5 charge status is shown to illustrate the "sample" pulse application at the phase detector Q6. Actually, this operation of the phase detector performs a fine-tuning function to "lock" the vco Q12.

(2) VCO AND OUTPUT AMPLIFIER. - This circuit section consists of the vco Q12, the output amplifier Q13 and Q14, and the +12 volt dc regulating circuit using Q10 and Q11. The dc varactor-control voltage derived in the previous circuit sections is applied to the vco Q12, to govern its output frequency.

The vco Q12 is used in a modified Colpitts circuit, varactor controlled. The tank circuit is formed by the primary of transformer T3, tuned by capacitors C15 and C12 in series with varactor CR2. A dc varactor-control voltage, applied to CR2 via resistor R24, governs the oscillator frequency over its range from 32.400,000 to 33.598,800 mc. Transformer T3 couples the vco output to a cascode output amplifier using the complementary stages Q13 and Q14. Transformer T4 couples the amplifier output to the digital #3 card A1A3A1A6.

The vco Q12 and amplifier stages Q13 and Q14 receive operating power from a dc regulator formed by Q10 and Q11. During the regulating process, the original +15 volt supply potential is reduced to +12 volts dc.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the rf #2 card before beginning trouble shooting, with emphasis on the following:

- (1) Seating of the plug-in module in its compartment.
- (2) Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Not applicable.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figure 5-40.) - No external test points are provided at the rf #2 card. Therefore, trouble shooting is performed by repeating the test data steps for the rf #3 card A1A3A1A2. Satisfactory completion of these tests assures normal performance of the rf #2 card (see paragraph 4-22e).

4-24. DIGITAL #3, A1A3A1A6. (See figures 4-43 and 4-44.)

The digital #3 card contains an input amplifier and divide-by-six frequency divider circuit, a digital mixer employing NAND gates, a divide-by-N digital counter with a variable division range from 2999 to 2000, and control gates to select the divide-by-N counter range via the 10 kc, 1 kc, and 100 cps tuning dials of the MEGACYCLES frequency selector A1A1A5. These circuits, in conjunction with the rf #2 card A1A3A1A5, form the phase-locked loop for the 100-cycle control circuit. Faulty operation of this card can prevent reception, partially or completely, over the entire receiver tuning range.

a. DESCRIPTION. - The digital #3 card indirectly controls the vco operating frequency at card rf #2, and therefore affects operation of both the 100 kc and 100 cycle tuning control circuits. In addition, the digital #3 card supplies a

standard 5 mc frequency, derived from the 3 mc frequency standard A1A1A1 via the mixer/multiplier module A1A3A2, to the bfo module A1A1A2. A 30 mc (standard) frequency from the mixer/multiplier module is amplified by Q1 and Q2, and applied to terminal 5 of the digital mixer Z2 via coupling capacitor C4. The 30 mc frequency is also applied to the high-speed binary flip-flop Q3 and Q4 for frequency division by a factor of two to obtain a 15 mc frequency. Emitter-follower Q5 applies this frequency to a divide-by-three circuit formed by digital flip-flops Z6 and Z7. The 5 mc resultant frequency goes through emitter-follower Q6 for application to the bfo module A1A1A2.

A 32,400,000 to 33,598,000 mc frequency range supplied from the rf #2 card A1A3A1A5 is combined with the 30 mc frequency from amplifier Q2 at the digital mixer Z2 to obtain a 2,400,000 to 3,598,800 mc difference frequency which is applied to the input of the divide-by-N counter circuit at Z4. The divide-by-N counter (Z4 and Z8 thru Z10, Z13 thru Z16, and Z18 thru Z22) develops the final frequency reduction to 1.2 kc when set (by the control gates) for frequency division by factors from 2999 to 2000. Control gates (Z11, Z12, and Z17), in response to the 10 kc, 1 kc, and 100 cps tuning dial settings, govern the divide-by-N counter operation. The 100 cps dial controls counting (frequency division) by "units", the 1 kc dial controls counting by "tens", and the 10 kc dial controls counting "hundreds", in a decimal sequence.

The 1.2 kc output from the divide-by-N circuit occurs only when the vco circuit in the rf #2 card A1A3A1A5 is phase-locked. When any one of the three tuning dials is reset, changing the divide-by-N division factor, the initial output frequency will be higher (or lower) than 1.2 kc until vco phase-locking occurs.

(1) BINARY LOGIC CIRCUITS. - The binary logic circuits employed are similar to those used in the digital #2 card A1A3A1A3. Refer to paragraph 4-21(1) for a description of the pulse-triggered binary circuits, and the Johnson divide-by-five counter circuits used in the digital #3 card.

(2) INPUT AMPLIFIER AND FREQUENCY DIVIDER ($\div 6$). - The input amplifier consists of stages Q1 and Q2. A 30 mc fixed frequency from the mixer/multiplier module A1A3A2 is amplified and applied to two separate circuits. Amplifier output from the emitter of Q2 is applied to the digital mixer Z2, and output from the collector of Q2 is applied to a high-speed flip-flop consisting of Q3 and Q4 for initial frequency division by a factor of two. Emitter-follower Q5 applies the 15 mc frequency obtained to a "short-counted" divide-by-three frequency divider formed by Z6 and Z7 to obtain a 5 mc frequency. Emitter-follower Q6 applies this frequency to the bfo module A1A1A2.

(3) DIVIDE-BY-N FREQUENCY DIVIDER. - The divide-by-N (2999 to 2000) digital counter consists of the thirteen diode-transistor (micro-logic) gated flip-flop circuits Z4, and Z8 thru Z10; Z13 thru Z16; and Z18 thru Z22, including the five-input dual gates of Z5. The counter is controlled (preset) by the dual-input quad gates Z11, Z12, and Z17 governed by the 10 kc, 1 kc, and 100 cps tuning dials. Each input pulse supplied by the 2,400,000 to 3,598,800 mc pulse train from the digital mixer Z2 decreases the preset count factor by one count, until an output pulse is produced to reset the counter and repeat the counting cycle. For example, when the input frequency is 2,400,000 mc, a 1.2 kc output frequency represents a frequency division by a factor of 2000. When the input frequency is 3,598,800 mc, a 1.2 kc output frequency represents division by a factor of 2999.

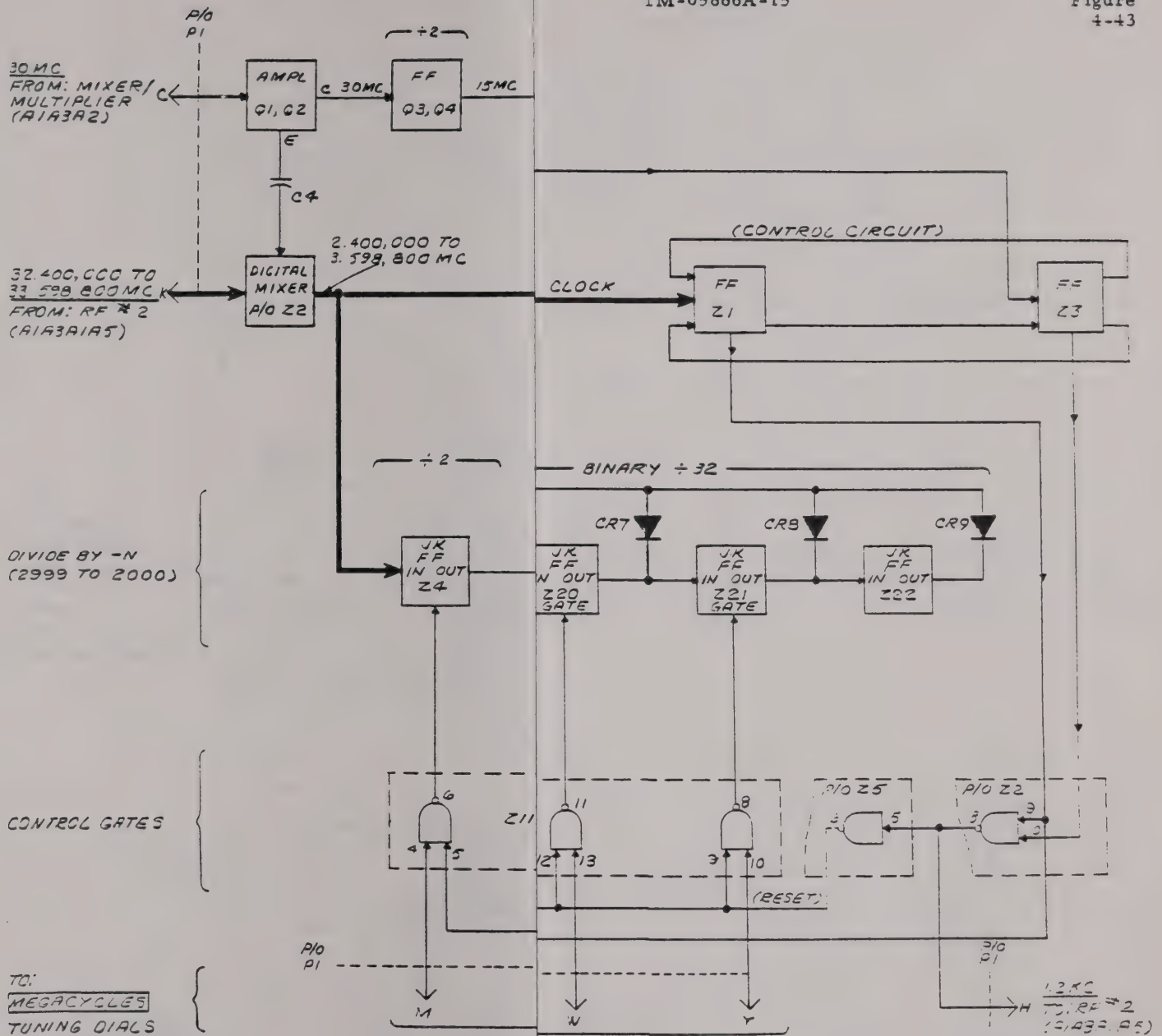


Figure 4-43. Digital #3 A1A3A1A6,
Simplified Block Diagram

standard 5 mc frequency, derived from the 3 mc frequency standard A1A1A1 via the mixer/multiplier module A1A3A2, to the bfo module A1A1A2. A 30 mc (standard) frequency from the mixer/multiplier module is amplified by Q1 and Q2, and applied to terminal 5 of the digital mixer Z2 via coupling capacitor C4. The 30 mc frequency is also applied to the high-speed binary flip-flop Q3 and Q4 for frequency division by a factor of two to obtain a 15 mc frequency. Emitter-follower Q5 applies this frequency to a divide-by-three circuit formed by digital flip-flops Z6 and Z7. The 5 mc resultant frequency goes through emitter-follower Q6 for application to the bfo module A1A1A2.

A 32,400,000 to 33,598,000 mc frequency range supplied from the rf #2 card A1A3A1A5 is combined with the 30 mc frequency from amplifier Q2 at the digital mixer Z2 to obtain a 2,400,000 to 3,598,800 mc difference frequency which is applied to the input of the divide-by-N counter circuit at Z4. The divide-by-N counter (Z4 and Z8 thru Z10, Z13 thru Z16, and Z18 thru Z22) develops the final frequency reduction to 1.2 kc when set (by the control gates) for frequency division by factors from 2999 to 2000. Control gates (Z11, Z12, and Z17), in response to the 10 kc, 1 kc, and 100 cps tuning dial settings, govern the divide-by-N counter operation. The 100 cps dial controls counting (frequency division) by "units", the 1 kc dial controls counting by "tens", and the 10 kc dial controls counting "hundreds", in a decimal sequence.

The 1.2 kc output from the divide-by-N circuit occurs only when the vco circuit in the rf #2 card A1A3A1A5 is phase-locked. When any one of the three tuning dials is reset, changing the divide-by-N division factor, the initial output frequency will be higher (or lower) than 1.2 kc until vco phase-locking occurs.

(1) BINARY LOGIC CIRCUITS. - The binary logic circuits employed are similar to those used in the digital #2 card A1A3A1A3. Refer to paragraph 4-21(1) for a description of the pulse-triggered binary circuits, and the Johnson divide-by-five counter circuits used in the digital #3 card.

(2) INPUT AMPLIFIER AND FREQUENCY DIVIDER ($\div 6$). - The input amplifier consists of stages Q1 and Q2. A 30 mc fixed frequency from the mixer/multiplier module A1A3A2 is amplified and applied to two separate circuits. Amplifier output from the emitter of Q2 is applied to the digital mixer Z2, and output from the collector of Q2 is applied to a high-speed flip-flop consisting of Q3 and Q4 for initial frequency division by a factor of two. Emitter-follower Q5 applies the 15 mc frequency obtained to a "short-counted" divide-by-three frequency divider formed by Z6 and Z7 to obtain a 5 mc frequency. Emitter-follower Q6 applies this frequency to the bfo module A1A1A2.

(3) DIVIDE-BY-N FREQUENCY DIVIDER. - The divide-by-N (2999 to 2000) digital counter consists of the thirteen diode-transistor (micro-logic) gated flip-flop circuits Z4, and Z8 thru Z10; Z13 thru Z16; and Z18 thru Z22, including the five-input dual gates of Z5. The counter is controlled (preset) by the dual-input quad gates Z11, Z12, and Z17 governed by the 10 kc, 1 kc, and 100 cps tuning dials. Each input pulse supplied by the 2,400,000 to 3,598,800 mc pulse train from the digital mixer Z2 decreases the preset count factor by one count, until an output pulse is produced to reset the counter and repeat the counting cycle. For example, when the input frequency is 2,400,000 mc, a 1.2 kc output frequency represents a frequency division by a factor of 2000. When the input frequency is 3,598,800 mc, a 1.2 kc output frequency represents division by a factor of 2999.

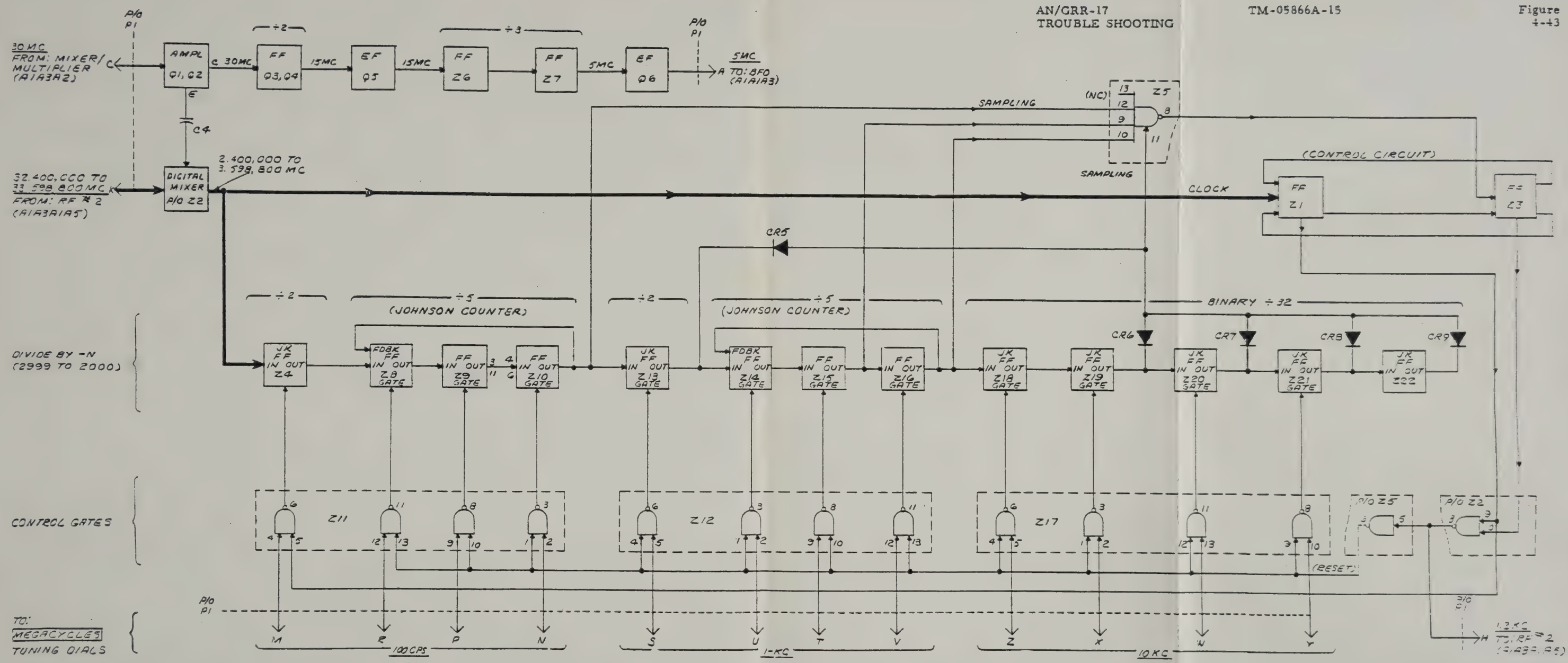


Figure 4-43. Digital #3 A1A3A1A6,
Simplified Block Diagram

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4-119/4-120

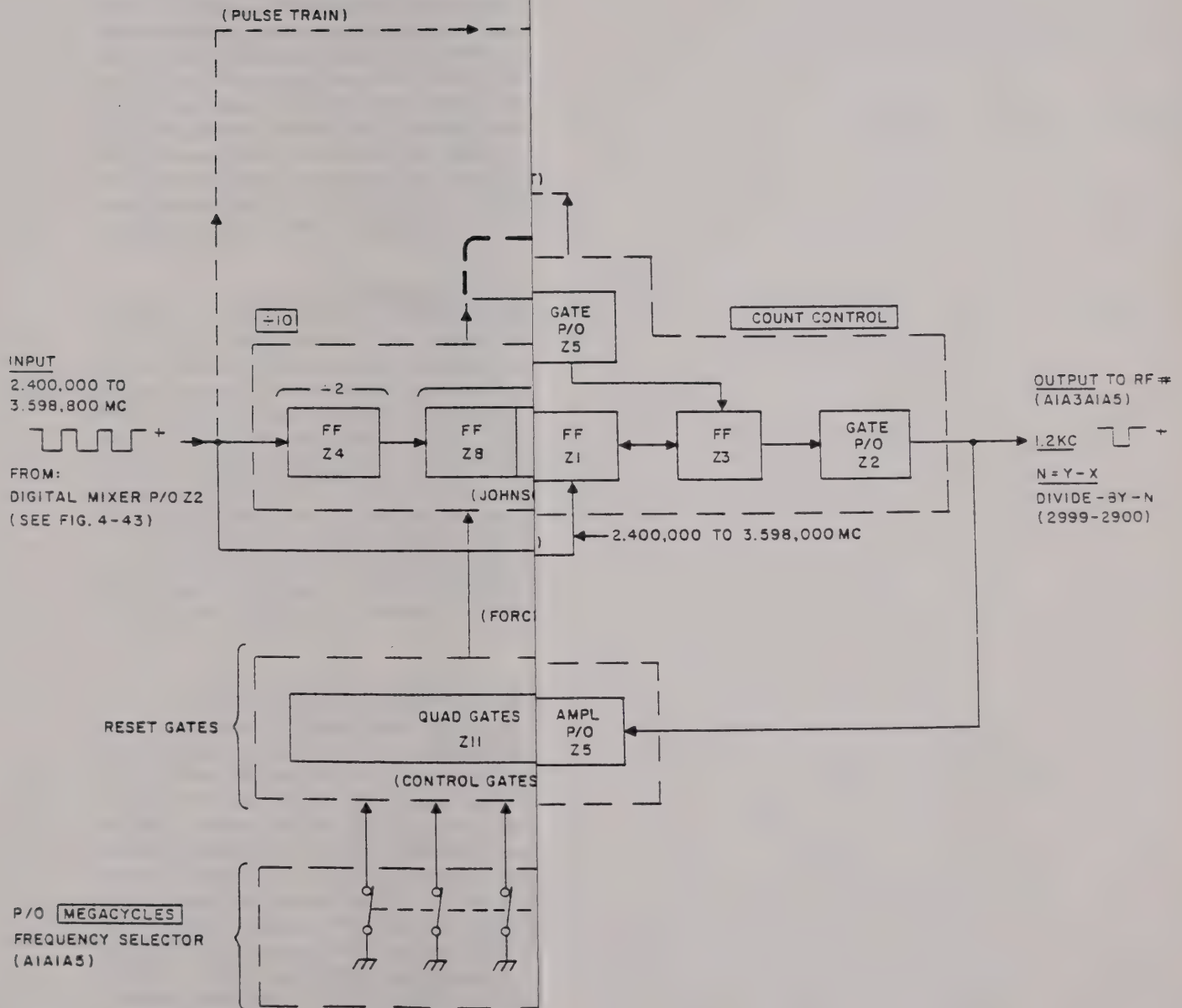


Figure 4-44. Digital #3 Divide-by-N
Counter, Mechanical Analogy

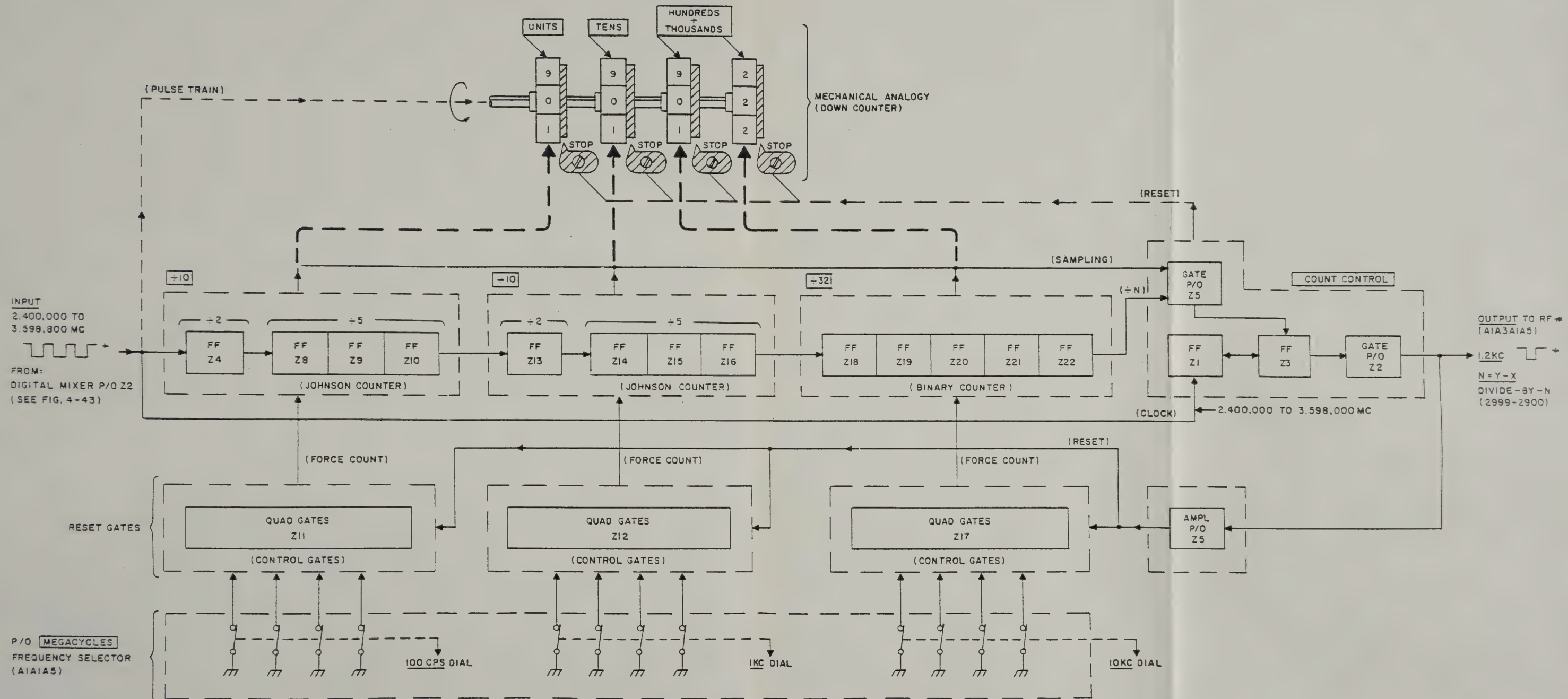


Figure 4-44. Digital #3 Divide-by-N
Counter, Mechanical Analogy

ORIGINAL

(a) Mechanical Analogy. - Figure 4-44 is a basic block diagram of the divide-by-N counter circuit and includes a mechanical analogy which, although not identical in every respect, resembles the counting functions performed by the digital counting circuits. The two divide-by-ten blocks, followed by the divide-by-32 block, function in a manner similar to the units, tens, and hundreds/thousands drums of the mechanical counter. Although the thousands drum remains permanently at the digit 2 position and does not change during counter operation, it is included in the analogy to represent the thousands digit of the division factors. The input pulse train is assumed to control the counting rate (or speed of operation) in both instances. Whereas the control gates, governed by setting the three tuning dials, set the count length for the binary dividers, the stop pawls shown in the analogy perform a similar function at the counter drums, with the exception of the aforementioned digit 2 drum. When the control gates preset the count length or cycle, the stop pawls similarly preset the drum readings. Because the divide-by-N counter is a "count-down" device, the mechanical counter drums also "count-down" from the preset digits. Each successive input pulse of the train decreases the count by one digit, until a count is reached terminating the cycle and the counter is reset to repeat the procedure. The count termination is the equivalent of the 1.2 kc output frequency, and represents division by a factor ranging from 2000 to 2999.

(b) Counting Cycle. - The divide-by-N counter is a variable length "down-counter" with a counting cycle which follows the mathematical expression: $N = y - x$; where N is the count length or division factor, y is the preset (start) count determined by the tuning dials settings, and x is the end (stop) count which produces a 1.2 kc output frequency. The first divide-by-ten block, controlled by the 100 cps tuning dial, counts in units. The second divide-by-ten block counts in tens and is controlled by the 1 kc tuning dial. The divide-by-32 block, controlled by the 10 kc tuning dial, counts in hundreds (and thousands). Therefore, the tens block receives one counting pulse for each group of ten (or less) pulses applied to the units block by the input pulse train, and the hundreds block receives one pulse for every ten (or less) applied to the tens block. Counter operation at this point is closely analogous to the mechanical four-drum counter illustrated in figure 4-44. Note that the hundreds/thousands drums only contain the digits from 20 to 29, corresponding to the hundreds/thousands digits of the minimum and maximum division factors.

A desired division factor is programmed by setting the three tuning dials. For example: A dial setting of 0, 0, 0 corresponds with the division factor 2000, and a dial setting of 9, 9, 9 corresponds with the division factor 2999. This is analogous to setting the mechanical counter drums for a reading of 2000 or 2999, respectively, reading from right to left. (Note that the division factor digits appear reversed at the counter drums to comply with the counting sequence of units, tens, hundreds, and thousands.) The counting cycle starts when a preset signal from the count-control block enables the control gates to insert the programmed division factor. Down-counting proceeds from the preset number until a 1.2 kc output is obtained. The count control block again presets the counter and the cycle is repeated, unless the tuning dials are reset for a different division factor. This action is analogous to the mechanical counter operation in the following manner: Mechanical counting starts when the preset signal from the count-control block releases the stop pawls, allowing the counter drums to operate. Down-counting progresses until the counter drums register 0, 0, 0, 0. At this point, the count-control block signal activates the stop pawls to stop the drums and stop the counting process, preset the drums to the division factor reading, and

release the drums to repeat the counting cycle. Although the mechanical counter can be described as "counting-down" to a 0, 0, 0, 0 reading, the digital counter circuit "zero count" condition occurs when a 1.2 kc output pulse appears. At this precise point, the individual counting blocks will contain an arrangement of logical "0" and "1" states. Consequently, it is misleading to refer to a literally "zero" count state.

(c) Count Control. - The count-control block contains five-input NAND gate (p/o Z5) and two dual gated-input flip-flops Z1 and Z3. The count control stops and resets the divide-by-N counter circuits (clears), presets the next count (division factor) by enabling the control gates, and initiates production of the 1.2 kc output pulse at the count termination. During the "count-down" cycle, the count control monitors the logical state of the counting process at the outputs of flip-flops Z10, Z13, Z15, Z16, and Z19 through Z22, via diodes CR5 through CR9. When the "zero-count" conditions appear at the end of a count cycle, the count control performs the stop, reset, and preset functions accompanied by the production of a 1.2 kc output pulse.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check on the digital #3 card before beginning trouble shooting, with emphasis on the following:

(1) Seating of the plug-in card in its compartment.

(2) Cable connections (if any) attached to the module.

c. TEST EQUIPMENT. - Not applicable.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figure 5-41.) - No external test points are provided at the digital #3 card. Therefore, trouble shooting is performed by repeating the test data steps for the rf #3 card A1A3A1A2. Satisfactory completion of these tests assures normal performance of the digital #3 card (see paragraph 4-22e).

4-25. DIGITAL #1, A1A3A1A7. (See figure 4-45.)

The digital #1 card contains a series of binary frequency-dividers for frequency divisions by factors of 12, 20, and 125, to obtain output frequencies of 12.5 kc and 1.2 kc from the 3 mc frequency-standard input frequency. These circuits supply a 12.5 kc pulse train to the rf #1(B) card A1A3A1A4, a 12.5 kc "sync" pulse train to the power supply module A1A3PS1, and a 1.2 kc pulse train to the rf #2 card A1A3A1A5. Because the frequencies are derived from the 3 mc frequency standard module A1A1A1, (via mixer/multiplier A1A3A2), they exhibit the same degree of accuracy and stability as that of the standard frequency. Faulty operation of this module can prevent reception completely.

a. DESCRIPTION. - The digital #1 card consists of two circuit sections: digital #1(A) A1A3A1A7A1 and digital #1(B) A1A3A1A7A2. The digital #1(A) circuit contains five binary flip-flops for division by a factor of 20 (Z3 through Z7), a dual five-input buffer (Z2), and three triple-input gates (Z1). The digital #1(B) circuit contains four flip-flops for division by a factor of 12 (Z1 through Z4), and seven flip-flops for division by a factor of 125 (Z5 through Z11). The dual buffer and the gates "sample" the binary counting process to obtain 12.5 kc and 1.2 kc pulse trains of different pulse widths, suitable for the intended applications.

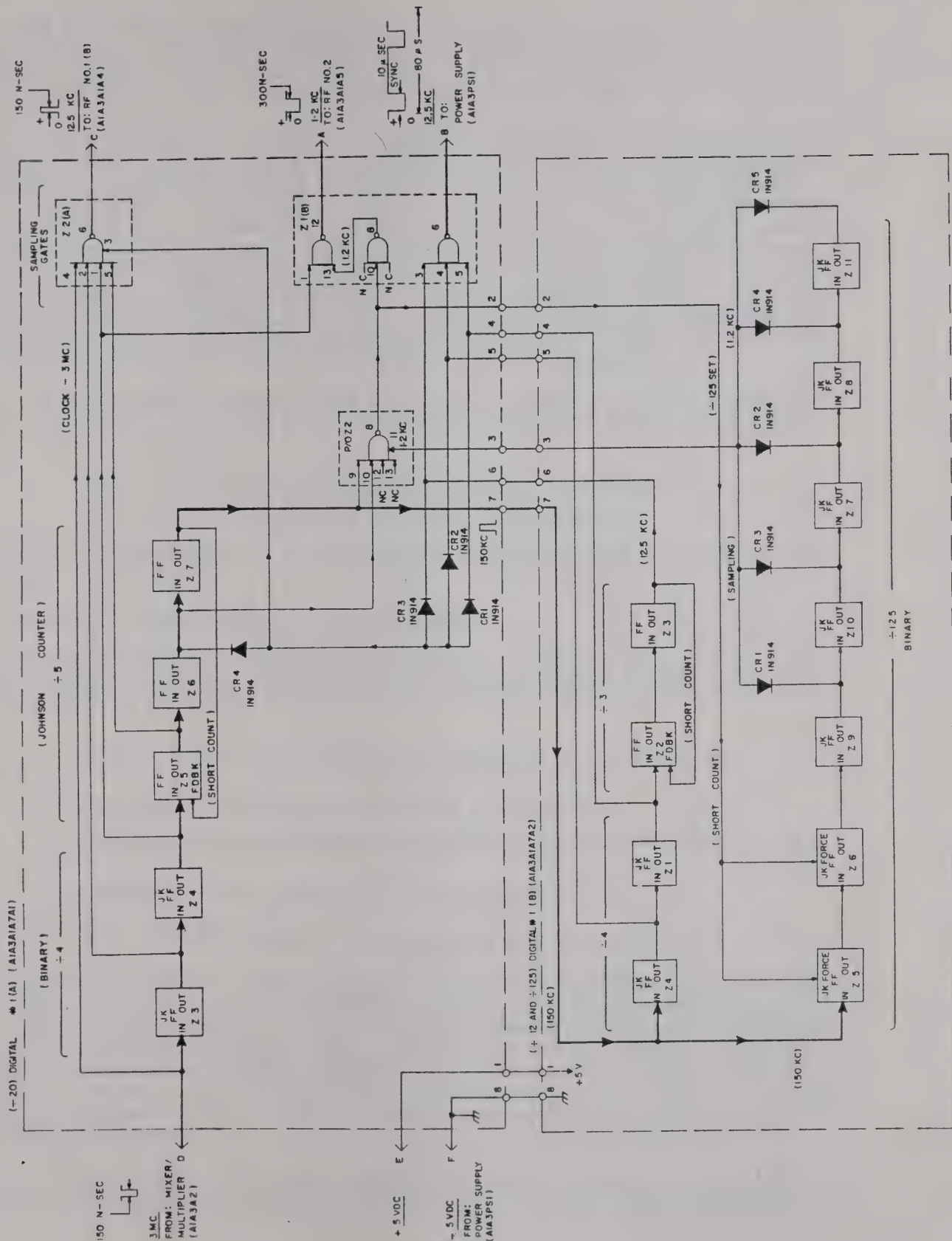


Figure 4-45. Digital #1 AIA3A1A7,
Simplified Block Diagram

from Z3 and applied at terminal 3 of Z1. Terminals 4 and 5 receive sample logic pulses of a shorter duration because they occur further back in the divider circuit. The resultant comparatively wide 12.5 kc pulse from Z1-6 has a width of approximately 10 usec, determined by the shortest of the sampled pulses.

The 1.2 kc output at terminal 12 of gate Z1 is a function of NAND gate operation, specifically at Z4, Z6, and Z7, via diode gates CR1 through CR5 in the digital #1(B) circuit. Terminals 9 and 10 of buffer Z2 receive a 150 kc pulse from Z6 and Z7 in digital #1(A). Terminal 11 receives a decoded sample of the divide-by-125 divider circuit in the digital #1(B) circuit. When these pulses occur simultaneously, output from terminal 8 of Z2 is applied to terminal 10 of Z1 where the pulse is inverted and reapplied to terminal 13 of Z1. Terminal 12 of Z1 produces a 1.2 kc pulse when all required gate inputs are applied simultaneously. The output pulse width is approximately 300 nsecs. The 1.2 kc frequency is a function of the sampled divide-by-125 counter pulse at terminal 11 of Z2, and the pulse width is determined by the sampled logical state at terminal 1 of buffer Z2.

b. PRELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check on the digital #1 card before beginning trouble shooting, with emphasis on the following:

- (1) Seating of the double-plug-in card in its compartment.
- (2) Cable connections (if any) attached to the module.

c. TEST EQUIPMENT. - Use Frequency Counter 5245L or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figures 5-42 and 5-43.) - Trouble shooting the digital #1 card consists of verifying the presence of output frequencies at test points provided. Perform the following:

- (1) Connect frequency counter to test point J2(TP) on the rf #1(B) card A1A3A1A4.
- (2) The counter should measure a 12.5 kc frequency.
- (3) Connect frequency counter to test point J7(TP) on the power supply module A1A3PS1.
- (4) Counter should measure a 12.5 kc frequency.

4-26. MIXER/MULTIPLIER A1A3A2. (See figures 4-46 and 4-47.)

The mixer/multiplier module consists of frequency multiplier circuits which develop output frequencies of 30 mc and 117 mc from a 3 mc standard input frequency. These circuits supply a 3 mc frequency to the digital #1 card A1A3A1A7, a 30 mc frequency to the digital #3 card A1A3A1A6, a 117 mc frequency (fixed, or tunable ± 150 cycles by the FREQ VERNIER ± 150 CPS panel control) to the first i-f amplifier module A1A2A3, and a 120 mc frequency to the rf #3 card A1A3A1A2, via the X4 multiplier Z2 (p/o A1A3A1). Faulty operation of this module can prevent reception completely.

a. DESCRIPTION. - The mixer/multiplier module contains two circuit sections: the X4 multiplier (A1) and the X10 multiplier (A2). The X4 multiplier

(1) DIVIDE-BY-20 FREQUENCY DIVIDER. - The divide-by-20 frequency divider in the digital #1(A) circuit consists of a divide-by-four divider using Z3 and Z4 connected as JK binary counters, followed by a divide-by-five divider using Z5, Z6, and Z7 arranged in a Johnson counter configuration (see paragraph 4-21a(1)(b)). The 750 kc frequency at the output of Z4 is reduced to 150 kc by the Johnson circuit. Short counting is obtained by the feedback connections from Z7 to Z5. A peculiarity of the Johnson counter is the presence of an output frequency at more than one circuit point. Therefore, the 150 kc frequency is obtained at Z6 as well as at Z7 and applied to diode CR4 and to terminal 9 of buffer Z2, respectively.

(2) DIVIDE-BY-12 FREQUENCY DIVIDER. - The divide-by-12 frequency divider in the digital #1(B) circuit consists of a divide-by-four divider using Z4 and Z1 connected as JK binary counters, followed by a divide-by-three divider using Z2 and Z3. The latter divider employs a "short count" connection from Z2 to Z3 to obtain division by a factor of 3 instead of a factor of 4. The 150 kc input frequency applied to Z4 is reduced to 12.5 kc at the Z3 output and applied to diode gate CR3 and one of the Z1 gates, located in the digital #1(A) circuit. In addition, binary outputs are sampled from Z4 and Z1, and applied to diodes CR2 and CR1.

(3) DIVIDE-BY-125 FREQUENCY DIVIDER. - The divide-by-125 frequency divider in the digital #1(B) circuit consists of a string of binary, JK connected, flip-flops using Z5 through Z11. Normally, seven flip-flops will count up to 128 (2^7). To reduce this count by 3 digits to obtain a count or frequency division by 125, a "short count" connection at Z5 and Z6 forces a logical "1" state at these flip-flops and counting occurs in a digital sequence from 3 to 128 for a net count of 125. The 150 kc input frequency at Z5 is reduced to 1.2 kc at the Z11 output. The count status at Z9, Z10, Z7, Z8, and Z11 is sampled via diode gates CR1 through CR5 and applied to one input of dual buffer Z2 on the digital #1(A) circuit. In this manner, the logical state of the divide-by-125 flip-flops is decoded because a logical "0" occurs at the sampled circuit points only when a division by 125 has occurred.

(4) DIVIDER OUTPUT GATES. - The two 12.5 kc and the single 1.2 kc output pulse trains are obtained from the various frequency divider circuits via the dual five-input buffer Z2 and the three triple-input gates Z1 in the digital #1(A) circuit. These gating circuits perform the function of sampling and decoding to obtain several pulse-train output frequencies with different pulse widths.

The 12.5 kc output from terminal 6 of Z2 has a relatively narrow pulse width determined by the 150 nsec rise time of the 3 mc "clock" pulse from the mixer/multiplier module A1A3A2 at terminal 4. Terminals 2, 1, and 5, sample the logic state at flip-flops Z3, Z4, and Z5, respectively. Terminal 3 receives the actual 12.5 kc frequency from Z3 in the digital #1(B) circuit as well as other logic states sampled by diode gates CR1 through CR4. Because the buffer Z2 circuits also function as NAND gates, output occurs at terminal 6 only when all buffer inputs are present, simultaneously. Therefore, the output frequency is determined by the 12.5 kc frequency at terminal 3 and the pulse duration is governed by the narrow "clock" pulse at terminal 4.

The 12.5 kc output from terminal 6 of gate Z1 is obtained by sampling the logical state of flip-flops Z4, Z1, and Z3, respectively, in the digital #1(B) circuit. The three Z1 gates are also NAND gates and an output occurs only when all three inputs are applied simultaneously. A 12.5 kc frequency is obtained directly

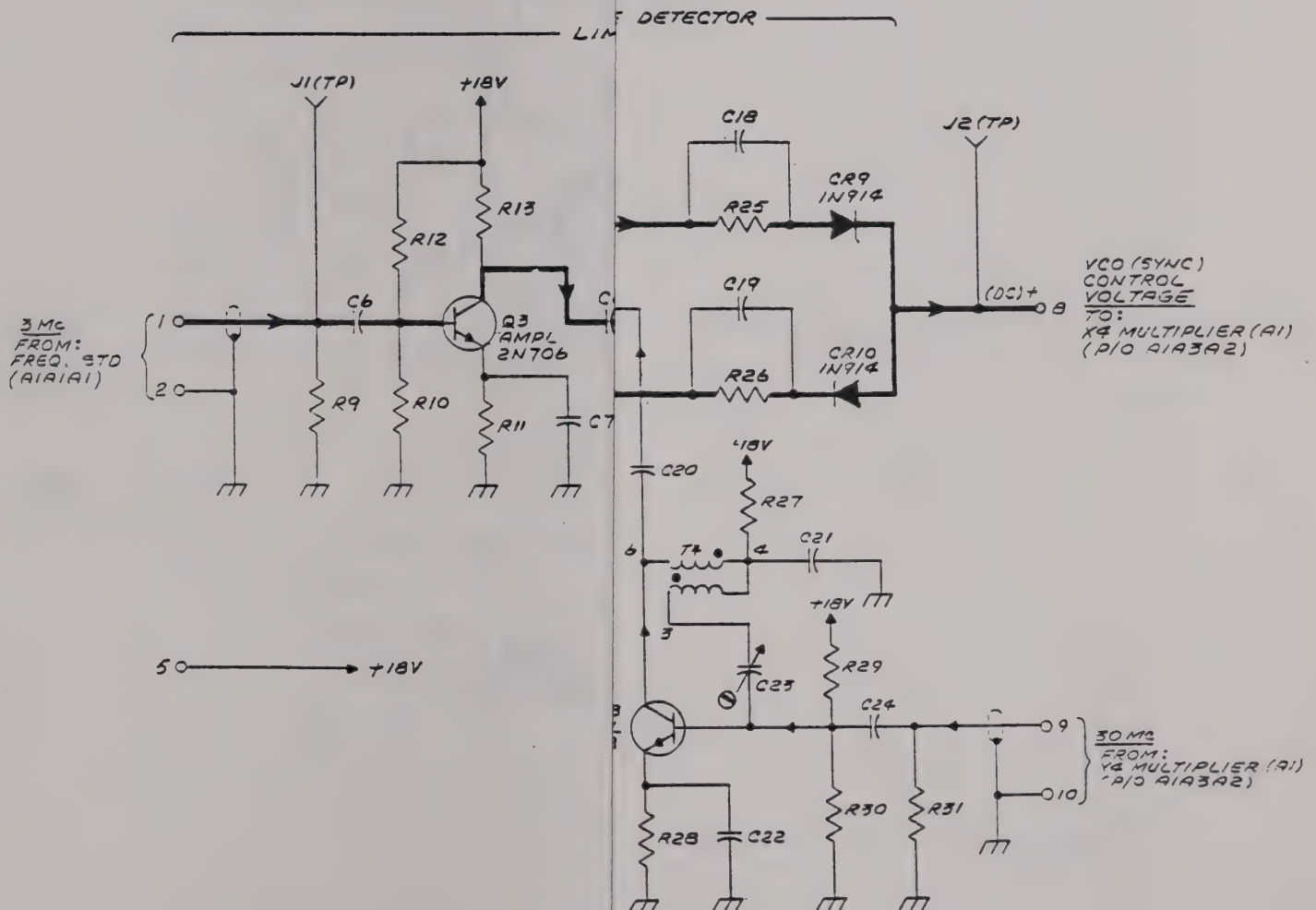


Figure 4-46. Mixer/Multiplier A1A3A2,
X10 Multiplier (A2);
Simplified Schematic Diagram

(1) DIVIDE-BY-20 FREQUENCY DIVIDER. - The divide-by-20 frequency divider in the digital #1(A) circuit consists of a divide-by-four divider using Z3 and Z4 connected as JK binary counters, followed by a divide-by-five divider using Z5, Z6, and Z7 arranged in a Johnson counter configuration (see paragraph 4-21a(1)(b)). The 750 kc frequency at the output of Z4 is reduced to 150 kc by the Johnson circuit. Short counting is obtained by the feedback connections from Z7 to Z5. A peculiarity of the Johnson counter is the presence of an output frequency at more than one circuit point. Therefore, the 150 kc frequency is obtained at Z6 as well as at Z7 and applied to diode CR4 and to terminal 9 of buffer Z2, respectively.

(2) DIVIDE-BY-12 FREQUENCY DIVIDER. - The divide-by-12 frequency divider in the digital #1(B) circuit consists of a divide-by-four divider using Z4 and Z1 connected as JK binary counters, followed by a divide-by-three divider using Z2 and Z3. The latter divider employs a "short count" connection from Z2 to Z3 to obtain division by a factor of 3 instead of a factor of 4. The 150 kc input frequency applied to Z4 is reduced to 12.5 kc at the Z3 output and applied to diode gate CR3 and one of the Z1 gates, located in the digital #1(A) circuit. In addition, binary outputs are sampled from Z4 and Z1, and applied to diodes CR2 and CR1.

(3) DIVIDE-BY-125 FREQUENCY DIVIDER. - The divide-by-125 frequency divider in the digital #1(B) circuit consists of a string of binary, JK connected, flip-flops using Z5 through Z11. Normally, seven flip-flops will count up to 128 (2^7). To reduce this count by 3 digits to obtain a count or frequency division by 125, a "short count" connection at Z5 and Z6 forces a logical "1" state at these flip-flops and counting occurs in a digital sequence from 3 to 128 for a net count of 125. The 150 kc input frequency at Z5 is reduced to 1.2 kc at the Z11 output. The count status at Z9, Z10, Z7, Z8, and Z11 is sampled via diode gates CR1 through CR5 and applied to one input of dual buffer Z2 on the digital #1(A) circuit. In this manner, the logical state of the divide-by-125 flip-flops is decoded because a logical "0" occurs at the sampled circuit points only when a division by 125 has occurred.

(4) DIVIDER OUTPUT GATES. - The two 12.5 kc and the single 1.2 kc output pulse trains are obtained from the various frequency divider circuits via the dual five-input buffer Z2 and the three triple-input gates Z1 in the digital #1(A) circuit. These gating circuits perform the function of sampling and decoding to obtain several pulse-train output frequencies with different pulse widths.

The 12.5 kc output from terminal 6 of Z2 has a relatively narrow pulse width determined by the 150 nsec rise time of the 3 mc "clock" pulse from the mixer/multiplier module A1A3A2 at terminal 4. Terminals 2, 1, and 5, sample the logic state at flip-flops Z3, Z4, and Z5, respectively. Terminal 3 receives the actual 12.5 kc frequency from Z3 in the digital #1(B) circuit as well as other logic states sampled by diode gates CR1 through CR4. Because the buffer Z2 circuits also function as NAND gates, output occurs at terminal 6 only when all buffer inputs are present, simultaneously. Therefore, the output frequency is determined by the 12.5 kc frequency at terminal 3 and the pulse duration is governed by the narrow "clock" pulse at terminal 4.

The 12.5 kc output from terminal 6 of gate Z1 is obtained by sampling the logical state of flip-flops Z4, Z1, and Z3, respectively, in the digital #1(B) circuit. The three Z1 gates are also NAND gates and an output occurs only when all three inputs are applied simultaneously. A 12.5 kc frequency is obtained directly

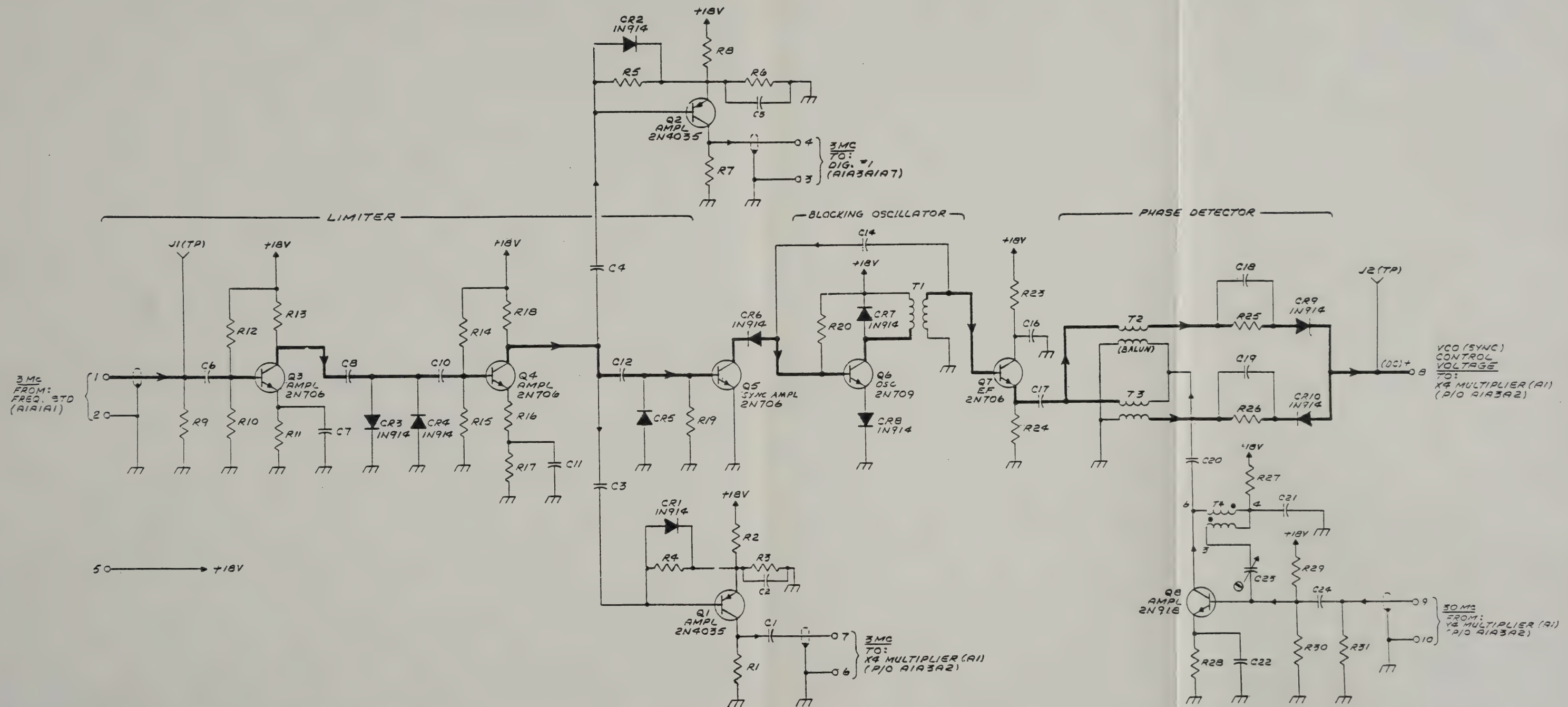


Figure 4-46. Mixer/Multiplier A1A3A2,
X10 Multiplier (A2);
Simplified Schematic Diagram

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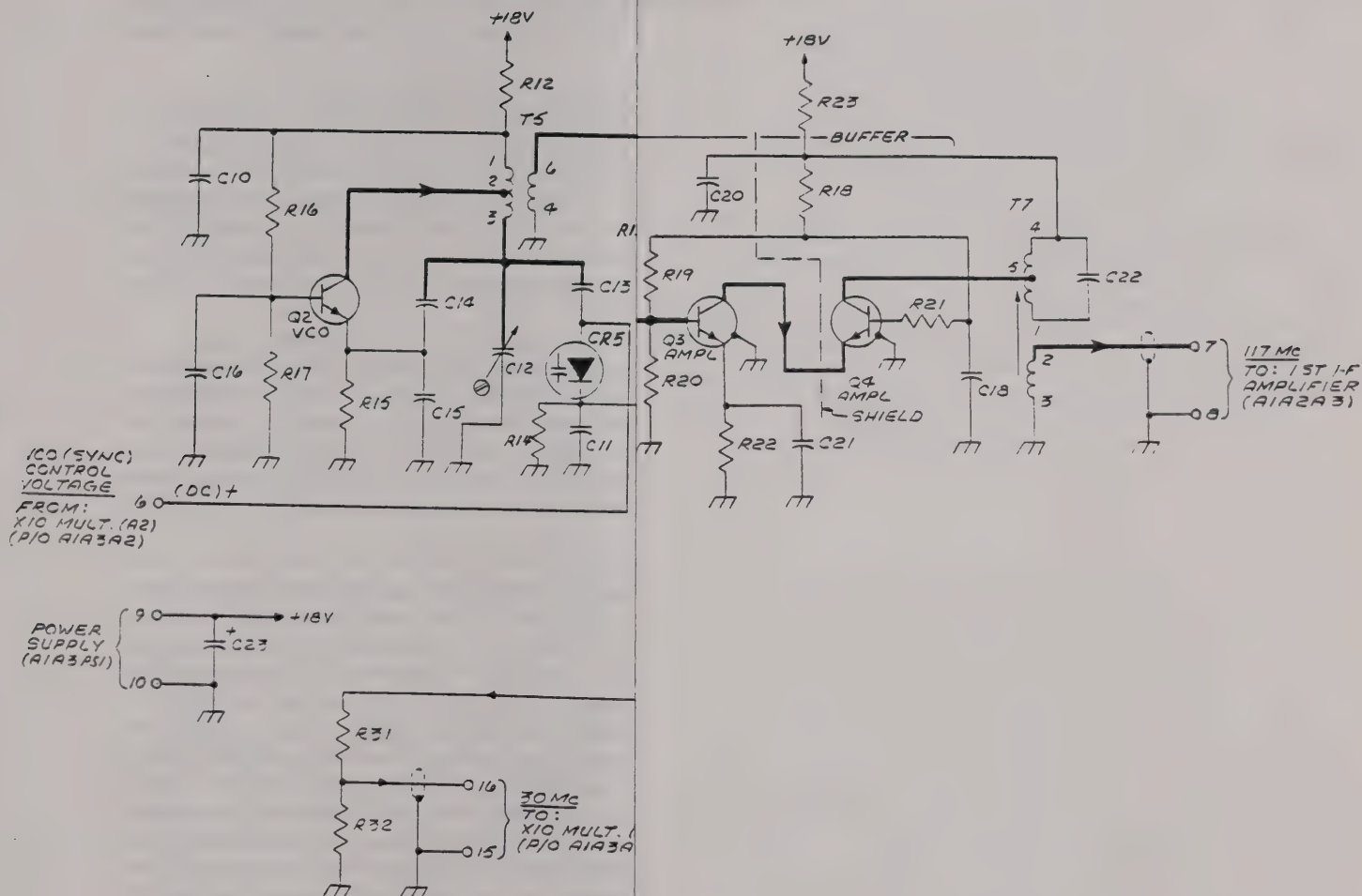
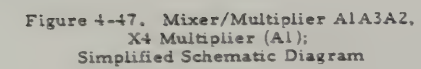


Figure 4-47. Mixer/Multiplier A1A3A2, X4 Multiplier (A1); Simplified Schematic Diagram



AN/GI
TROU

circuit
stages
buffer
30 mc
in turn
(A2).

limited
a phase
individ
A1A1A
amplifi
the ph

frequency
Q2 is
primary
adjust
(in se
lateral
cuit, :

frequency
multip
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uses t
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circuit employs a 30 mc voltage-controlled oscillator (vco, Q2), two X2 multiplying stages using varactor diodes (CR1 through CR4), mixer stage (Z1), and individual buffer amplifiers for the two output frequencies (Q3 and Q4, and Q7 and Q8). The 30 mc and 117 mc output frequencies are derived from the 30 mc vco output which in turn is frequency locked by a dc control voltage supplied by the X10 multiplier (A2).

The X10 multiplier A2 contains a three stage amplifier (Q3, Q4, and Q5), a limiter (CR3, CR4), a blocking oscillator (Q6) followed by emitter-follower (Q7), a phase detector (CR9 and CR10), and buffer amplifiers (Q1, Q2, and Q8). The individual buffer amplifiers supply a (limited) 3 mc frequency to the vfo module A1A1A3 and to the digital #1 card A1A3A1A7, respectively. The remaining buffer amplifier applies the 30 mc vco output frequency from the X4 multiplier (A1) to the phase detector (CR9 and CR10).

(1) X4 MULTIPLIER A1. - The X4 multiplier circuit generates a 30 mc frequency which is used to derive the 30 mc and 117 mc output frequencies. Vco Q2 is arranged in a modified Colpitts circuit with the tank circuit formed by the primary of transformer T5, series tuned by capacitors C14 and C15. Frequency adjustment capacitor C12 parallels the tuned circuit capacitors and varactor CR5 (in series with capacitors C11 and C13) provides for voltage control of the oscillator frequency. A varactor-control voltage, developed in the X10 multiplier circuit, is applied at the junction of varactor CR5 and capacitor C13.

Emitter-follower Q1 applies the 30 mc oscillator output frequency to two X2 frequency multipliers, in series, to obtain a 120 mc frequency. The first X2 multiplier stage uses transformers T4 and T3 with varactors CR4 and CR3, arranged to form a parametric frequency multiplier. The second X2 multiplier uses transformers T2 and T1 with varactors CR2 and CR1 in a similar circuit arrangement. The circuit operation is identical at each multiplier stage with the exception of the frequencies involved.

The first X2 multiplier employs varactors as non-linear components for harmonic generation, especially the 30 mc second harmonic (60 mc). The +18 volt supply potential provides a varactor reverse-bias via resistors R4 and R5. Capacitors C4, C5, and C6 bypass the signal components while blocking the dc supply voltage path to ground. A 30 mc signal applied from the secondary of transformer T4 drives the two varactors (as variable voltage-controlled capacitors) over their non-linear operating range in a push-pull manner. When the current through CR3 is increasing at the top half of the transformer T3 primary, the current through CR4 is decreasing at the bottom half of the winding. The two out-of-phase primary currents are additive and induce a large current flow in the T3 secondary, similar to push-pull operation employing signal amplifiers. Because the primary winding of T3 is tuned to 60 mc by the effective capacitance of C6, CR3, CR4, and C5, other harmonic frequencies present are greatly reduced and a 60 mc frequency predominates at the secondary of T3. The second X2 multiplier operates in the same manner to obtain a 120 mc frequency at the secondary of transformer T1. This frequency is applied to mixer Z1.

Mixer Z1 combines the 120 mc multiplier output frequency with a 3 mc frequency from the vfo module A1A1A3. The 117 mc difference frequency at the mixer output is coupled to the cascode amplifier Q3 and Q4 via transformer T6. The secondary of T6 is tuned to 117 mc by capacitor C17. Cascode amplifier output passes through transformer T7, capacitor C22 tuning the primary to 117 mc.

3 mc frequency generated by vco Q2 is applied to other circuits via Resistors R31 and R32 form an attenuator to reduce the signal level at the X10 multiplier circuit section A2. Also, a 30 mc signal through coupling capacitor C30 and amplified by cascode amplifier Q8 to application to the digital #3 card A1A3A1A6 and X4 multiplier. The primary of transformer T9 is tuned to 30 mc by capacitor C33.

X10 MULTIPLIER A2. - The X10 multiplier circuit A2 receives a signal from the 3 mc frequency standard module A1A1A1. The signal is limited (clipped) by diodes CR3 and CR4. The amplitude is then amplified by Q4 and applied to the "sync" amplifier Q5.

Diode CR6 protects the base-emitter junction of Q5 from damage by negative-going pulses. Diode CR6 permits application of the +18 volt supply potential and collector-emitter junction of Q5 from pulse excursions generated by oscillator Q6. The square wave (limited) pulse train from Q5 is applied to blocking oscillator Q6 at a 30 mc frequency. Diode CR8 protects the base-emitter junction of Q6 from the effect of negative-going "sync" pulses, and CR7 protects the collector-emitter junction by functioning as a "damper" in the primary winding. Pulse transformer T1 applies the blocking oscillator in the form of a positive-going pulse train with a 30 nsec pulse width, to the base of Q7. Capacitor C14 from the primary of T1 serves as a positive feedback path to the base of Q6. Pulse output from Q7 is applied to one input of phase detector CR9 and CR10 via balun transformers T2 and T3.

The "x-car" phase detector CR9 and CR10 is "turned-on" during the 30 mc frequency period from emitter-follower Q7. A 30 mc signal sample from the multiplier circuit A1 is applied to the second phase-detector input, via balun transformers T2 and T3, and appears at the phase-detector output during pulse duration period only. Consequently, the dc varactor control voltage is a function of the frequency relation between the two phase-detector inputs. When the two input frequencies coincide, zero output voltage occurs. When the two input frequencies are out-of-phase, a corresponding positive or negative dc voltage is developed to correct the frequencies and bring the frequencies into phase. In this manner, the varactor control voltage is developed by the phase detector controls and "locks" the vco operation.

The "sample" frequency from the X4 multiplier vco circuit is amplified and applied to the phase detector via capacitor C20. The 30 mc (limited) signal at the output of limiter amplifier Q4 is applied to other circuits via buffer amplifiers. Amplifier Q2 receives a 3 mc square-wave input via capacitor C4, amplifies it, and applies it to the digital #1 card. Amplifier Q1 also receives a 3 mc square wave input signal via capacitor C4. Following amplification, it is applied to the vfo (A1A1A3). Diodes CR1 and CR2 protect the base-emitter junctions of Q1 and Q2.

ELIMINARY CHECK. (See figure 4-58.) - With power off, make a preliminary check of the mixer/multiplier module before beginning trouble shooting, as follows on the following:

Seating of the plug-in module in its socket.

Cable connections (if any) attached to module.

c. TEST EQUIPMENT. - Use Frequency Counter 5245L or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figures 5-44 and 5-45.) - Trouble shooting the mixer/multiplier module consists of verifying the output frequency at a test point provided. Perform the following:

(1) Connect the frequency counter to test point J1(TP) on the mixer/multiplier module.

(2) The counter should measure 3.0 mc.

4-27. POWER SUPPLY A1A3PS1. (See figures 4-48 and 4-49.)

The power supply module consists of an ac power supply and regulator circuit (producing +24 vdc), followed by individual regulating circuits which supply 5 volts dc, 15 volts dc, 18 volts dc, and an unregulated 125 volts dc to the receiver modules when operated from a primary power source of 117 volts ac, 50 to 400 cycles, single phase. For operation from a 24 volt dc primary power source, the ac power supply and regulator circuit is by-passed and the 24 volt dc primary source is substituted. Each regulating circuit is equipped with a protective fuse and a test point for measuring the supply voltage.

a. DESCRIPTION. - The power supply module contains the ac power supply and regulator which supplies a regulated +24 volts dc to operate a chain of individual regulator and supply circuits. These are: a +5 volt and +18 volt regulator (A3A1), a +15 volt regulator (A3A2), and a +125 volt unregulated supply (A1). The +24 volt regulating circuit employs a series regulator (Q1) controlled by a reference amplifier (Q2). The +5 volt and +18 volt regulating circuits use a series "switching" regulator (A1A3PS1A2Q2 and A1A3PS1A2Q1, respectively), controlled by a driver stage (Q4, Q5, and Q1, Q2, respectively). Digital-type differential comparators (Z1 and Z2) sense the supply voltage changes and in turn control the switch driver stages. During operation, the series "switching" regulators are turned off and then on rapidly, in response to the driver stage output pulses. Voltage regulation is a function of the duration of off and on pulse periods. The +15 volt regulating circuit is conventional with the series regulator (A1A3PS1A2Q3) controlled by dc amplifier (Q1). Differential amplifiers (Q2 and Q3) in turn, control the dc amplifier. The +125 volt supply circuit is a sealed component containing the circuits for obtaining a +125 volt dc supply voltage from the +15 volt output of the +15 volt regulating circuit. In addition, the power supply supplies +24 volts dc to the TTY power supply (A1A3Z1) when the TELETYPE MODE switch is in the INT BAT (internal battery) position.

(1) AC POWER SUPPLY AND REGULATOR. - The ac power supply and regulator circuit consists of power transformer T1, a full-wave bridge rectifier using CR1 through CR4, a single section LC filter using L1 and C1, and the 24 volt regulating circuit of Q1 and Q2. The regulated +24 volts dc from this supply serves as the source voltage for operation of the +5 volt and +18 volt regulator circuit A3A1. Zener CR6 supplies the reference dc voltage for the reference amplifier Q2.

Regulator stage Q1 and Q2 form a Darlington circuit for high current gain and series regulator Q1 is controlled by Q2. Zener diode CR6 provides a reference voltage for regulator operation.

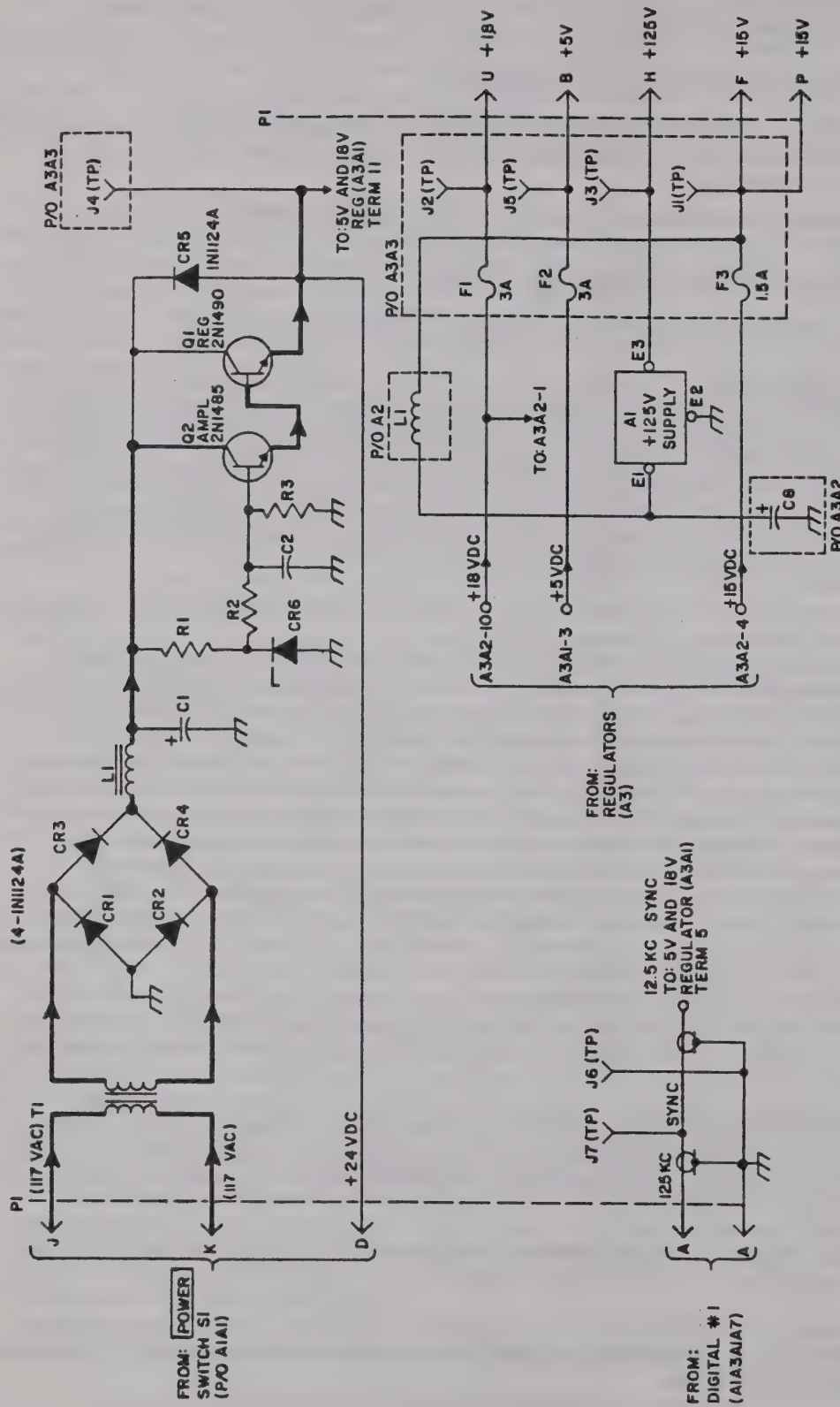


Figure 4-48. Power Supply A1A3PS1; Pre-regulator and +125 Volt Supply (A1),
Simplified Schematic Diagram

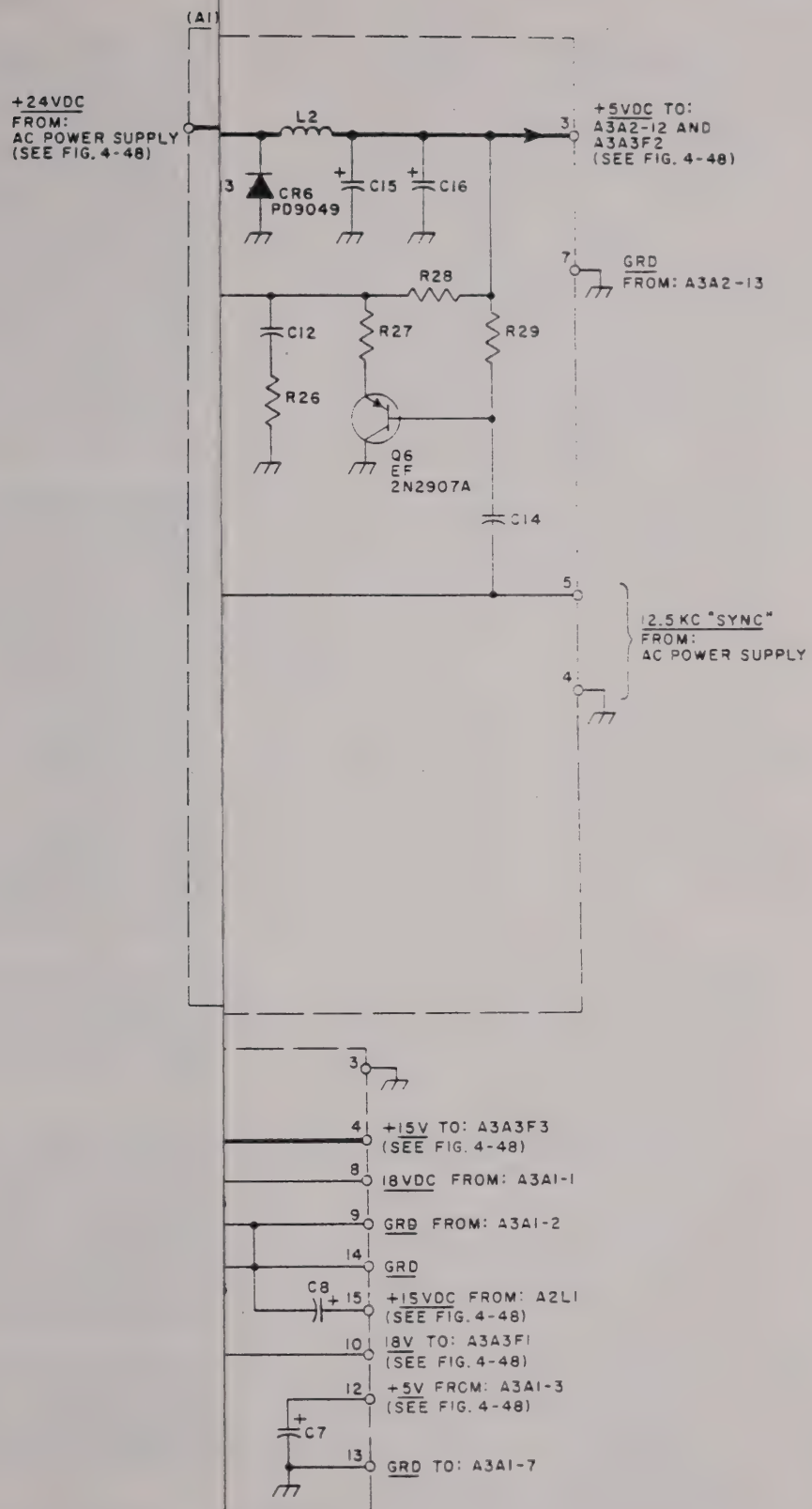
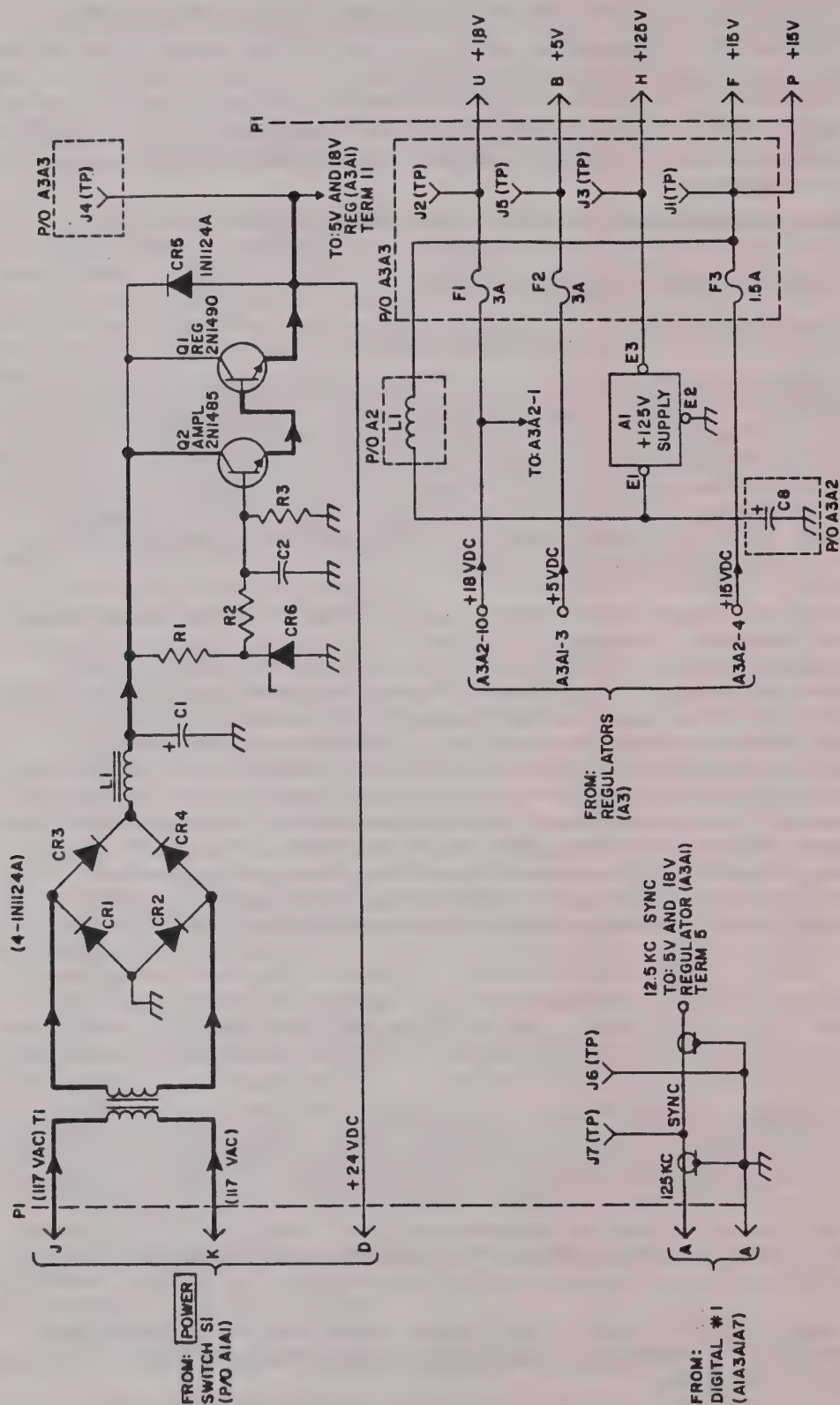


Figure 4-49. Power Supply A1A3PS1;
+5 Volt, +18 Volt Regulators (A3A1),
+15 Volt Regulator (A3A2);
Simplified Schematic Diagram



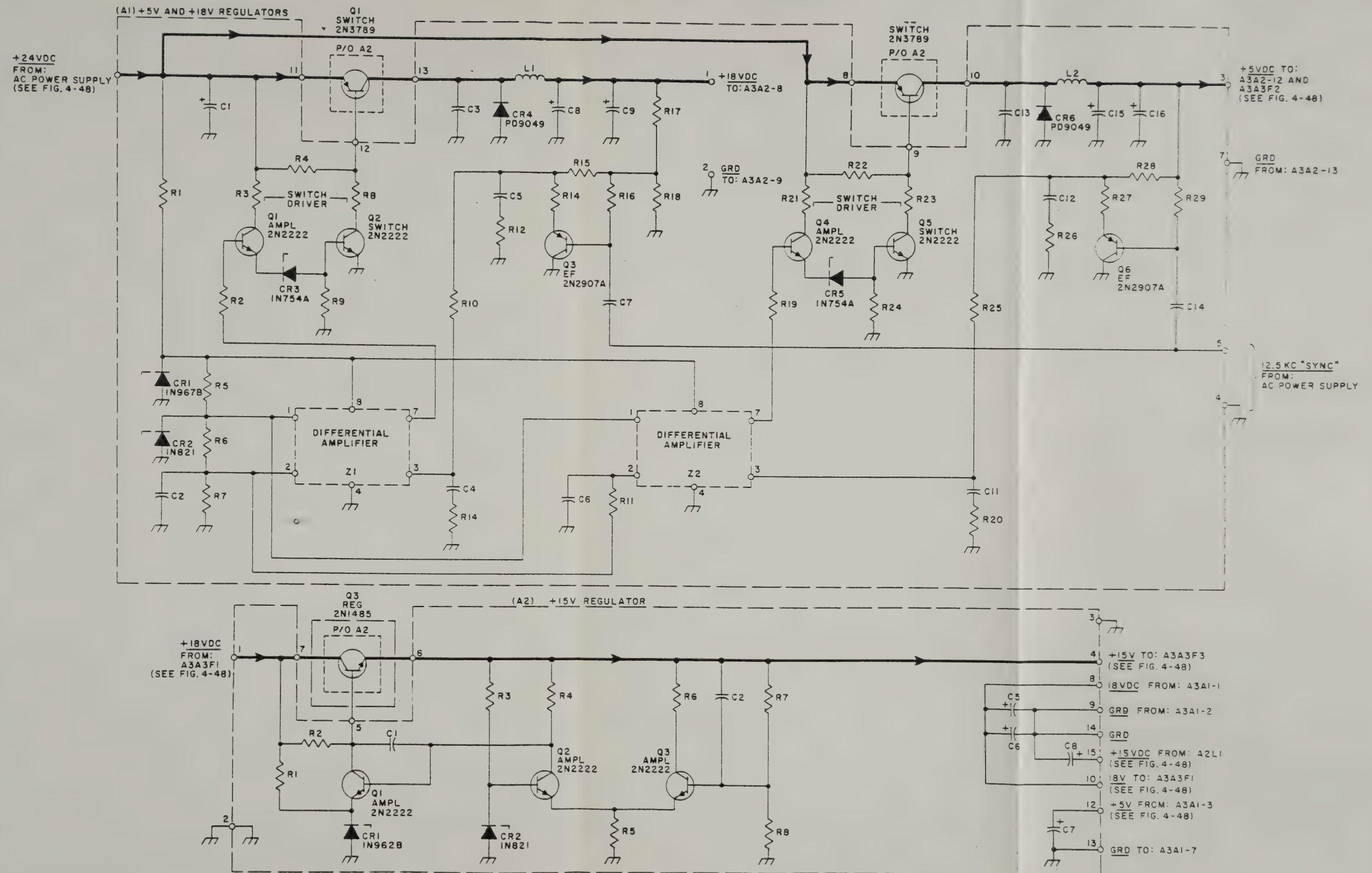


Figure 4-49. Power Supply AlA3PS1;
+5 Volt, +18 Volt Regulators (A3A1),
+15 Volt Regulator (A3A2);
Simplified Schematic Diagram

(2) +5 VOLT AND +18 VOLT REGULATORS A3A1. - The +5 volt and +18 volt regulating circuits are similar in that they both employ a "switching" type series regulating stage and share a common 12.5 kc "sync" pulse train supplied from the digital #1 card A1A3A1A7. To this extent, circuit operation is the same in both regulating circuits. Switching-type series regulators offer high regulator efficiency because of the low power dissipation accompanying their pulse-mode type of operation. The regulating transistor is operated at either saturation or cut-off and the width of the pulse drive determines the duty-time of each operating mode. A switch driver circuit provides the pulse drive in response to the output of a digital-type differential amplifier which samples the regulator output voltage. Circuit parameters are selected to obtain a "switching" rate of approximately 12 kc and the circuit is synchronized by application of a 12.5 kc "sync" pulse supplied from the digital #1 card A1A3A1A7. To integrate the "switched" regulator output voltage, a single LC filter section follows the switching regulator stage, smoothing the pulses to obtain a steady dc output.

(a) +5 Volt Regulator Circuit. - A 24 volt dc supply voltage from the ac power supply circuit is applied to the emitter of series "switching" regulator A1A3PS1A2Q2 and also as an operating voltage to the switch driver stage Q4 and Q5. Switch Q5 is triggered on and off by current amplifier Q4, in response to drive pulses supplied by the differential comparator Z2. The comparator output pulses are above ground by approximately 6 volts. Therefore, to assure a "turn-off" at switch Q5, Zener diode CR5 inserts a similar (bucking) potential in series with the emitter of Q4 to ground, "restoring" the pulse train to a ground reference level. Differential comparator Z2 compares a sample of the +5 regulator output voltage with a fixed reference voltage contributed by Zener diode CR2. When the regulator output exceeds the reference voltage, the pulse width is decreased to decrease the switch regulator A1A3PS1A2Q2 on time and thereby lower the output voltage. When the regulator output voltage is less than the reference voltage, the pulse width is increased to increase the switch regulator on time and raise the output voltage. In this manner, the switch regulator is controlled in a step sequence to regulate the circuit output voltage and hold it constant.

To stabilize the regulator and improve its operation, a 12.5 kc "sync" pulse is amplified by emitter-follower Q6 and applied to the differential comparator Z2 via a low pass filter consisting of R25, and C11 and C12. The "sync" pulse "times" the comparator output pulse train and therefore the switching rate of A1A3PS1A2Q2.

The dc pulses at the output of switch regulator A1A3PS1A2Q2 go through a low-pass LC filter network consisting of L2, C13, C15, and C16 and C7 (p/o A3A2). A "commutating" diode CR6 functions as a circuit return path for L2, C15 (and C16). During the switch regulator A1A3PS1A2Q2 off intervals, the collapsing field of inductor L2 charges capacitor C15 (and C16) via the diode CR6 return circuit. In this manner, the charge at C15 is maintained during the regulator off periods to assure adequate regulator output current to the load at all times.

It is evident that the reference Zener diode CR2 supplies a "reference" potential to both the +5 volt and the +18 volt regulating circuits. Zener diode CR1 provides a +18 volt operating potential to both differential comparators, the comparator Z1 in the +18 volt regulator circuit and comparator Z2 in the +5 volt regulating circuit.

(b) +18 Volt Regulator Circuit. - The +18 volt regulating circuit is similar to the +5 volt regulating circuit in many respects. A 24 volt dc supply

voltage from the ac power supply is applied to the emitter of series "switching" regulator A1A3PS1A2Q1 and also to the switch driver stage Q1 and Q2. Drive pulses supplied from differential comparator Z1 trigger the current amplifier Q1 and in turn the switch Q2 to control the "switching" regulator. Zener diode CR3 provides a "dc restoration" function to assure "turn-off" at switch Q2 in response to the above-ground comparator pulse train. The regulator output voltage at the junction of resistors R17 and R18 is sampled and applied to the differential comparator Z1. Comparator Z1 compares the sampled voltage with a fixed reference voltage contributed by Zener diode CR2, and produces a "switching-control" pulse train which is applied to the base of switch regulator A1A3PS1A2Q1 via the switch driver stage Q1 and Q2. The pulse width decreases when the sampled output voltage exceeds the reference voltage and the width increases when the sample voltage is less than the reference voltage. In this manner, the on time of the switch regulator is varied to correct the output voltage and maintain it at a constant +18 volts.

Emitter-follower Q3 receives a 12.5 kc "sync" pulse train which is applied to the differential comparator Z1 to stabilize the regulator and improve its operation. Zener diode CR1 provides a regulated +18 volt potential for the operation of comparator Z1 and also for the operation of comparator Z2 in the +5 volt regulator circuit.

The dc pulse output from switching regulator A1A3PS1A2Q1 goes through a low-pass LC filter network consisting of L1 and C3, C8, and C9. A "commutating" diode CR4 provides a circuit return path from L1, through C8 (and C9) and back to L1. During the switch regulator A1A3PS1A2Q1 off intervals, the collapsing field of inductor L1 charges capacitor C8 (and C9) via the diode return circuit. In this manner, the charge at C8 is maintained during the regulator off periods to assure adequate regulator output current to the load at all times.

(3) +15 VOLT REGULATOR A3A2. - The +15 volt regulating circuit employs conventional regulation methods. Series regulator A1A3PS1A2Q3 is conducting at all times, the degree of conduction being controlled by amplifier Q1. A sample of the +15 volt output voltage is obtained at the junction of resistors R7 and R8. The sample voltage is compared with a fixed reference voltage from Zener diode CR2 by the differential amplifier stage Q2 and Q3. The collector of Q2 drives the base of Q1 and therefore controls the series regulator A1A3PS1A2Q3. When the sampled output voltage exceeds the reference voltage, the differential amplifier drives Q1 to increase the voltage dropped across the series regulator. When the sampled voltage is less than the reference voltage, Q1 decreases the voltage dropped across it. In this manner, the conductance of series regulator A1A3PS1A2A3 is controlled to correct the output voltage and maintain a constant +15 volt potential at the regulator output. Zener diode CR1 establishes a stable bias voltage at the emitter of Q1.

(4) +125 VOLT SUPPLY A1. - The +125 volt supply is contained in a sealed module and cannot be subjected to trouble shooting techniques except at the external connections. Operating power for the regulator is supplied from the +15 volt regulator circuit and applied to terminal E1 (see figure 4-48). The +125 volt output is available at terminal E3.

b. PRELIMINARY CHECK. (See figure 4-49.) - With power off, make a preliminary check of the power supply module before beginning trouble shooting, with emphasis on the following:

- (1) Seating of the plug-in module on the receiver deck.

(2) Cable connections (if any) attached to the module.

(3) Condition of fuses F1, F2, and F3.

c. TEST EQUIPMENT. - Use Multimeter AN/USM-116 or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figures 5-46, 5-47, and 5-48.) - Trouble shooting the power supply module consists of measuring the various output voltages at the test points provided.

WARNING

Potentials as high as 125 volts are present in power supply circuits. Avoid contact.

(1) Connect dc voltmeter to test point J3(TP). Meter should read +125 vdc, minimum.

(2) Connect meter to test point J2(TP). Meter should read +18 vdc.

(3) Connect meter to test point J1(TP). Meter should read +15 vdc.

(4) Connect meter to test point J5(TP). Meter should read +5 vdc.

WARNING

Potentials as high as 125 volts are present in the power supply circuits. Use caution.

4-28. POWER SUPPLY DECOUPLING BOARDS A1A2A8 AND A1A3A3. (See figure 4-50.)

Two power-supply decoupling boards are incorporated in the receiver to provide circuit isolation between various modules which receive their operating voltages from a common power-supply output termination. In addition, one decoupling board contains a meter rectifier circuit to operate the front panel signal-level meter A1A1M1.

a. DESCRIPTION. - The front-deck decoupling board (A1A2A8) contains LC single section decoupling circuits for the +18 volt dc power supply output voltage. It also contains the audio output transformer (T1) for the PHONES jack A1A1J2 output circuit and a meter rectifier (CR1) and multiplier resistor (R2) for the signal-level panel meter (A1A1M1). The rear-deck decoupling board (A1A3A3) contains LC single section decoupling circuits for the +18 volt and the +24 volt dc power supply output voltages and an RC decoupling circuit for the +125 volt dc output voltage.

(1) FRONT-DECK DECOUPLING BOARD A1A2A8. - This circuit board, in addition to containing the PHONES jack output transformer and the panel meter rectifier circuit, contains four low-pass single section LC filters. The following list identifies the decoupling filter circuit and the board output terminal with the module circuit supplied.

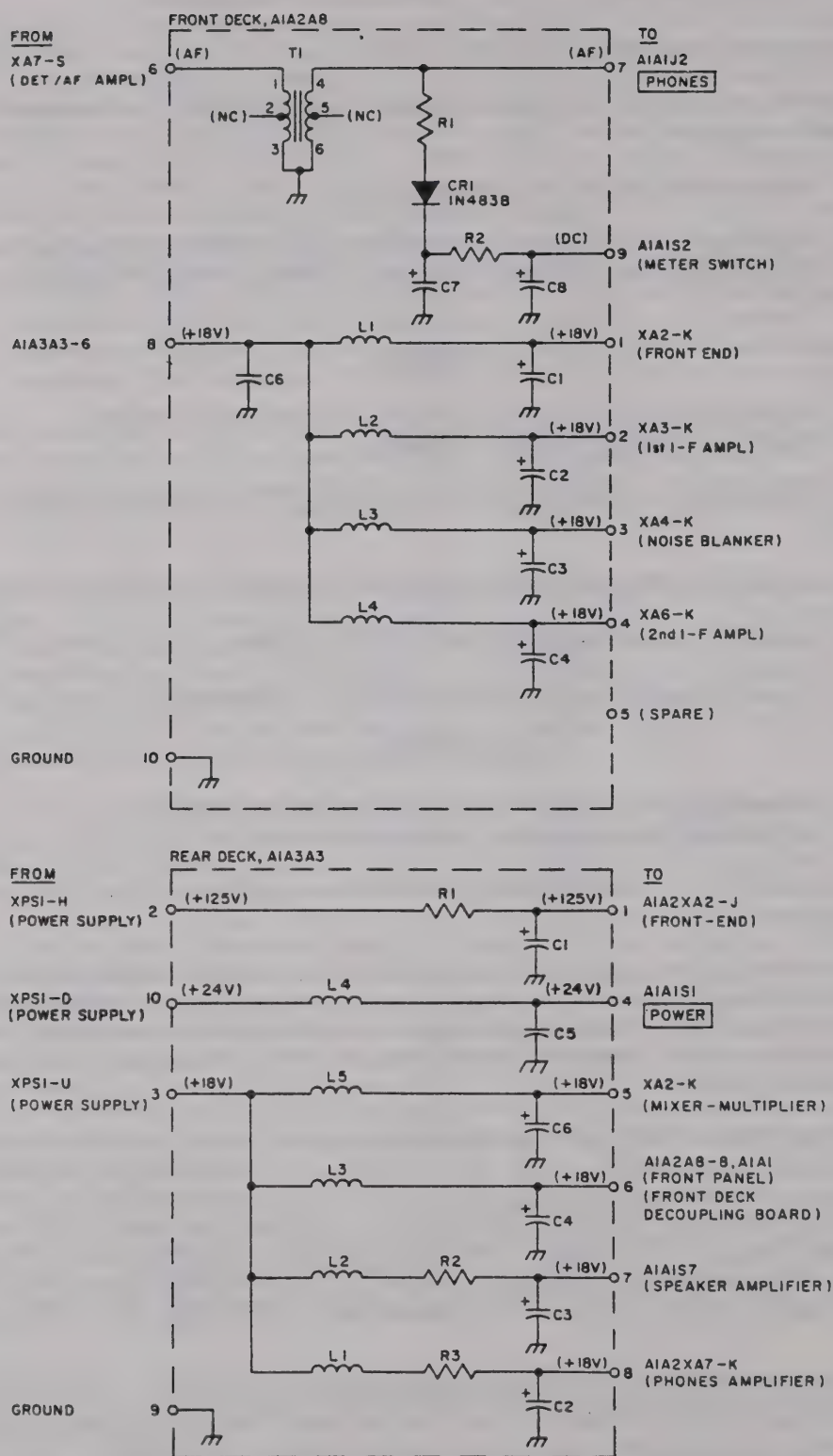


Figure 4-50. Power Supply Decoupling Boards A1A2A8 and A1A3A3,
Simplified Schematic Diagram

<u>Output Voltage</u>	<u>Output Terminal</u>	<u>Decoupling Circuit</u>	<u>Module Circuit Supplied</u>
+18	1	L1, C1	Front End, A1A2A2
	2	L2, C2	First I-F Amplifier, A1A2A3
	3	L3, C3	Noise Blanker, A1A2A4
	4	L4, C4	Second I-F/AGC Amplifier, A1A2A6

Output transformer T1, located on the front-deck decoupling board, supplies audio output signals from the detector/af amplifier module A1A2A7 to the PHONES jack A1A1J2 on the receiver front-panel. Diode CR1 receives a portion of the audio output signal from transformer T1, via resistor R1, and functions as a meter rectifier for the signal-level panel meter A1A1M1. Resistor R2 serves as the meter multiplier and also forms a low-pass RC filter with capacitors C7 and C8.

(2) REAR-DECK DECOUPLING BOARD A1A3A3. - This circuit board contains five low-pass single section LC filters for decoupling the +18 volt dc and the +24 volt dc power supply circuits, and a single RC filter to decouple the +125 volt dc supply circuit. The following list identifies the filter circuits and the module circuit to be decoupled.

<u>Output Voltage</u>	<u>Output Terminal</u>	<u>Decoupling Circuit</u>	<u>Module Circuit Supplied</u>
+125 v	1	R1, C1	Front End, A1A2A2
+18 v	5	L5, C6	Mixer/Multiplier, A1A3A2
	6	L3, C4	Front Deck Decoupling Board A1A2A8 and Front Panel A1A1
	7	L2, R2, C3	Speaker Amplifier, p/o A1A2A7
	8	L1, R3, C2	Phones Amplifier, p/o A1A2A7
+24 v	9	L4, C5	(Part of Power Supply A1A3PS1)

Resistors are inserted in series with the inductors at the terminal 7 and 8 decoupling filters. This addition extends the filter effective range to form an RC filter for audio frequencies and a more effective LC filter at radio frequencies.

b. PRELIMINARY CHECK. (See figures 5-33 and 5-51.) - With power off, make a preliminary check of the front and rear deck decoupling boards, with emphasis on the following:

- (1) Condition of decoupling board components and printed circuit.
- (2) Load connections to the board terminals.

c. TEST EQUIPMENT. - Use Multimeter AN/USM-116 or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Not applicable.

e. TEST DATA. (See figures 5-33 and 5-51.) - Trouble shooting the front

and rear deck decoupling boards consists of measuring the voltages at the various terminals, at each board.

WARNING

Potentials as high as 125 volts are present in power supply circuits. Avoid contact.

(1) FRONT-DECK DECOUPLING BOARD A1A2A8.

(a) Connect dc voltmeter to terminal 8. Meter should read +18 vdc.

(b) Connect voltmeter, in turn, to terminals 1, 2, 3, and 4. Meter should read +18 volts at each of the terminals.

(2) REAR-DECK DECOUPLING BOARD A1A3A3.

(a) Connect dc voltmeter to terminal 2. Meter should read +125 vdc, minimum.

(b) Connect meter to terminal 1. Meter should read +125 vdc, minimum.

(c) Connect meter to terminal 3. Meter should read +18 vdc.

(d) Connect voltmeter, in turn, to terminals 5, 6, and 7. Meter should read +18 vdc at each of the terminals.

(e) Connect voltmeter to terminal 8. Meter should read +14.5 vdc, minimum.

(f) Connect voltmeter to terminal 9. Meter should read +24 vdc, minimum.

4-29. TTY POWER SUPPLY A1A3Z1.

The TTY power supply module, located underneath the rear deck assembly (A1A3), contains an encapsulated dc-to-dc converter circuit which supplies a loop potential for external teletype equipment. Faulty operation of this module will affect the quality of the teletypewriter print-out or prevent it completely.

a. DESCRIPTION. - The TTY power supply module requires a +24 volt dc supply voltage for operation and provides an output of 120 volts dc at 60 milli-amperes. The output is controlled by the FSK converter output (A1A2A7A2) when the TELETYPE MODE switch (A1A1S4) is in the INT BAT (internal battery) position.

b. PRELIMINARY CHECK. - With power off, make a preliminary check of the TTY power supply module before trouble shooting, with emphasis on the following:

(1) Soldered connections at the module.

(2) Operation of the TELETYPE MODE switch.

c. TEST EQUIPMENT.- Use Electronic Multimeter AN/USM-116 or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the TELETYPE MODE switch as directed.

e. TEST DATA. - Trouble shooting the TTY power supply module consists of measuring the output level.

- (1) Unsolder the connection to terminal E1 on the TTY power supply module.
- (2) Turn the TELETYPE MODE switch to INT BAT.
- (3) Connect the multimeter to the TELETYPE terminals on the front panel.
- (4) The output level should be 0 volt dc.
- (5) Short terminal E1 to ground.
- (6) The output level should be 120 volts dc.

4-30. ANTENNA TRIMMING CIRCUIT A1A1A6. (See figure 5-80.)

The antenna trimming circuit module, located on the front panel assembly (A1A1), contains an antenna transformer for each band on the BAND MC switch, and capacitors to resonate the transformer over the band of frequencies selected. It also contains switches to select the proper combination of transformers and capacitors. Faulty operation of this module will impair receiver performance with antennas other than 50 ohms.

a. DESCRIPTION. - The BAND MC switch selects an antenna transformer for each position, and connects the REACT TRIM trimmer capacitor C2 across the primary of the selected transformer. The HI/MED/LOW switch shunts fixed values of capacitors across the REACT TRIM control and extends its range. In the OFF position of the BAND MC switch, the entire antenna trimming circuit is bypassed.

b. PRELIMINARY CHECK. (See figure 5-80.) - With power off, make a preliminary check of the antenna trimming circuit module before trouble shooting, with emphasis on the following:

- (1) Cable connections attached to module.
- (2) Operation of the BAND MC switch and REACT TRIM, HI/MED/LOW controls.

c. TEST EQUIPMENT. - Use Signal Generator AN/URM-25D and RF VTVM ME-286/U or equivalent. No special tools are required.

d. CONTROL SETTINGS. - Set all controls according to table 3-2. During the test procedure, set the BAND MC switch and REACT TRIM, HI/MED/LOW controls as directed.

e. TEST DATA. (See figure 5-80.) - Trouble shooting the antenna trimming circuit module consists of checking the antenna trimming circuit and noting its effect on the signal passed through it.

(1) Remove the input and output rf cables on the antenna trimming circuit module.

(2) Connect signal generator to the input jack on the module; connect RF VTVM to the output jack.

(3) Set BAND MC switch to 2-4 position. Adjust signal generator for 3 mc output.

(4) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(5) Set BAND MC switch to 4-8 position. Adjust signal generator for 6 mc output.

(6) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(7) Set BAND MC switch to 8-16 position. Adjust signal generator for 12 mc output.

(8) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(9) Set BAND MC switch to 16-30 position. Adjust signal generator for 24 mc output.

(10) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(11) Set BAND MC switch to OFF position.

(12) Vary REACT TRIM and HI/MED/LOW controls. These controls should have no effect on output as measured on RF VTVM.

TM-05866A-15

Figure 4-51

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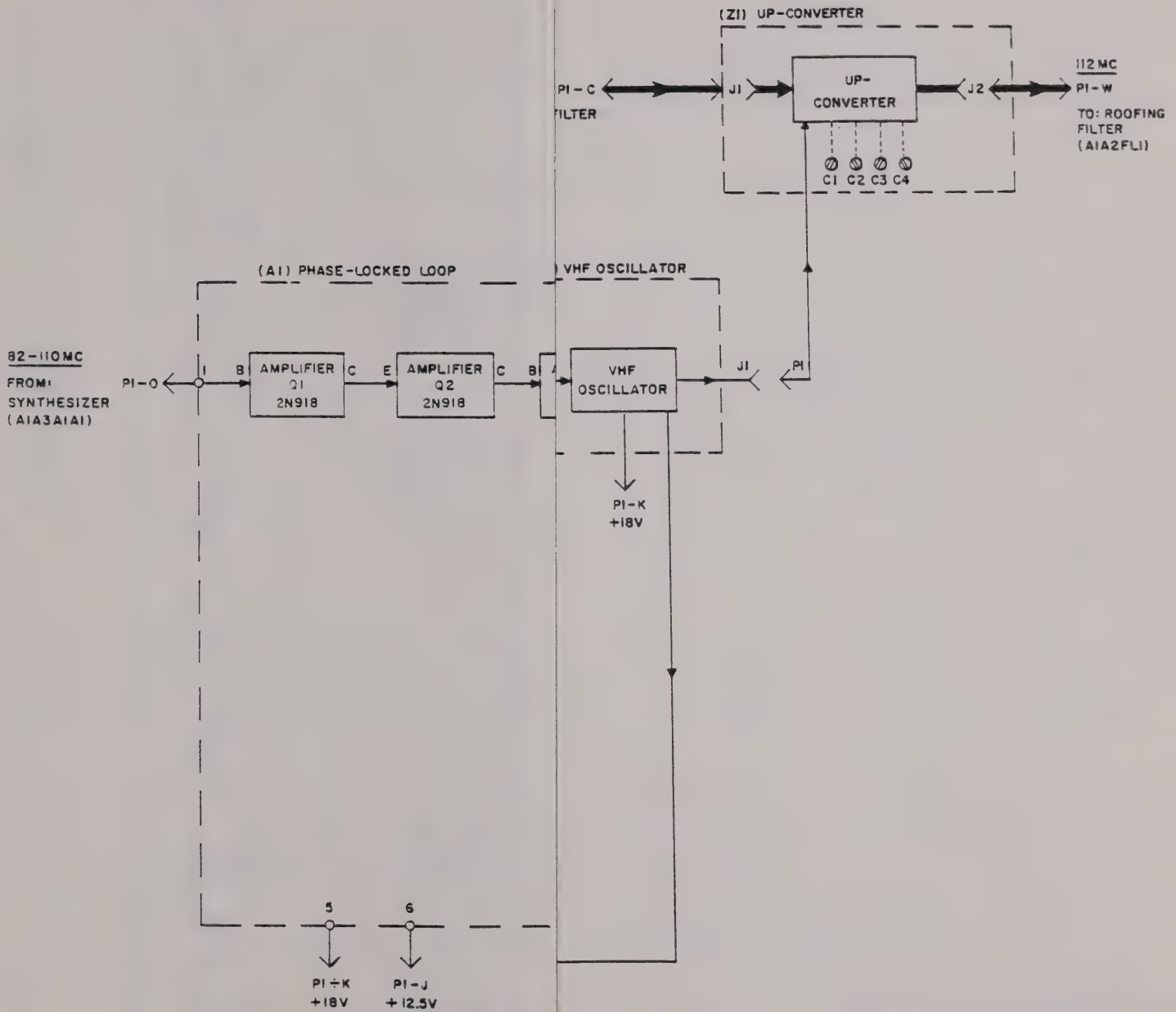


Figure 4-51. Front End AlA2A2, Servicing Block Diagram

4-147/4-148

e. TEST DATA. (See figure 5-80.) - Trouble shooting the antenna trimming circuit module consists of checking the antenna trimming circuit and noting its effect on the signal passed through it.

(1) Remove the input and output rf cables on the antenna trimming circuit module.

(2) Connect signal generator to the input jack on the module; connect RF VTVM to the output jack.

(3) Set BAND MC switch to 2-4 position. Adjust signal generator for 3 mc output.

(4) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(5) Set BAND MC switch to 4-8 position. Adjust signal generator for 6 mc output.

(6) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(7) Set BAND MC switch to 8-16 position. Adjust signal generator for 12 mc output.

(8) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(9) Set BAND MC switch to 16-30 position. Adjust signal generator for 24 mc output.

(10) Vary REACT TRIM and HI/MED/LOW controls. Note effect on output as measured on RF VTVM.

(11) Set BAND MC switch to OFF position.

(12) Vary REACT TRIM and HI/MED/LOW controls. These controls should have no effect on output as measured on RF VTVM.

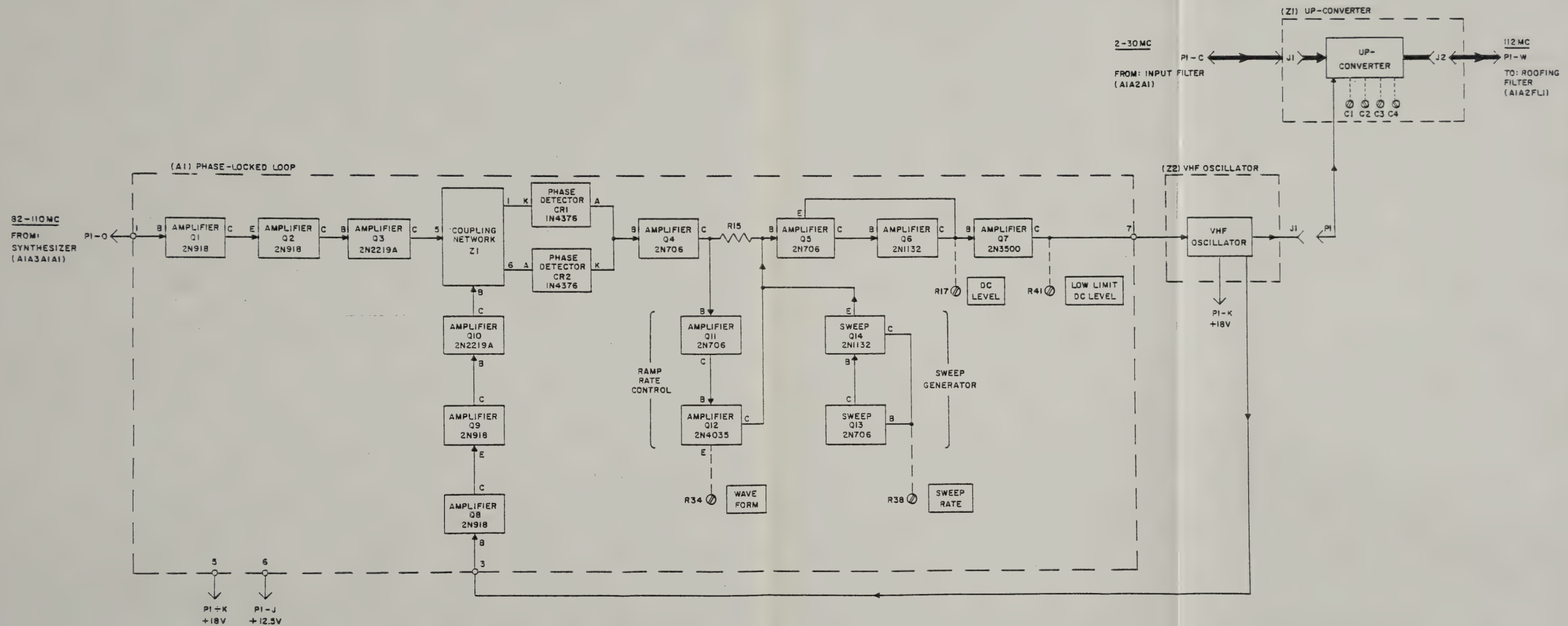


Figure 4-51. Front End AlA2A2,
Servicing Block Diagram

ORIGINAL

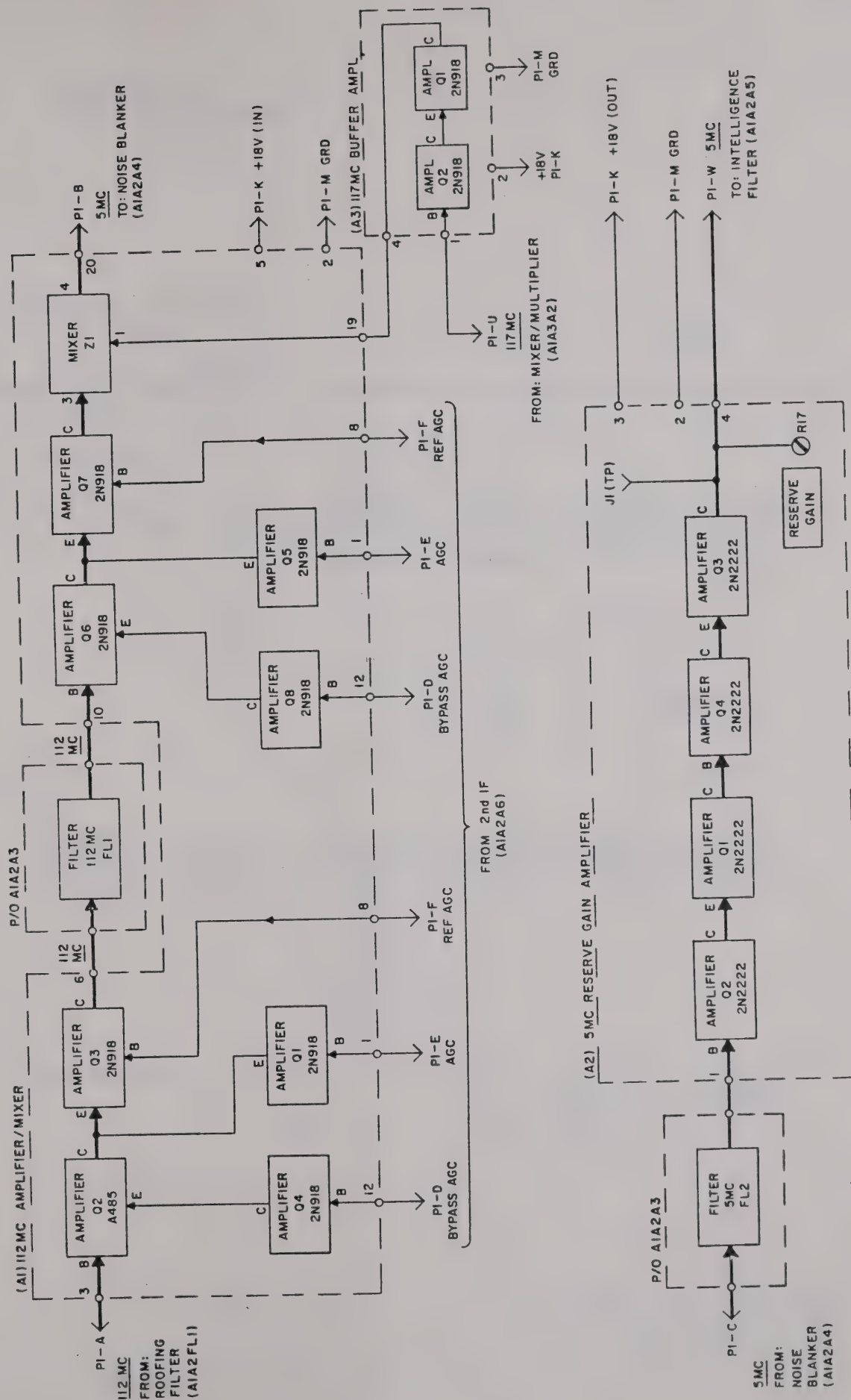


Figure 4-52. First I-F Amplifier AlA2A3,
Servicing Block Diagram

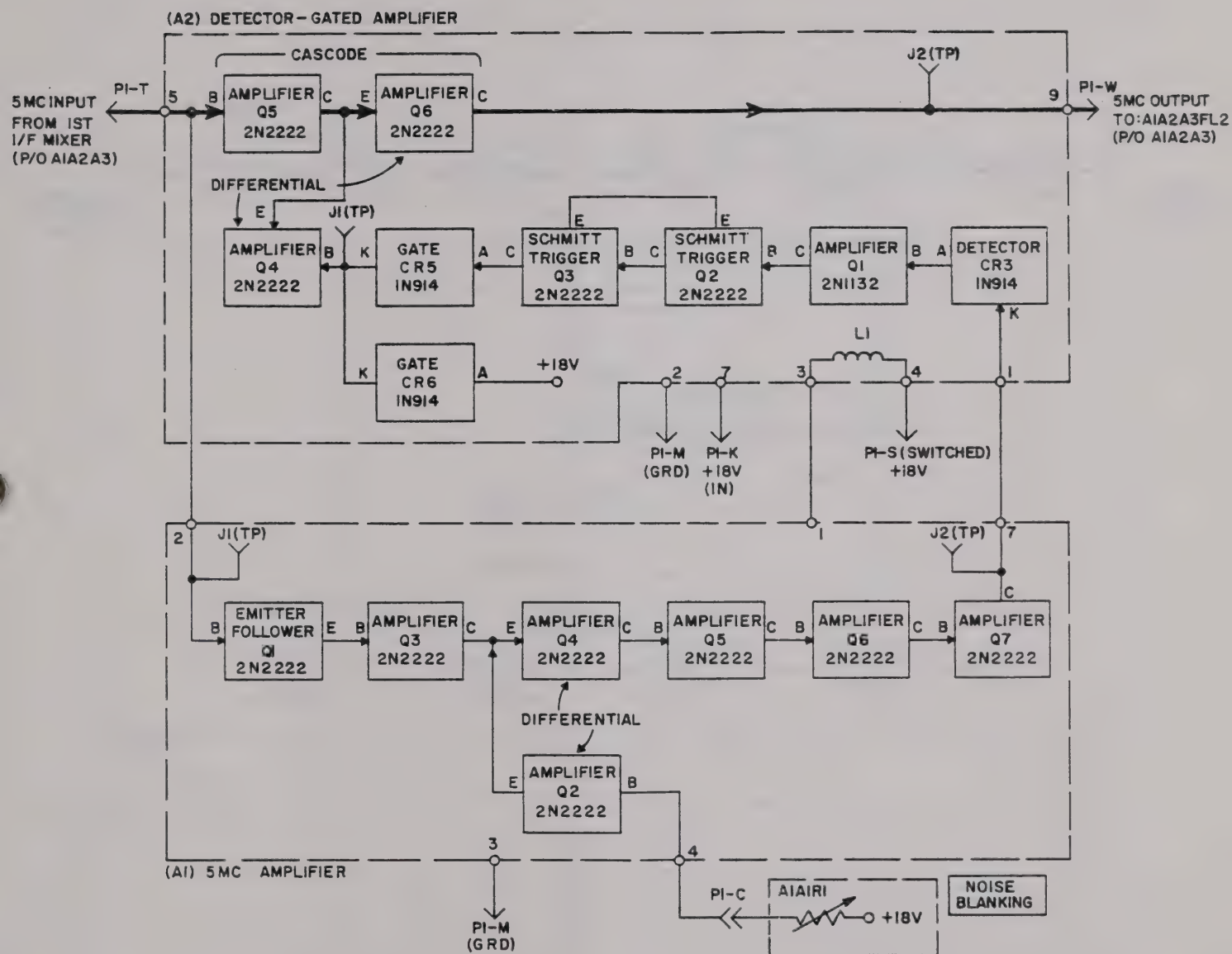


Figure 4-53. Noise Blanker A1A2A4,
Servicing Block Diagram

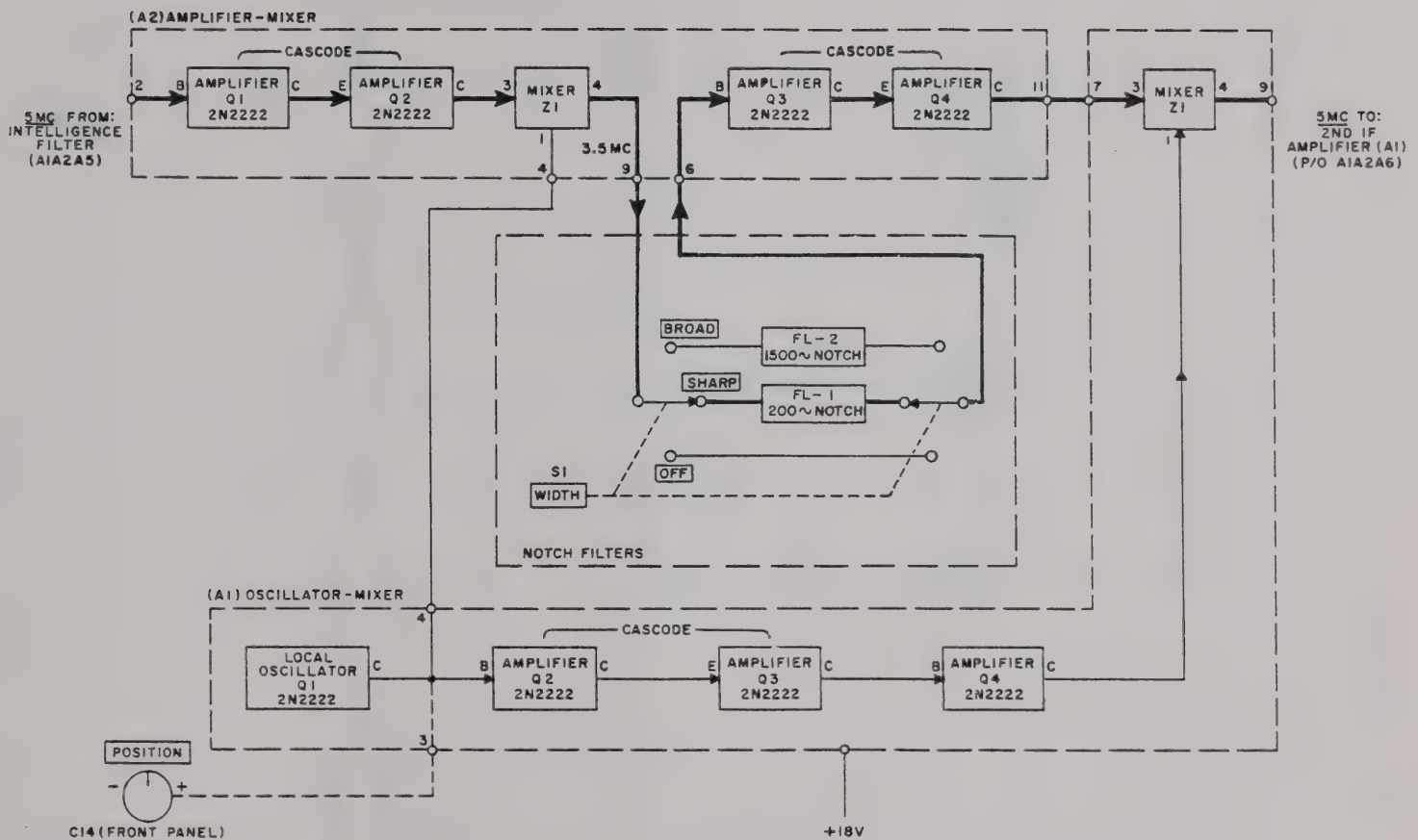


Figure 4-54. Notch Filter A1A1A4,
Servicing Block Diagram

ORIGINAL

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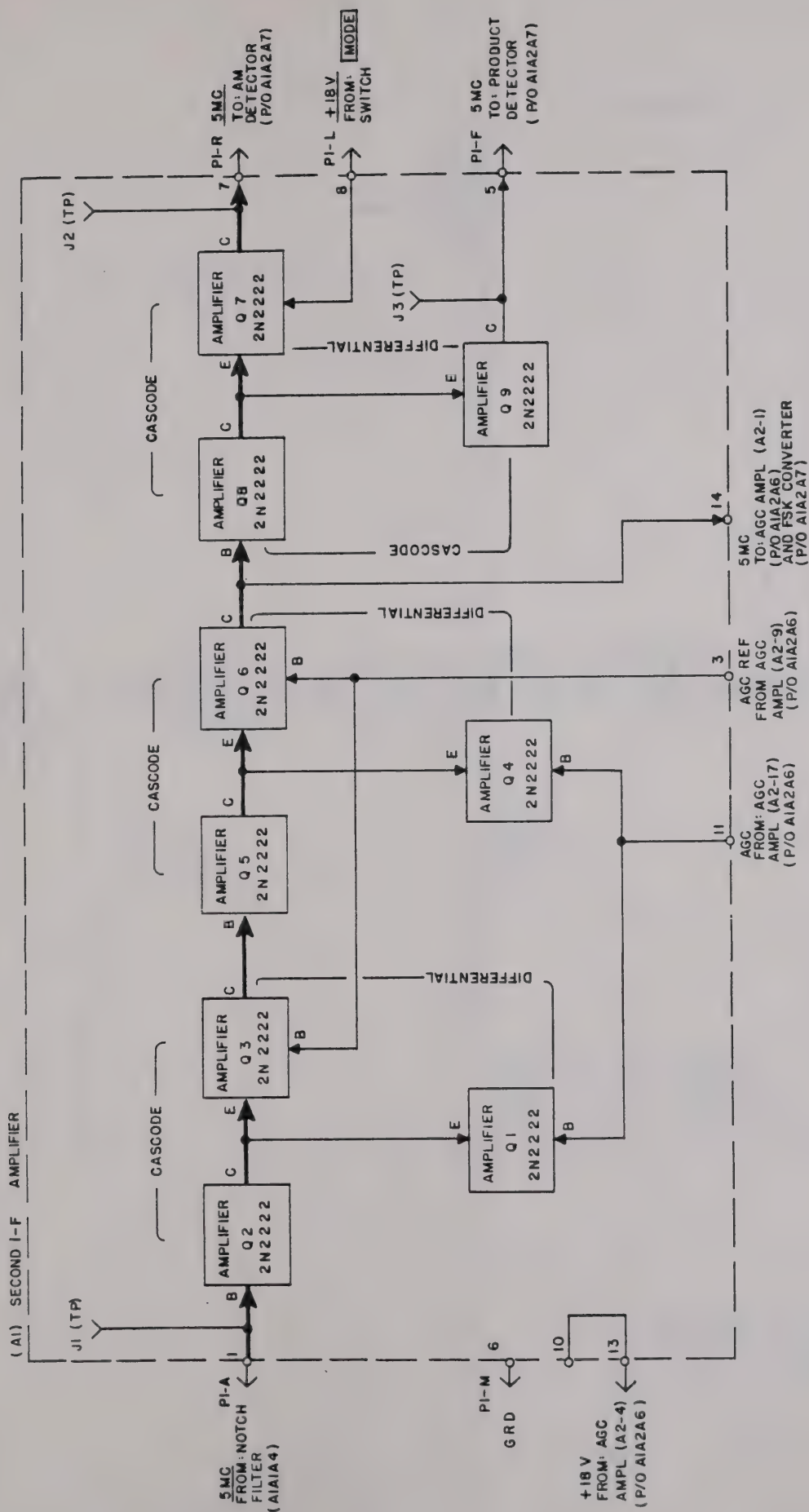


Figure 4-55. Second I-F/AGC Amplifier
A1A2A6, Servicing Block Diagram
(Sheet 1 of 2)

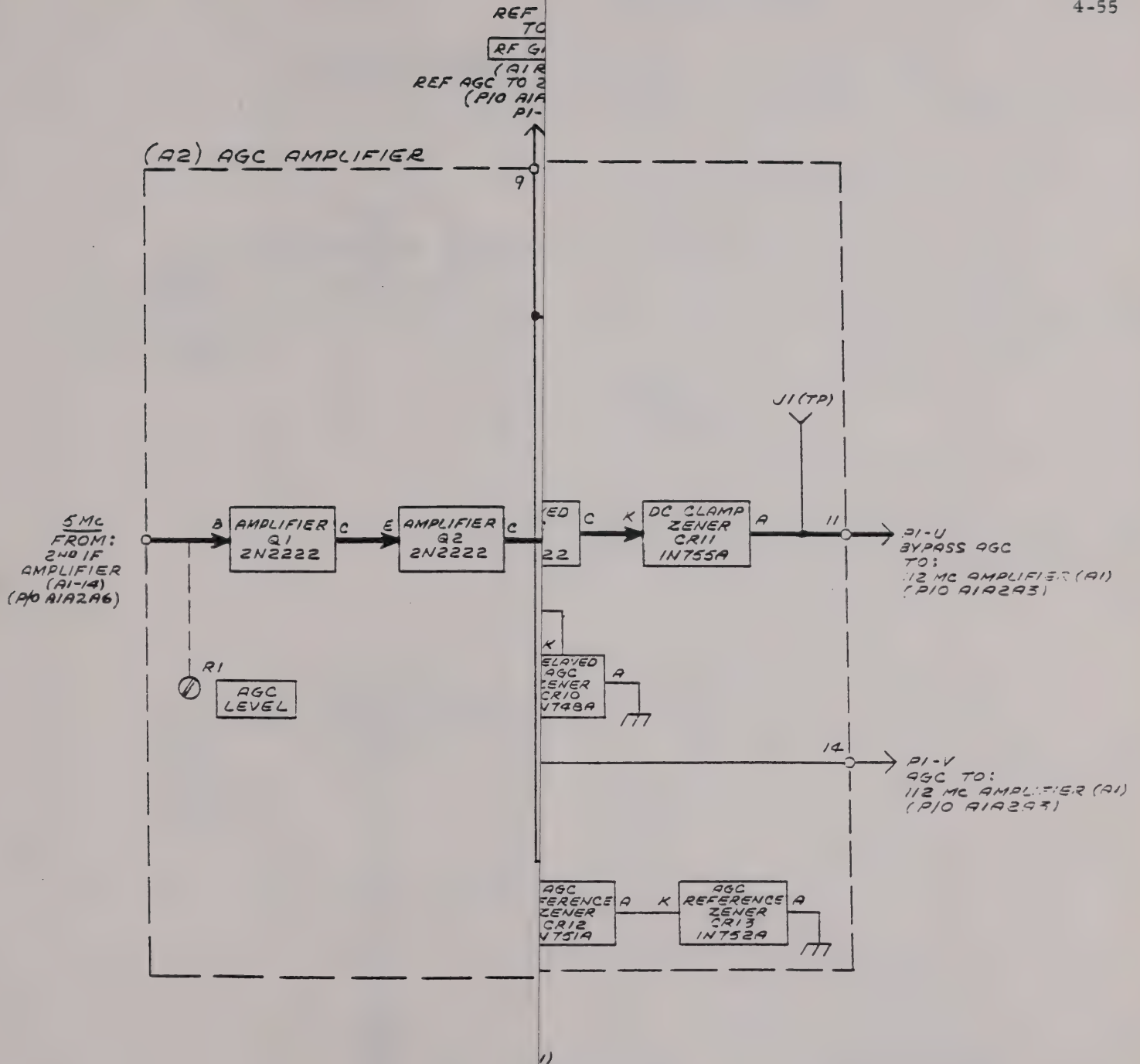


Figure 4-55. Second I-F/AGC Amplifier
A1A2A6, Servicing Block Diagram
(Sheet 2 of 2)

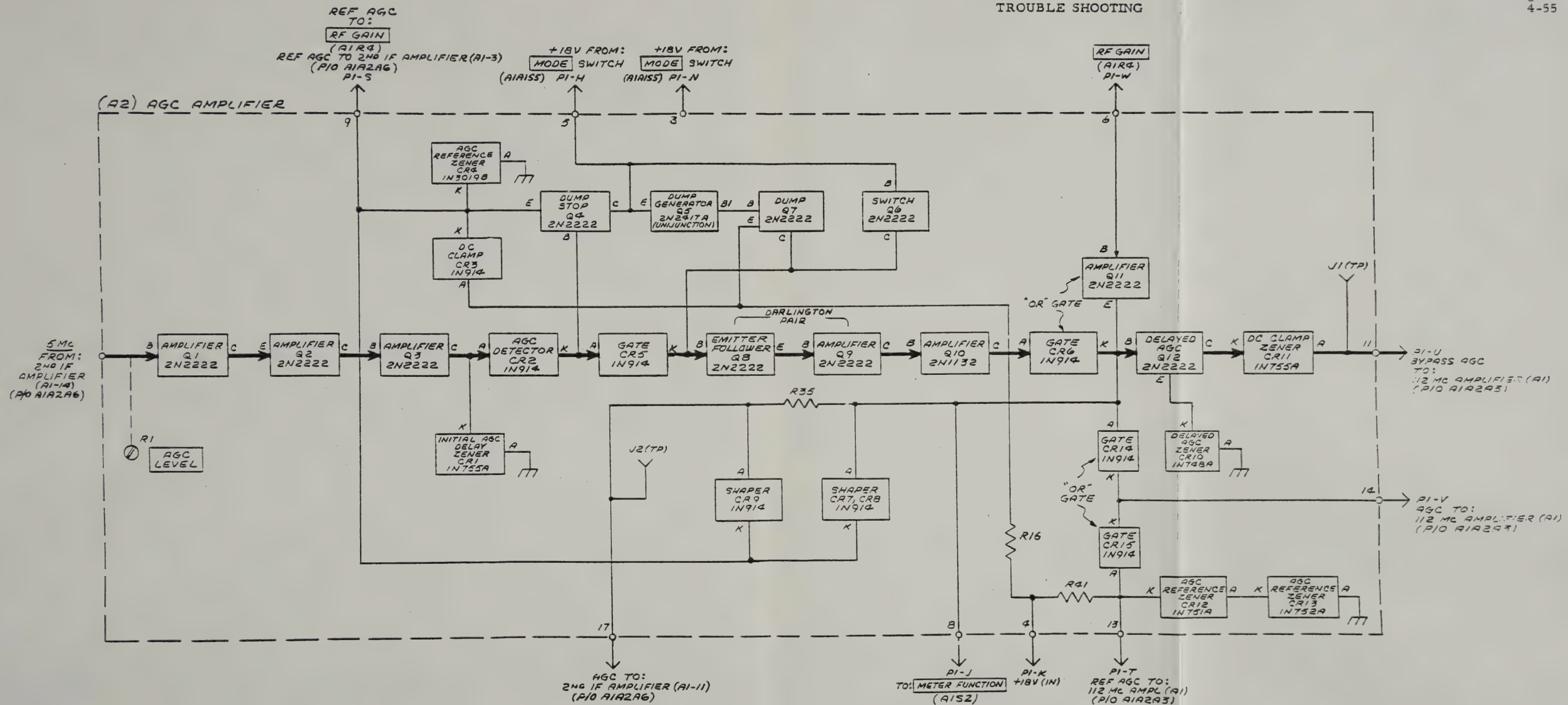
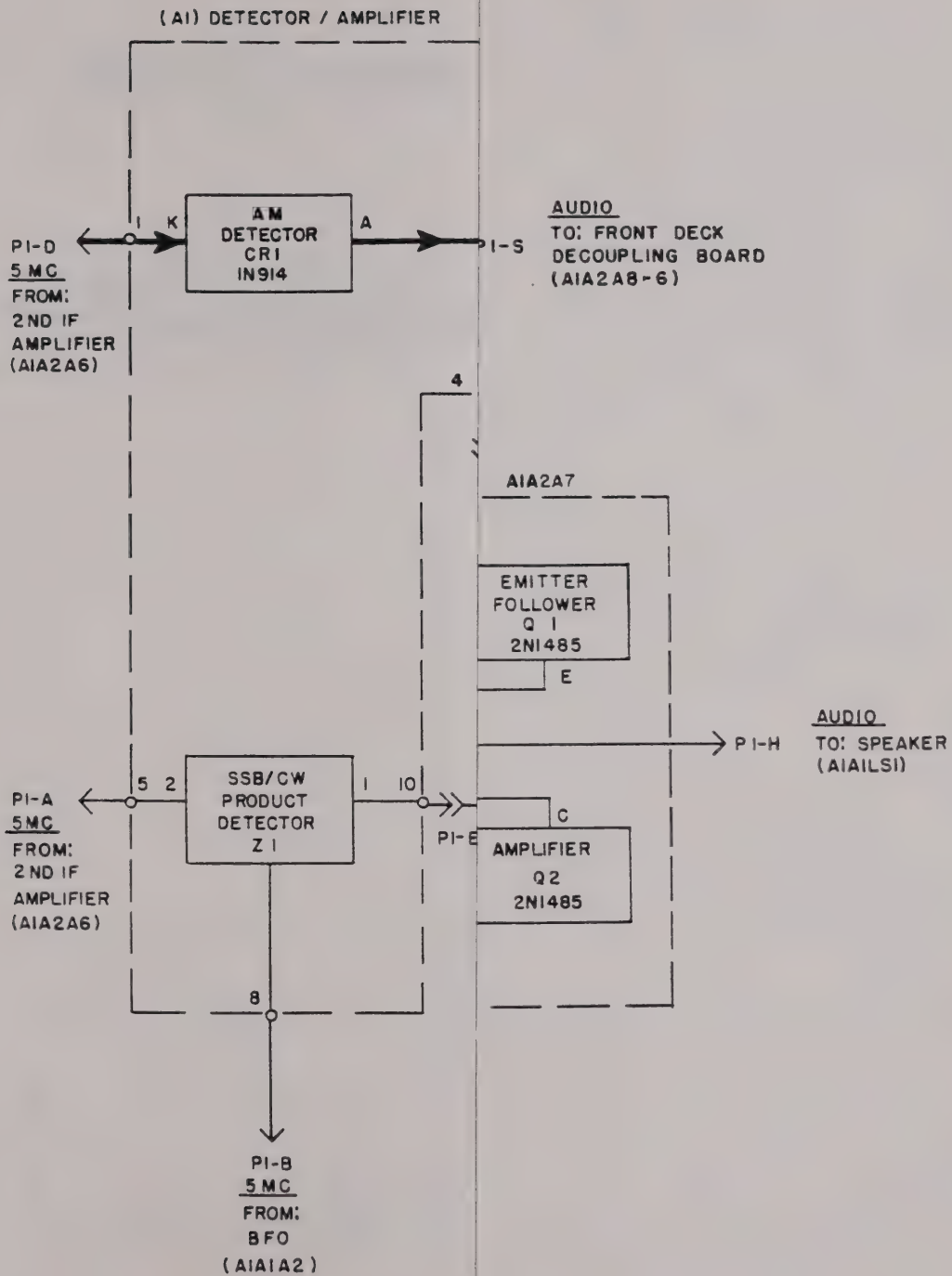


Figure 4-55. Second I-F/AGC Amplifier
A1A2A6, Servicing Block Diagram
(Sheet 2 of 2)

Figure
4-56



Detector/AF Amplifier A1A2A7,
Block Diagram (Sheet 1 of 2)

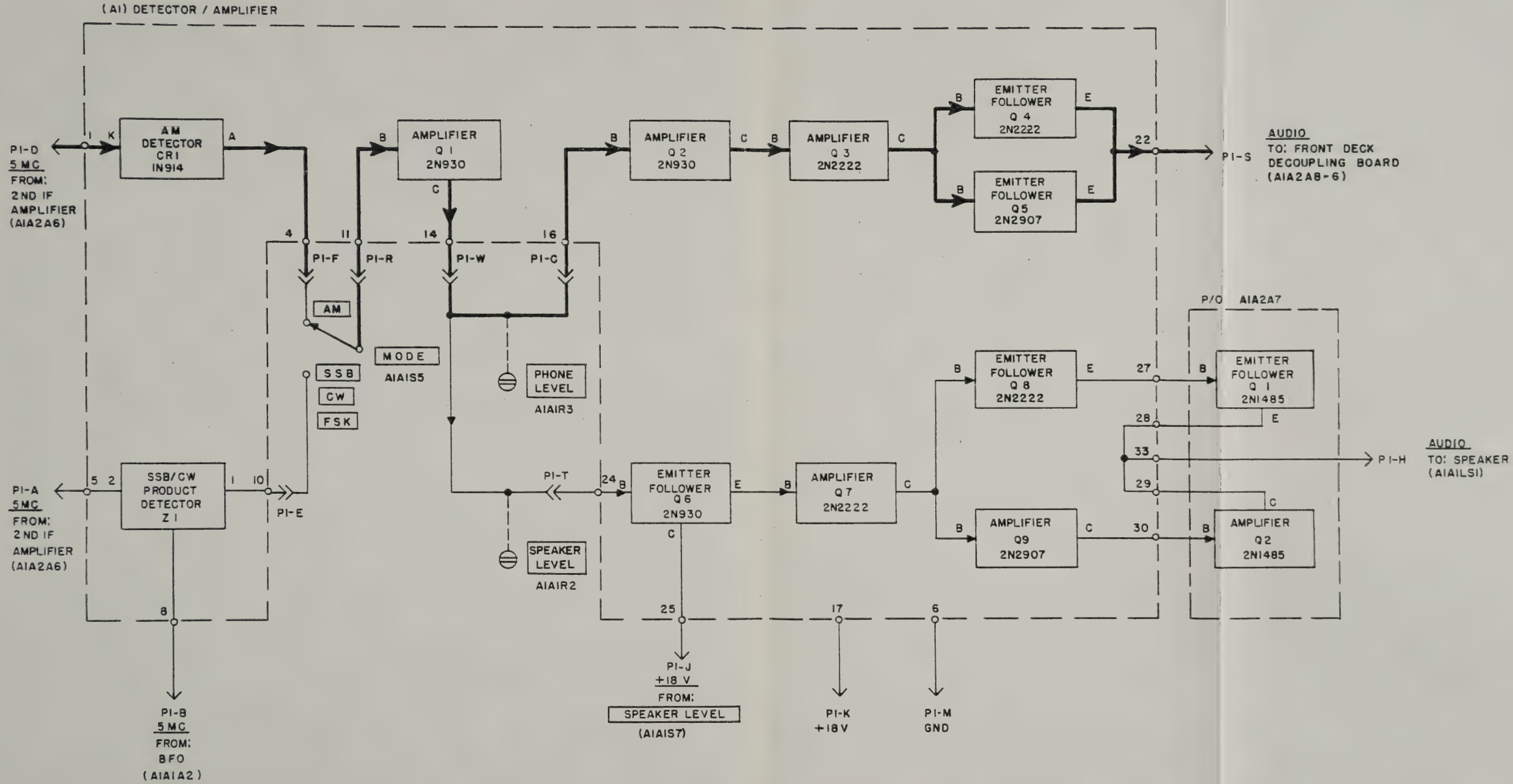


Figure 4-56. Detector/AF Amplifier A1A2A7,
Servicing Block Diagram (Sheet 1 of 2)

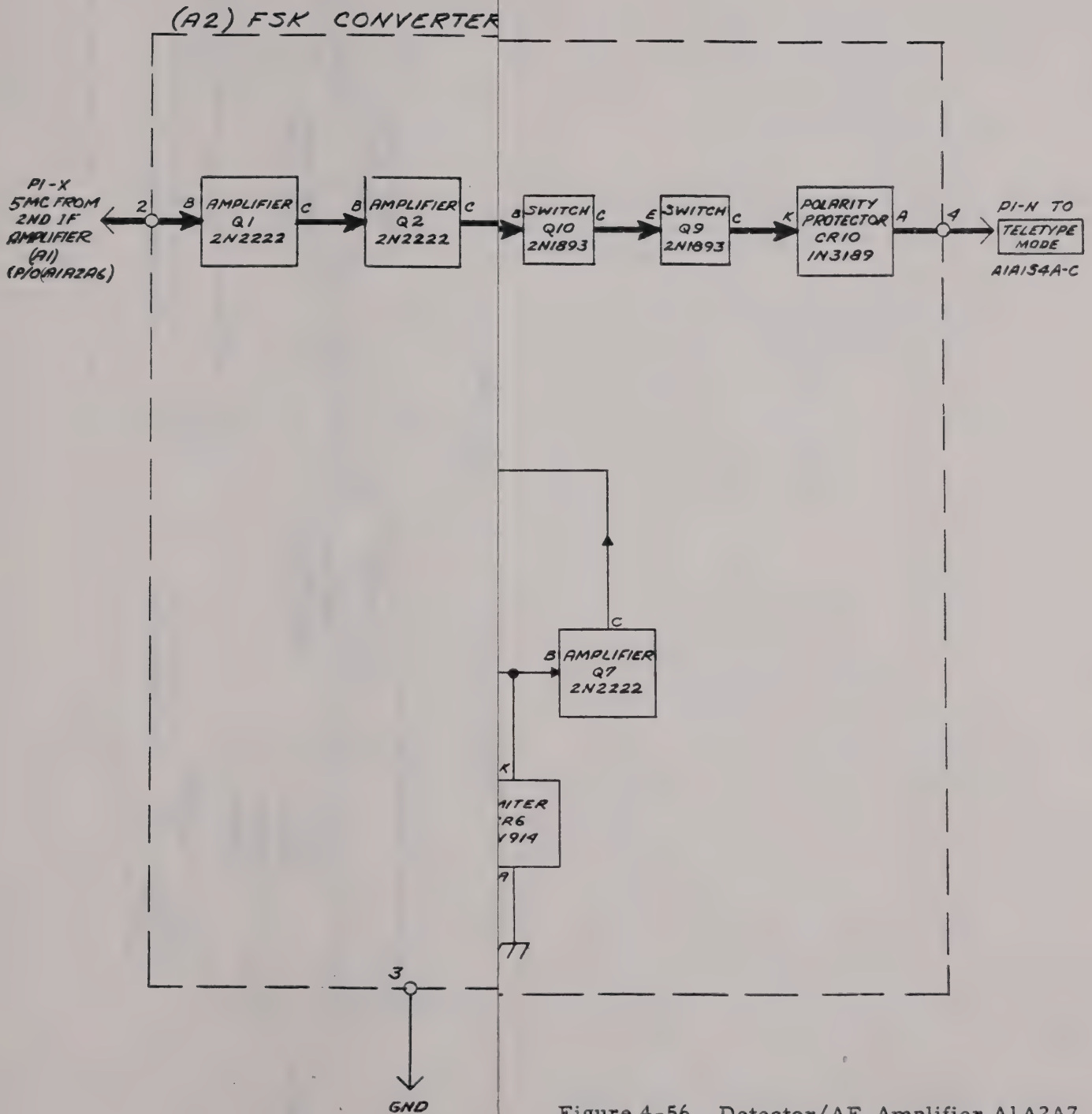


Figure 4-56. Detector/AF Amplifier A1A2A7,
Servicing Block Diagram (Sheet 2 of 2)

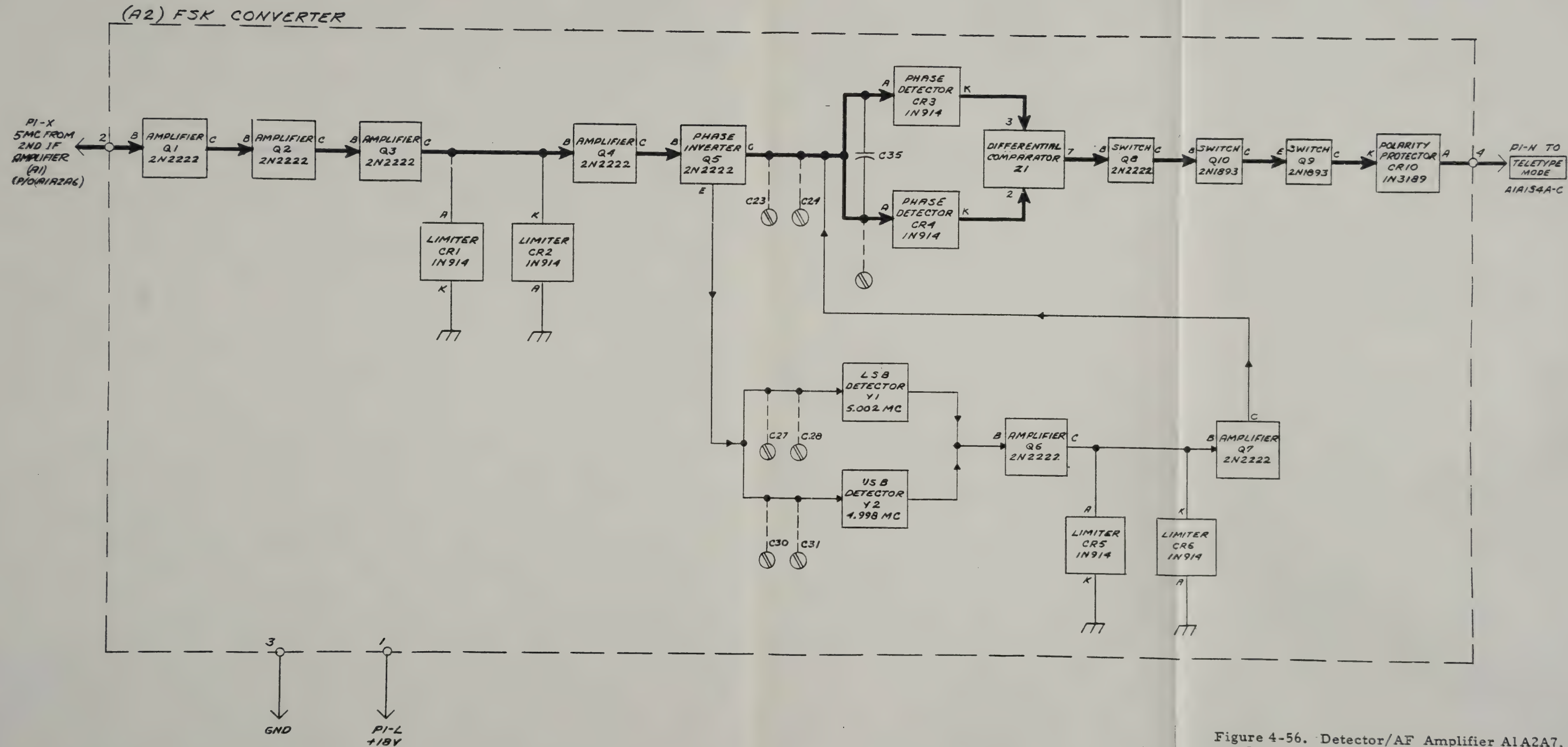
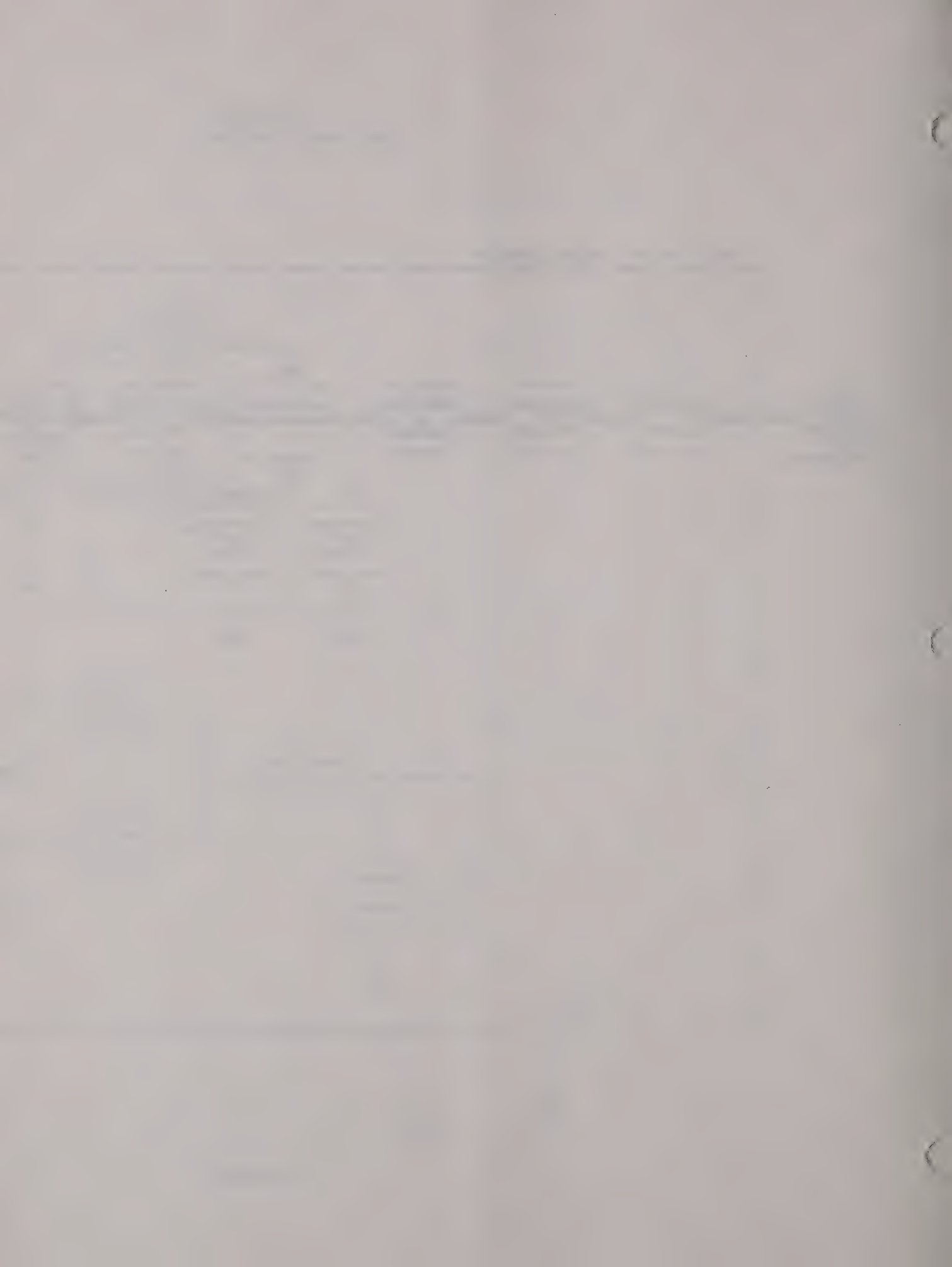


Figure 4-56. Detector/AF Amplifier A1A2A7,
Servicing Block Diagram (Sheet 2 of 2)

ORIGINAL



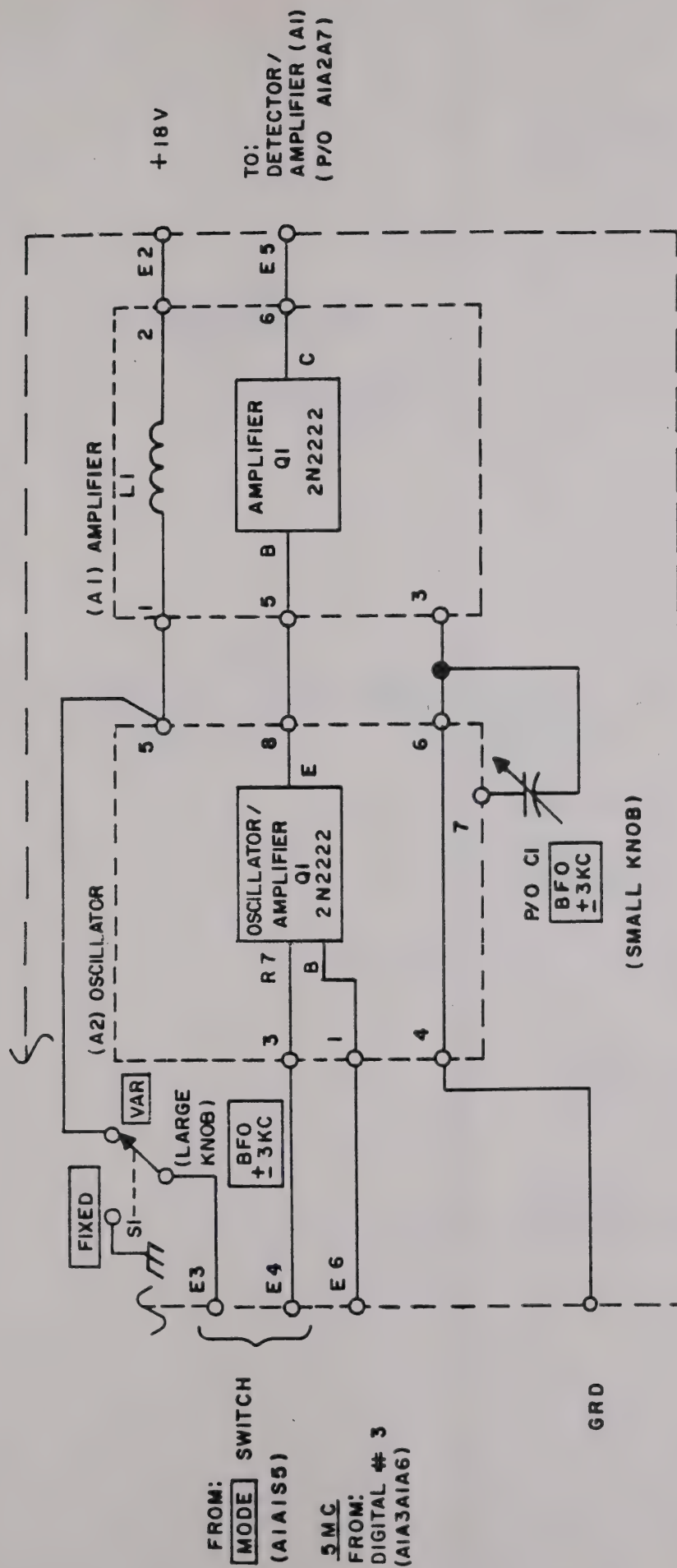


Figure 4-57. BFO A1A1A2,
Servicing Block Diagram

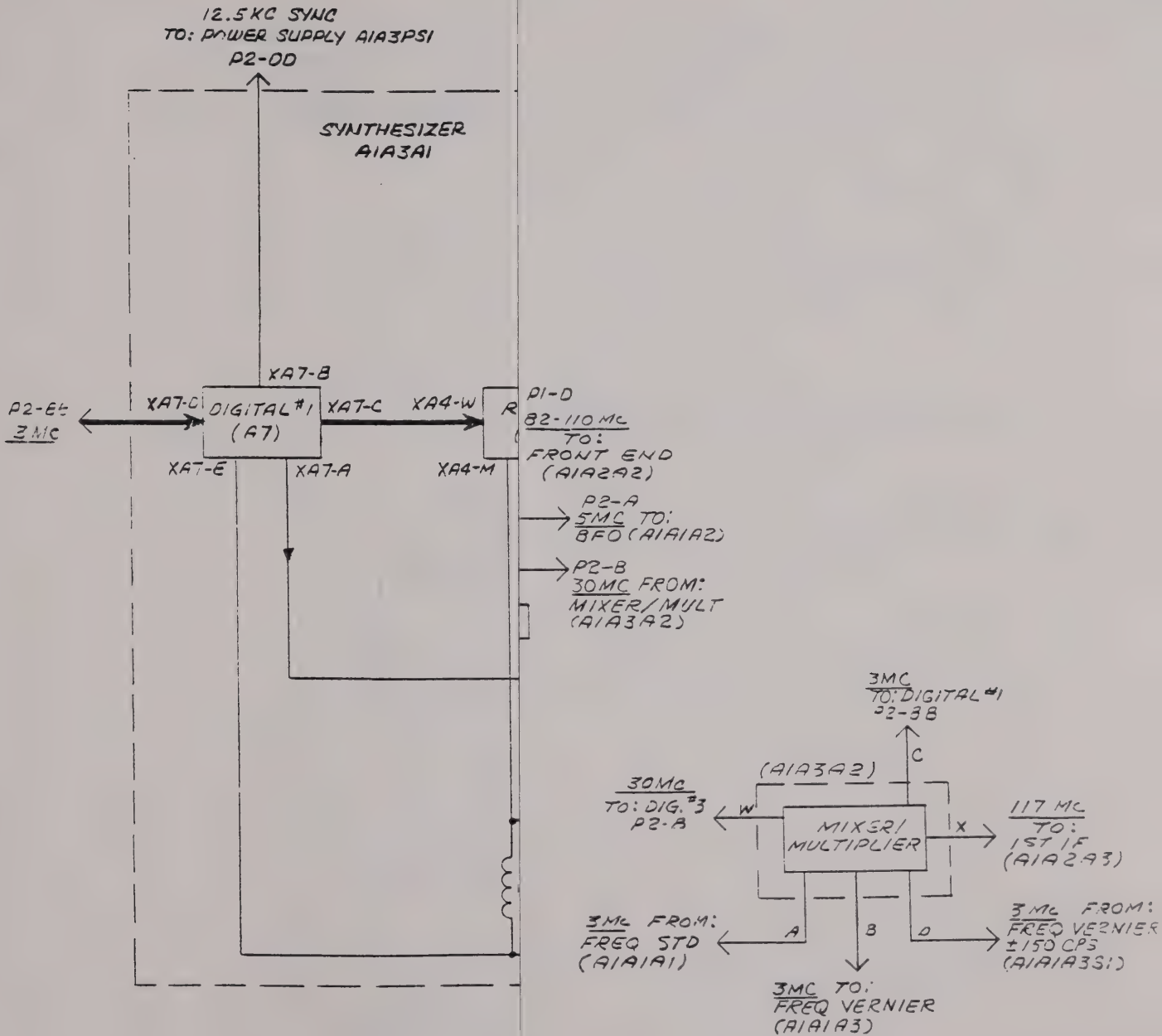


Figure 4-58. Synthesizer A1A3A1,
Servicing Block Diagram

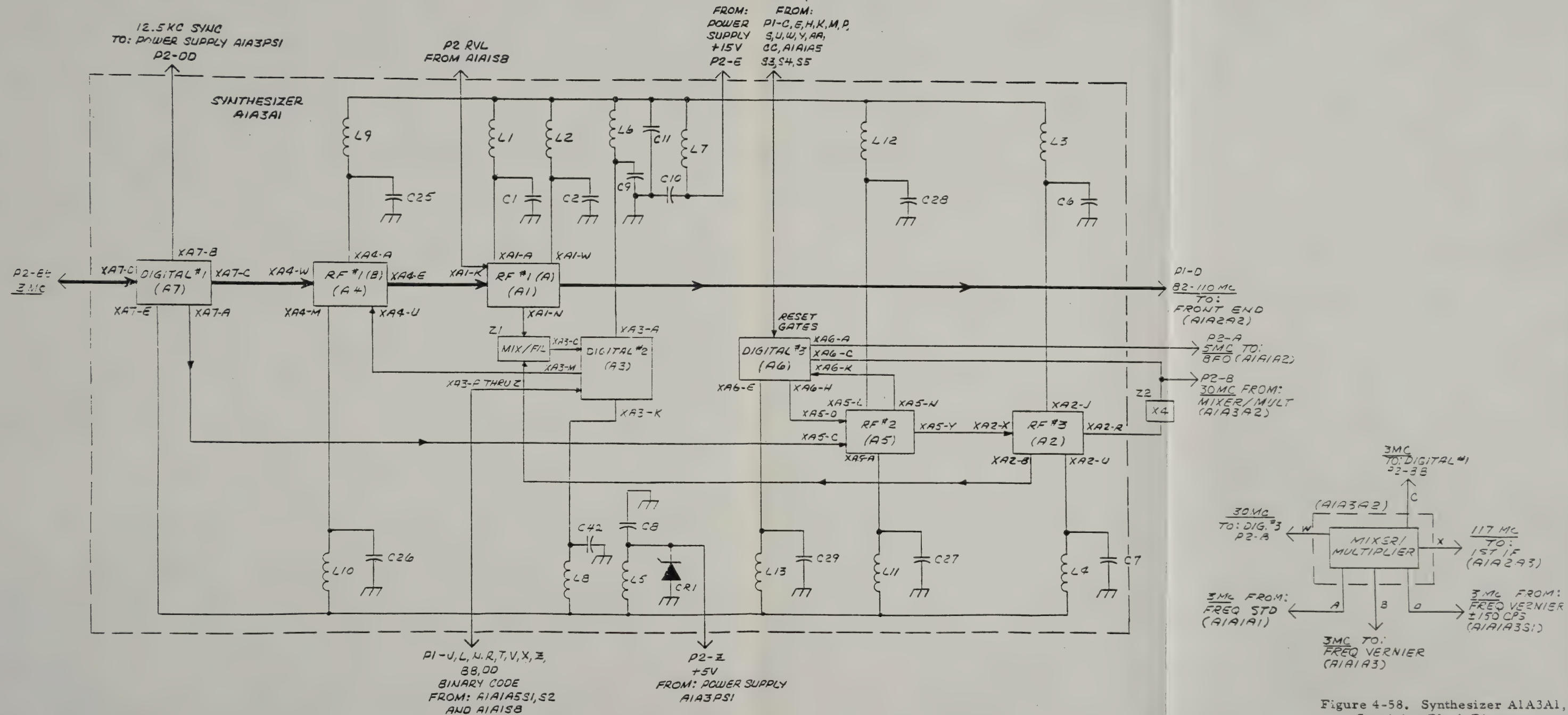
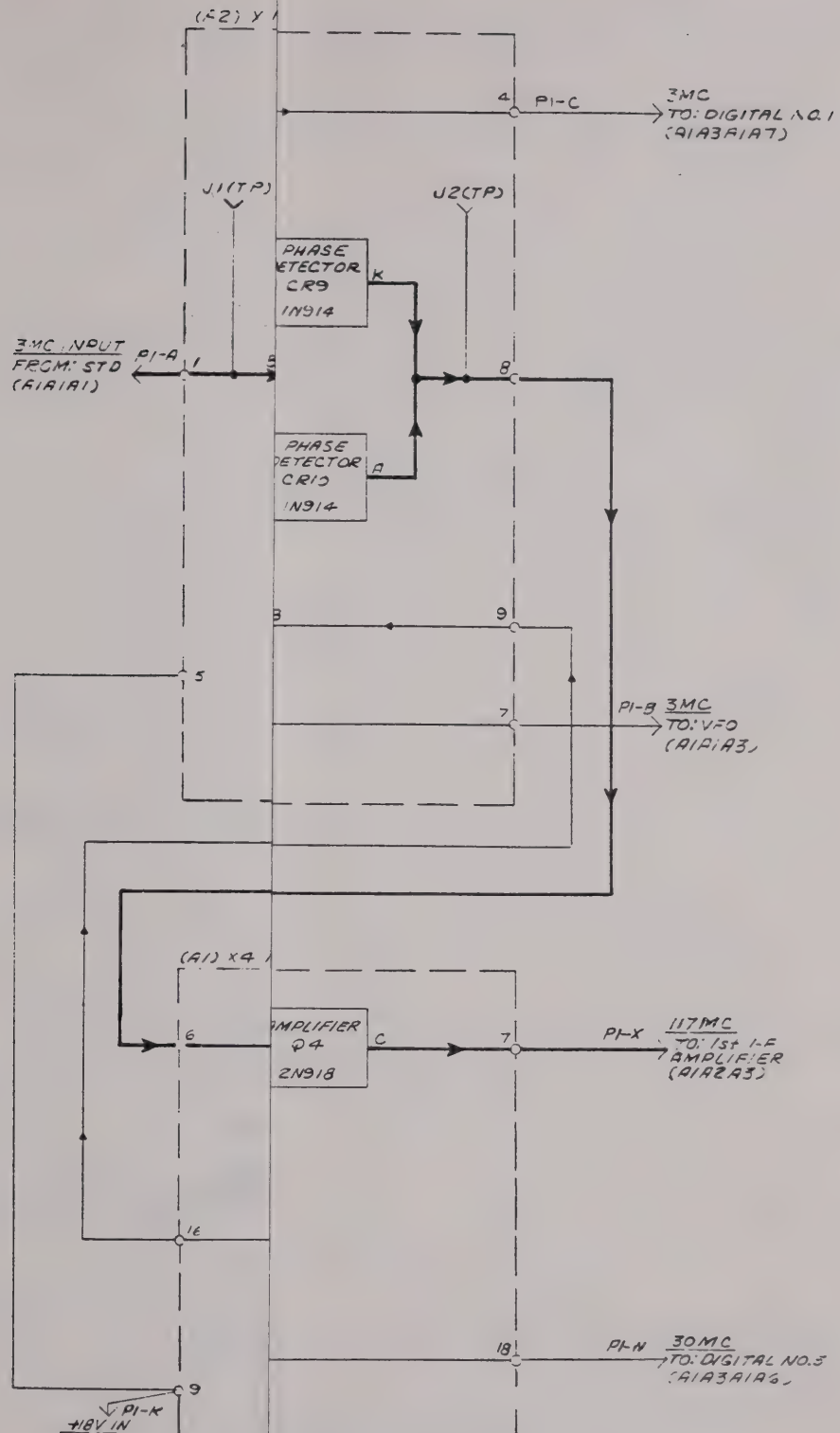
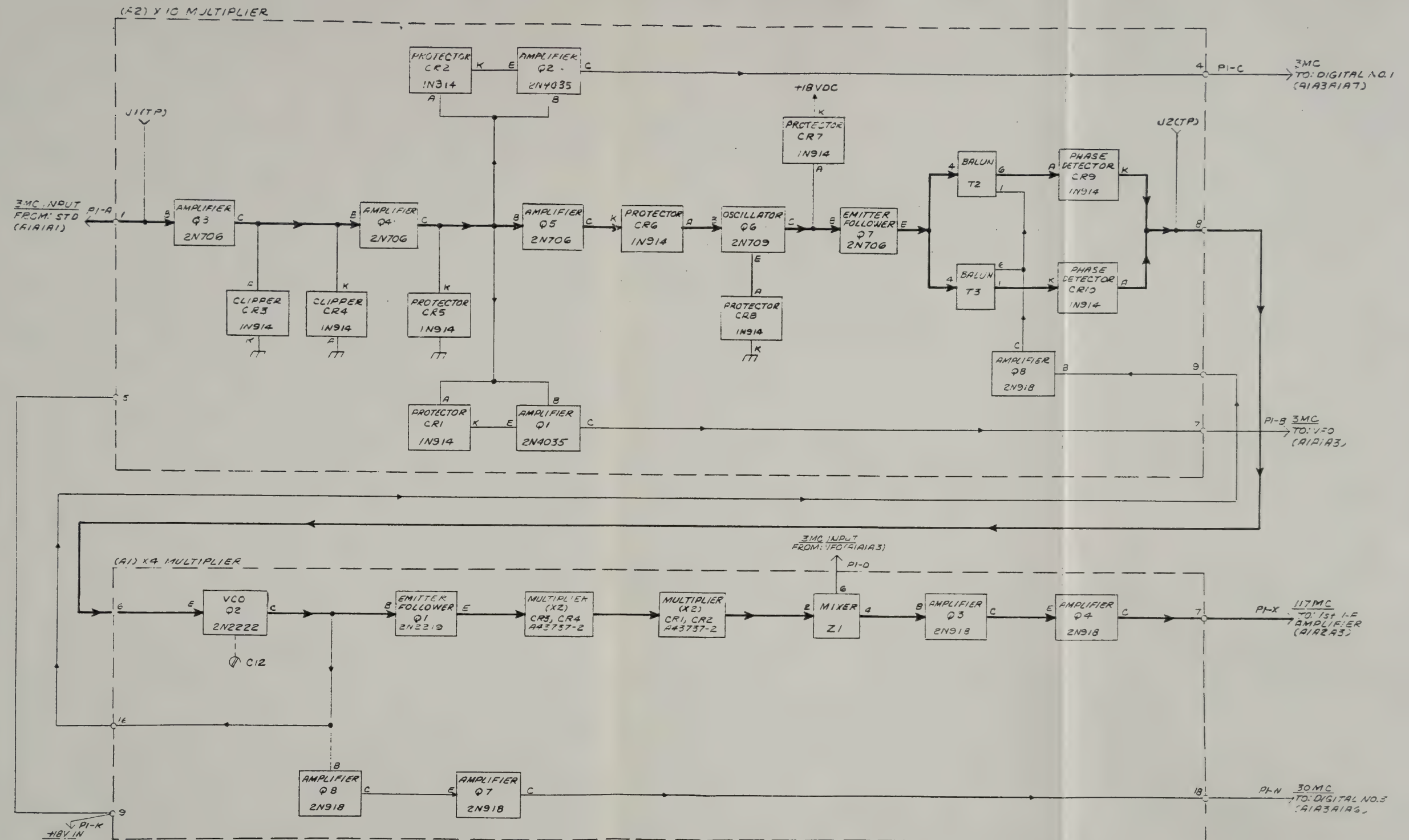


Figure 4-58. Synthesizer A1A3A1,
Servicing Block Diagram

ORIGINAL

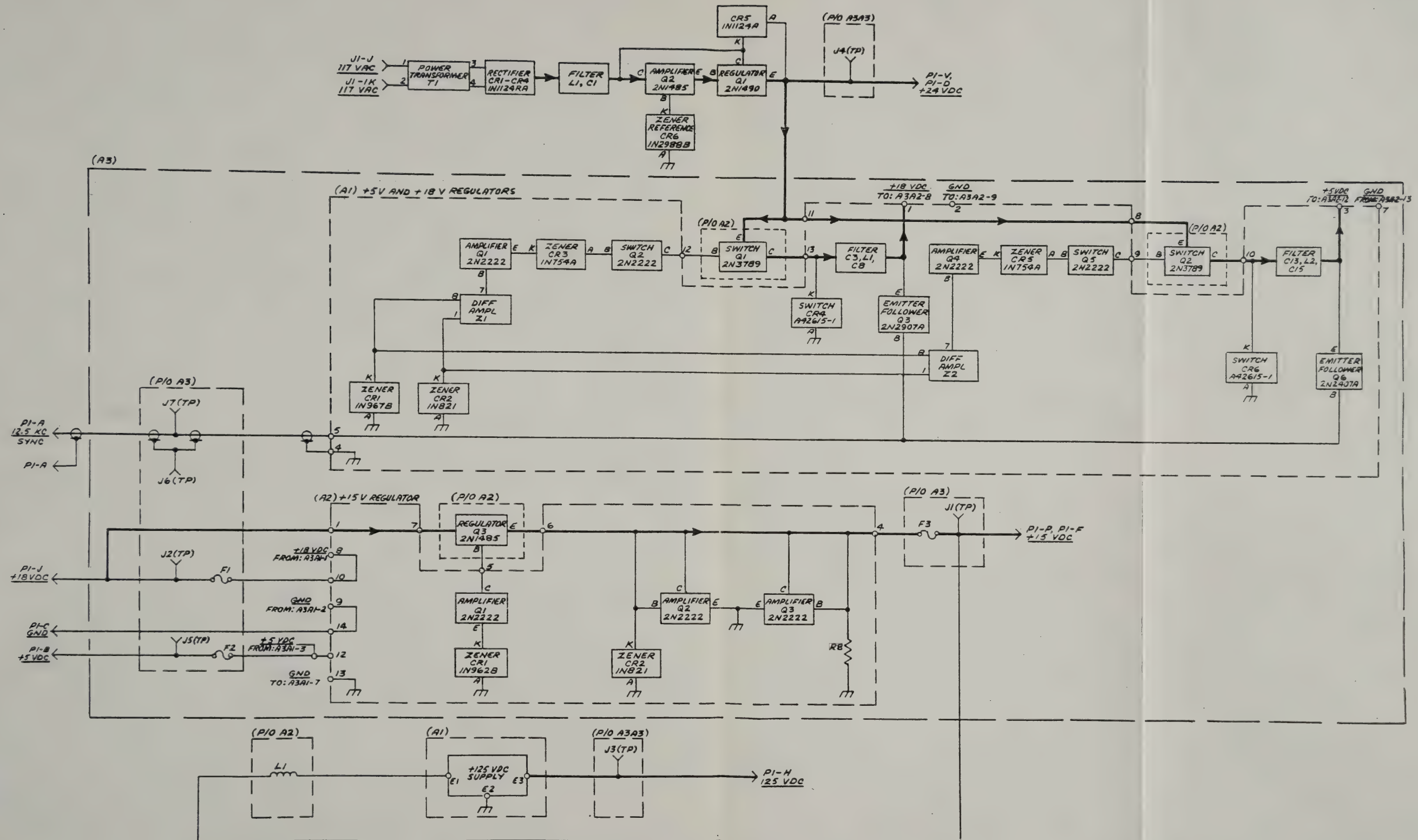
Figure 4-59. Mixer/Multiplier A1A3A2,
Servicing Block Diagram

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Figure 4-59. Mixer/Multiplier A1A3A2,
Servicing Block Diagram

4-60. Power Supply A1A3PS1, Servicing Block Diagram



Figure 4-60. Power Supply A1A3PS1,
Servicing Block Diagram

SECTION 5 MAINTENANCE

5-1. INTRODUCTION.

This section provides routine maintenance, removal, repair, replacement, and alignment procedures for Radio Receiving Set AN/GRR-17.

Note

The Naval Electronics Systems Command no longer requires the submission of failure reports for all equipments. Failure reports and performance and operational reports are to be accomplished for designated equipments (refer to Electronics Installation and Maintenance Book, NAVSHIPS 0967-000-0000) only to the extent required by existing directives. All failures shall be reported for those equipments requiring the use of failure reports.

5-2. PREVENTIVE MAINTENANCE.

This paragraph contains complete and comprehensive information, tables, and procedures required for effective preventive maintenance of Radio Receiving Set AN/GRR-17. Properly executed, the procedures in this paragraph will: (a) indicate optimum equipment performance, (b) reveal areas of deteriorated performance, and (c) extend operational equipment life.

a. MAINTENANCE STANDARDS.

(1) TEST EQUIPMENT AND SPECIAL TOOLS. - The test equipment required for preventive maintenance procedures is listed in table 5-1. Equivalent test equipment may be used if available.

(2) SPECIAL PROCEDURES.

(a) To energize Radio Receiving Set AN/GRR-17, follow the instructions contained in Section 3. Before taking Reference Standards Tests, allow 30 minutes for test equipment warm-up.

(b) Disconnect test equipment following completion of each reference standards procedure, preparatory to the next procedure.

(c) Preset all operating controls to the positions listed below. If a control setting is changed during a procedure, return it to the preset position

TABLE 5-1. TEST EQUIPMENT REQUIRED FOR PREVENTIVE MAINTENANCE

CATEGORY	RECOMMENDED	PARAMETERS
Frequency Counter	H-P 5245L with head H-P 5253B	Frequency Range: dc to 10 mc Stability: 5 parts in 10^8 per week
Audio Level Meter	H-P 403A	Direct Reading: -60 to +20 dbm (with 600-ohm shunt resistor)
Shunt Resistor	H-P 11033A	600 ohms
RF/VTVM	ME-286/U	20 cps to 100 mc; 0-1000 vac
Electronic Multimeter	AN/USM-116	DC Volts: 1 volt to 300 volts
RF Signal Generator	AN/URM-25D	Frequency Range: 1.9999 mc to 30.0001 mc Output Impedance: 50 ohms Output Voltage: 1 microvolt to 2 volts Modulation: 30% at 1000 cps
Oscilloscope	Tektronix Type 545A with Type C-A Preamplifier	DC to 24 mc; dual trace; dual time base

when the procedure is completed. The abbreviation (Adj) indicates that the control is to be adjusted as required by the procedural step or is not relevant to the procedure.

POWER switch: AC or DC (depending on power source)

RF GAIN control: NORMAL

MODE switch: (Adj)

BANDWIDTH switch: (Adj)

FREQ VERNIER control: FIXED

NOISE BLANKING control: Off

BFO control: FIXED

NOTCH WIDTH switch: OFF

METER FUNCTION switch: (Adj)

SPEAKER LEVEL control: (Adj)

PHONE LEVEL control: (Adj)

BAND MC switch: OFF

TELETYPE MODE: EXT BAT

(d) If difficulty is encountered in ascertaining the frequency of the rf input or af output, connect a frequency counter across the point in question.

(3) REFERENCE STANDARDS PROCEDURES. - The reference standards tests (see table 5-2) are subdivided into functional groups to facilitate accomplishment of equipment check-out. The reference standards test indications are to be established and recorded in the "Reference Standard" column of table 5-3 upon completion of installation, and these recorded values should be altered only when a major overhaul or field change necessitates such revision.

Note

The tolerance in the "Reference Standard" column of table 5-3 indicates the maximum and minimum limits of a test within which satisfactory operation can be expected for units of the same model. The tolerances are not to be construed as absolute limits since they are not necessarily developed from a complete evaluation. However, if any tolerance appears unreasonable when compared with the result of the test, the accomplishment of the test must be certified as correct by an electronics engineer.

(4) PREVENTIVE MAINTENANCE PROCEDURES. - The recommended periodic maintenance schedule (table 5-4) includes those checks which are indicative of equipment performance levels (e.g., sensitivity, selectivity, etc.) and the required cleaning and lubricating procedures. The schedule briefly describes the steps to be performed, the detailed procedures of which can be found by referring to the PM STEP column. Following completion of the preventive maintenance procedure, the equipment should be in proper operating condition. Differences from normal indications should receive corrective action.

TABLE 5-2. REFERENCE STANDARDS TESTS

SECTION	STEP	ACTION REQUIRED
A Crystal Oscillator	A1	Check frequency standard accuracy.
B Receiver (Over-All)	B1	Observe performance of equipment.
	B2	Check sensitivity at 2.0000 mc.
	B3	Check sensitivity at 16.0000 mc.
	B4	Check sensitivity at 29.9999 mc.
	B5	Check bandwidth at 6 db points using selectivity of 8 kc.
	B6	Check bandwidth at 6 db points using selectivity of 1 kc.
	B7	Check bandwidth at 6 db points using selectivity of 350 cps.
	B8	Check notch width (BROAD setting).
	B9	Check notch width (SHARP setting).
	B10	Check maximum audio output.
	B11	Check agc characteristic.

TABLE 5-3. PREVENTIVE MAINTENANCE PROCEDURES

STEP NO.	ACTION REQUIRED	READ INDICATION ON	REFERENCE STANDARD
A1	Check frequency standard accuracy	Frequency Counter	3 mc \pm 1 cps
	PROCEDURE: Connect frequency counter to test point A1A3A2A2J1 (TP). Observe reading on frequency counter.		
B1	Observe performance of equipment.		
(a)	Perform preliminary adjustment of control.		
	PROCEDURE: Place POWER switch in AC or DC position (depending on primary power source). Set FREQ VERNIER to FIXED for incremental tuning or VAR for fine tuning. Connect receiving antenna to 50 Ω ANT connector. Set SPEAKER LEVEL and PHONE LEVEL controls to near maximum (clockwise). (Use RF GAIN control to adjust output level.)		
(b)	Tune receiver.		
	PROCEDURE: Set MEGACYCLES dials to desired frequency. Adjust FREQ VERNIER control if in VAR position.		
(c)	Check AM reception.		
	PROCEDURE: Place MODE switch in AM position. Place BANDWIDTH switch in 8 KC position. Tune receiver to AM station transmitting voice signals. Check quality of AM reception.		
(d)	Check CW reception.		
	PROCEDURE: Place MODE switch in CW position. Place BFO switch large (outer) knob in VAR position and BANDWIDTH switch in 1 KC position. Tune receiver to CW transmitting station and adjust BFO inner knob for desired beat note. Check quality of CW reception.		
(e)	Check SSB reception.		
	PROCEDURE: Place MODE switch in SSB position. Place BANDWIDTH switch in USB or LSB position depending on signal characteristics. Tune receiver to single-sideband station and check quality of SSB reception.		
(f)	Check FSK reception.		
	PROCEDURE: Connect a teletype unit to the TELETYPE terminals on the receiver panel. If Teletypewriter Set AN/TGC-14A(V) or		

TABLE 5-3. PREVENTIVE MAINTENANCE PROCEDURES (Cont)

STEP NO.	ACTION REQUIRED	READ INDICATION ON	REFERENCE STANDARD
	similar equipment which supplies its own loop potential is used, turn the TELETYPE MODE switch to EXT BAT. If a teletype unit which does not supply its own loop potential is used, turn the TELETYPE MODE switch to INT BAT. Select a known broadcast station employing two-tone (1575 and 2425-cps) fsk transmissions. Place MODE switch in FSK position and BANDWIDTH switch in either LSB or USB position, depending on signal characteristics. Energize teletype-writer equipment as instructed in applicable manual. Observe teletypewriter for quality of received intelligence.		
B2	Check sensitivity at 2.0000 mc.	Audio level meter	<u> </u> dbm 0 dbm or less
	PROCEDURE: Connect signal generator to 50Ω ANT connector; plug audio level meter (terminated in 600 ohms) into PHONES jack. Adjust audio level meter to read dbm (1 mw in 600 ohms) in the range of 0 to +10 dbm. Tune receiver to 2.0000 mc. Place MODE switch in CW position and BANDWIDTH switch in USB position. Set SPEAKER LEVEL control to the off (fully counterclockwise) position. Adjust signal generator to 2.0010 mc and set output to approximately 5 microvolts. Adjust PHONE LEVEL control until audio level meter reads approximately mid-scale. Adjust signal generator slightly to peak meter indication. (It may be necessary to reduce signal generator output to avoid overdriving meter.) Set signal generator output to 1.5 microvolt. Adjust PHONE LEVEL control for a reading of 10 dbm on the audio level meter. Reduce signal generator output to zero. Read audio level meter.		
B3	Check sensitivity at 16.0000 mc.	Audio level meter	<u> </u> dbm 0 dbm or less
	PROCEDURE: Repeat step B2 except tune receiver to 16.0000 mc and signal generator to 16.0010 mc.		
B4	Check sensitivity at 29.9999 mc.	Audio level meter	<u> </u> dbm 0 dbm or less
	PROCEDURE: Repeat step B2 except tune receiver to 29.9999 mc and signal generator to 30.0009 mc.		
B5	Check bandwidth at 6 db points using selectivity of 8 kc.	Signal Generator	<u> </u> kc (6.4 to 9.6 kc)
	PROCEDURE: Connect signal generator to 50Ω ANT connector; plug an RF vtvm (terminated in 50 ohms) into test point A1A2A6A1J3. Remove detector/af amplifier module A1A2A7. Place MODE switch in CW position and BANDWIDTH switch in 8 KC position. Tune receiver to 2.5000 mc. Adjust the signal generator to 2.5000 mc and set		

TABLE 5-3. PREVENTIVE MAINTENANCE PROCEDURES (Cont)

STEP NO.	ACTION REQUIRED	READ INDICATION ON	REFERENCE STANDARD
B5 (Cont)	output to 10 microvolts. Adjust signal generator frequency slightly to peak the reading on the vtm. Record the reading on the vtm. Raise the signal generator output to 20 microvolts (6 db increase). Carefully tune signal generator frequency above 2.5000 mc until vtm again indicates the same reading previously recorded. Note the generator frequency. Carefully tune generator frequency below 2.5000 mc until vtm again indicates the same reading recorded above. Note the generator frequency. Record the difference between the two frequencies as the bandwidth at 6 db points.		
B6	Check bandwidth at 6 db points using selectivity of 1 kc.	Signal Generator	kc (0.8 to 1.2 kc)
	PROCEDURE: Repeat step B5 except place BANDWIDTH switch in 1 KC position.		
B7	Check bandwidth at 6 db points using selectivity of 350 cps.	Signal Generator	kc (300 to 400 cps)
	PROCEDURE: Repeat step B5 except place BANDWIDTH switch in 350 CPS position.		
B8	Check notch width (BROAD setting).	Signal Generator	kc (1.5 kc or less)
	PROCEDURE: Tune receiver to 2.5000 mc. Connect signal generator to 50Ω ANT connector; plug an rf vtm (terminated in 50 ohms) into test point A1A2A6A1J3. Remove detector/af amplifier module A1A2A7. Place MODE switch in CW position and BANDWIDTH switch in 8 KC position. Tune signal generator to 2.5000 mc and set output to 10 microvolts. Place BANDWIDTH switch in 350 CPS position. Tune generator slightly for peak indication on rf vtm. Return BANDWIDTH switch to 8 KC position and place NOTCH WIDTH control in BROAD position. Adjust NOTCH POSITION control for peak indication on rf vtm. Note the reading. Readjust NOTCH POSITION control for minimum indication on rf vtm. Increase signal generator output to 20 microvolts. Carefully adjust signal generator frequency below 2.5000 mc until rf vtm indication noted above is reached. Note generator frequency. Adjust signal generator frequency above 2.5000 mc until rf vtm indication is again reached. Note generator frequency. Record the difference between the two frequencies as the notch width at 6 db points.		
B9	Check notch width (SHARP setting).	Signal Generator	cps (200 cps or less)
	PROCEDURE: Repeat step B8 except place NOTCH WIDTH control in SHARP position rather than BROAD position.		

TABLE 5-3. PREVENTIVE MAINTENANCE PROCEDURES (Cont)

STEP NO.	ACTION REQUIRED	READ INDICATION ON	REFERENCE STANDARD
B10	Check maximum audio output.	Audio level meter	dbm (11 dbm min)
	PROCEDURE: Connect signal generator to 50Ω ANT connector; plug audio level meter (terminated in 600 ohms) into PHONES jack. Adjust audio level meter to read dbm (1 mw in 600 ohms) in the range of 10-12 dbm. Tune receiver to 16.0000 mc. Place MODE switch in AM position and BANDWIDTH switch in 8 KC position. Adjust signal generator for a 16.0000 mc signal, modulated 30% at 1000 cps at an output level of 1000 microvolts. Adjust PHONE LEVEL control for a reading of +5 dbm on audio level meter. Adjust signal generator frequency slightly for maximum indication on audio level meter. Readjust PHONE LEVEL control for a reading of +11 dbm on meter. This corresponds with an audio output of 15 milliwatts.		
B11	Check agc characteristic.	Audio level	a. dbm (+3 dbm max) b. dbm (+3 dbm max)
	PROCEDURE: Connect signal generator to 50Ω ANT connector; plug audio level meter (terminated in 600 ohms) into PHONES jack. Adjust audio level meter to read 0 dbm (1 mw in 600 ohms). Tune receiver to 16.0000 mc. Place MODE switch in SSB position and BANDWIDTH switch in USB position. Adjust signal generator to 16.0010 mc and set output to 8 microvolts, unmodulated. Adjust PHONE LEVEL control for a convenient indication on audio level meter. Adjust signal generator frequency slightly to peak meter reading. Readjust PHONE LEVEL control for a reading of 0 dbm on audio level meter. Increase generator output to 40 microvolts. Note meter reading (reference standard a). Readjust PHONE LEVEL control for a reading of 0 dbm on audio level meter. Increase generator output to 2 volts. Note meter reading (reference standard b).		
B12	Perform mechanical inspection.		
	PROCEDURE: Operate all controls, observing mechanical action. If control sticks or binds DO NOT FORCE MOVEMENT; find cause (bent shaft, loose mounting, etc.) and correct it. Observe action of MEGACYCLES dials.		
B13	Perform electrical inspection.		
	PROCEDURE: Inspect all electrical components, wiring and cabling. Look and feel for loose connections, kinks, strains, and damaged insulation; correct defects or report them to a qualified technician. Look for evidence of overheating; take corrective action if any is found. Clean chassis with a vacuum cleaner.		

TABLE 5-4. RECOMMENDED PERIODIC MAINTENANCE SCHEDULE

MONTHLY		TIME REQ'D: 2 hours
STEP NO.	ACTION REQUIRED	PM STEP
1	Check frequency standard accuracy	A1
2	Observe performance of equipment	B1
3	Perform mechanical inspection	B12
4	Perform electrical inspection	B13
QUARTERLY		TIME REQ'D: 4 hours
1	Check sensitivity at 2.0000 mc	B2
2	Check sensitivity at 16.0000 mc	B3
3	Check sensitivity at 29.9999 mc	B4
4	Check bandwidth at 6 db points using selectivity of 8 kc	B5
5	Check bandwidth at 6 db points using selectivity of 1 kc	B6
6	Check bandwidth at 6 db points using selectivity of 350 cps	B7
7	Check notch width (BROAD setting)	B8
8	Check notch width (SHARP setting)	B9
9	Check maximum audio output	B10
10	Check agc characteristic	B11

b. TUNING AND ADJUSTMENT.

(1) INTRODUCTION. - This paragraph includes instructions for performance of all tuning, alignment, and other adjustment procedures required to insure optimum receiver performance. Use a card extender for access to unexposed card terminals or test points. Receiver components should be aligned in the following order:

- (a) Frequency Standard (A1A1A1).
- (b) Mixer/Multiplier (A1A3A2).
- (c) Frequency Synthesizer (A1A3A1).
- (d) HFO Phase Lock Loop (A1A2A2A1).
- (e) First I-F Module (A1A2A3).
- (f) Noise Blanker Module (A1A2A4).
- (g) Notch Filter (A1A1A4).
- (h) Second I-F/AGC Module (A1A2A6).
- (i) Beat Frequency Oscillator (A1A1A2).
- (j) Audio Detector/Amplifier (A1A2A7A1).
- (k) FSK Converter (A1A2A7A2).

(2) FREQUENCY STANDARD (A1A1A1).

(a) TEST EQUIPMENT. - To align the 3 mc frequency standard, the following test equipment or its equivalent is required:

1. Frequency Counter, H-P 5245L.

(b) INSTRUCTIONS. - To align the frequency standard, perform the following steps:

Note

To gain access to 3 mc output of frequency standard (A1A1A1), use test point A1A3A2A2J1(TP) on mixer/multiplier module.

1. Connect 3 mc output to signal input of frequency counter.
2. Adjust frequency adjustment screw on receiver frequency standard (A1A1A1) for frequency of 3 mc ± 0.3 cps, as measured by frequency counter.
3. Remove power from receiver and electronic frequency counter.

4. Disconnect electronic frequency counter from receiver.

(3) MIXER/MULTIPLIER (A1A3A2).

(a) TEST EQUIPMENT. - To align the mixer/multiplier, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.
2. Frequency Counter, H-P 5245L with head H-P 5253B.
3. Oscilloscope, Tektronix Type 545A with Plug-In Unit
4. Electronic RF Voltmeter, ME-286/U.

Type C-A.

(b) INSTRUCTIONS. - To align the mixer/multiplier, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of the terminal leads (steps 11, 14, 17, and 23).

1. Connect signal generator to input of frequency counter.
2. Adjust generator for unmodulated output frequency of 30 mc, as measured by frequency counter.
3. Disconnect external lead to 30-mc input (terminal (9) of frequency/multiplier (X10), card A2).
4. Connect generator to terminal 9 of card A2.
5. Adjust signal generator for output level of 20 mv.
6. Connect oscilloscope to test point J2 on card A2.
7. Set FREQ VERNIER ± 150 CPS control on receiver panel to

FIXED position.

Note

During performance of step 8 of this procedure, adjust frequency setting of rf signal generator as necessary to obtain a beat-note presentation on oscilloscope.

8. Adjust transformer T4 on frequency/multiplier (X10) card A2 for maximum amplitude as displayed by oscilloscope. Nominal peak-to-peak amplitude is 7 volts.
9. Disconnect signal generator from receiver.

10. Connect rf voltmeter to terminal 9 of card A2.
11. Adjust capacitor C23 on card A2 for minimum voltmeter reading.
12. Repeat steps 4 through 11 to verify adjustments.
13. Disconnect oscilloscope and electronic rf voltmeter.
14. Reconnect external lead to 30 mc input (terminal (9) of frequency/multiplier (X10) card A2).
15. Connect generator to frequency counter.
16. Adjust generator for unmodulated output frequency of 3 mc, as measured by electronic frequency counter.
17. Disconnect external lead to 3 mc input (terminal (1) of frequency/multiplier (X10) card A2).
18. Connect generator to 3 mc input test point (J1), card A2.
19. Adjust generator for unmodulated output level of 100 mv.
20. Connect electronic frequency counter to 30 mc output (terminal (18) of frequency/multiplier (X4), card A1).
21. Adjust capacitor C12 on card A1 for a 30 mc reading on frequency counter.
22. Adjust generator frequency and capacitor C12 so that phase-lock region is symmetrical at 3 mc and 30 mc. (Nominal phase-lock bandwidth is 30 kc (± 15 kc) at 3 mc and 300 kc (± 150 kc) at 30 mc. Phase lock is indicated by stable reading on electronic frequency counter.)
23. Reconnect external lead to 3 mc input (terminal (1) of frequency/multiplier (X10) card A2).
24. Connect rf voltmeter to 117 mc output (terminal (7) of card A1).
25. Adjust transformers T1, T2, T6, and T7 on card A1 for maximum reading on voltmeter. Nominal value at 117 mc is 1 volt rms.
26. Connect frequency counter to 117 mc output terminal of card A1. Check that frequency is 117 mc.

Note

Resonance "peak" may be very broad. Adjust transformers for center of "peak".

(4) FREQUENCY SYNTHESIZER (A1A3A1).

(a) TEST EQUIPMENT. - To align the frequency synthesizer, the following test equipment or its equivalent is required:

1. Electronic DC Voltmeter, AN/USM-116.

(b) INSTRUCTIONS. - To align the frequency synthesizer, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Connect dc voltmeter to junction of C14 and R22 on rf #2 card A5.
2. Tune receiver to 2.0000 mc.
3. Adjust capacitor C15 on card A5 for reading of +6.5 to +7.0 volts dc (Serial Numbers A5 through A54 inclusive) or +5.0 volts dc (all Serial Numbers higher than A54).
4. Connect dc voltmeter to test point J1 on rf #3 card A2.
5. Adjust inductor L3 on card A2 for reading of +4.5 volts dc.
6. Connect dc voltmeter to test point J1 on rf #1 (A) card A1.
7. Adjust inductor L1 on card A1 for reading of +10.0 volts dc.
8. Tune receiver to 12.0000 mc.
9. Adjust inductor L2 on card A1 for reading of +10.0 volts dc.
10. Tune receiver to 22.0000 mc.
11. Adjust inductor L3 on card A1 for reading of +10.0 volts dc.
12. Repeat steps 7 through 11 as necessary to verify adjustments.

(5) VHF OSCILLATOR PHASE-LOCK LOOP (A1A2A2A1).

(a) TEST EQUIPMENT. - To align the vhf oscillator phase-lock loop, the following test equipments or their equivalent are required:

1. Oscilloscope, Tektronix Type 545A with Plug-In Unit Type C-A.
2. Signal Generator URM-26D.
3. Electronic Frequency Counter, H-P 5245L with head H-P 5253B.

(b) INSTRUCTIONS. - To align the vhf oscillator phase-lock loop, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Connect oscilloscope to terminal 7 of vhf oscillator phase-lock loop card A1. Remove rf #1(A) card A1.
2. Adjust potentiometer R38 on card A1 for sweep period of approximately 1/2 second, as measured by oscilloscope.
3. Adjust potentiometer R34 on card A1 so that "peaks" and "valleys" of waveform are identical in size and shape.
4. Adjust potentiometer R17 on card A1 so that dc level at tops of "peaks" is approximately 110 volts.
5. Disconnect synthesizer output lead from terminal 1 of vhf oscillator phase-lock loop card A1 and connect signal generator in its place.
6. Tune generator to 75.0 mc and adjust output to 100 mv.
7. Adjust potentiometer R41 on card A1 so that the vhf oscillator "locks" at 75.0 mc.

Note

The intent of this alignment procedure is to assure that the vhf oscillator locks at 75.0 mc and above, but does not lock below 75.0 mc.

8. Replace card removed in step 1 and lead removed in step 5.

(6) FIRST I-F MODULE (A1A2A3).

(a) TEST EQUIPMENT. - To align the first i-f module, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.
2. Frequency Counter, H-P 5245L.

(b) INSTRUCTIONS. - To align the first i-f module, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to CW.
2. Set BANDWIDTH switch on front panel to 8 KC.
3. Set BFO switch on front panel to FIXED.
4. Set METER FUNCTION switch on front panel to PHONE

LEVEL.

5. Set PHONE LEVEL control on front panel to obtain an audio output of approximately +2 dbm on signal level meter.

6. Tune receiver to any convenient frequency from 2.0000 mc to 29.9999 mc.

7. Connect rf signal generator to input of frequency counter.

8. Adjust generator for unmodulated output frequency selected during step 6. Use frequency counter to measure frequency.

9. Connect generator to 50 Ω ANT connector on front panel.

10. Adjust generator for an output of approximately +11 dbm on the signal level meter.

Note

Reading on signal level meter may increase during performance of this procedure. Reduce output level from generator as necessary to maintain the +11 dbm meter reading.

11. Adjust inductors L2, L6, L9, and L13 on 112 mc amplifier card A1 for maximum reading on signal level meter.

12. Set RF GAIN control to approximate center of its adjustment range.

Note

Increase output level from generator to facilitate performance of step 13.

13. Adjust capacitor C8 on 112 mc amplifier card A1 for minimum reading on signal level meter.

14. Readjust RF GAIN control generator level as necessary to maintain an indication on signal level meter.

15. Adjust transformers T2 and T4 on 5 mc reserve-gain-amplifier card A2 for maximum reading on signal level meter.

Note

Final adjustment of 5 mc reserve-gain amplifier (A2) is performed during alignment of second i-f/agc module (A1A2A6). (Refer to paragraph 5-2b(8)(b).)

16. Adjust T1 and T2 on 117 mc buffer amplifier A3 for maximum reading on signal level meter.

Note

Resonance "peak" obtained during performance of step 16 may be broad. Adjust tuning control to approximate center of "peak".

(7) NOISE BLANKER MODULE (A1A2A4).

(a) TEST EQUIPMENT. - To align the noise blanker module, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.
2. Frequency Counter, H-P 5245L.

(b) INSTRUCTIONS. - To align the noise blanker module, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to CW.
2. Set BANDWIDTH switch on front panel to 8 KC.
3. Set BFO switch on front panel to FIXED.
4. Set METER FUNCTION switch on front panel to PHONE LEVEL.
5. Set PHONE LEVEL control on front panel to center of its adjustment.
6. Tune receiver to any convenient frequency from 2.0000 mc to 29.9999 mc.
7. Connect rf signal generator to signal input of frequency counter.
8. Adjust generator for unmodulated output frequency selected during step 6. Use frequency counter to measure frequency.

9. Connect generator to 50Ω ANT connector on front panel.
10. Adjust generator for an indication on signal level meter.

Note

Signal level meter reading may increase during following steps. Reduce output from generator as necessary to maintain usable meter reading.

11. Set NOISE BLANKING control on front panel to OFF.

12. Adjust transformer T2 on detector/gated-amplifier card A2 for maximum reading on meter.

(8) SECOND I-F/AGC MODULE (A1A2A6).

(a) TEST EQUIPMENT. - To align the second i-f/agc module, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.
2. Frequency Counter, H-P 5245L.
3. Electronic RF Voltmeter, ME-286/U.

(b) INSTRUCTIONS. - To align the second i-f/agc module, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to CW.
2. Set BANDWIDTH switch on front panel to 8 KC.
3. Set BFO switch on front panel to FIXED.
4. Set METER FUNCTION switch on front panel to PHONE LEVEL.
5. Set PHONE LEVEL control on front panel center of its adjustment.
6. Tune receiver to any convenient frequency from 2.0000 mc to 29.9999 mc.
7. Connect rf signal generator to frequency counter.
8. Adjust generator for unmodulated frequency selected during step 6. Use frequency counter to measure frequency.

9. Connect generator to 50Ω ANT connector on front panel.
10. Adjust generator for an indication on signal level meter.

Note

Signal level meter reading may increase during following steps. Reduce output from generator as necessary to maintain usable meter reading.

11. Adjust transformers T1, T2, and T4 on 5 mc i-f amplifier card A1 for maximum reading on meter.
12. Set MODE switch on front panel to SSB.
13. Set METER FUNCTION switch on front panel to RF IN.
14. Adjust transformers T1 and T2 on agc-amplifier card A2 for maximum reading on meter.
15. Remove detector/audio-frequency amplifier module (A1A2A7) from receiver.
16. Connect rf voltmeter (terminated in 50 ohms) to test point A1J3.
17. Adjust generator for unmodulated output of 100 mv.
18. Adjust AGC LEVEL control (R1) on agc amplifier card A2 for reading of 20 mv on voltmeter.
19. Adjust generator for unmodulated output of 8 uv (open-circuit).
20. Adjust RESERVE GAIN control (R17) on 5 mc reserve-gain-amplifier card A2 for very small reading on signal level meter.
21. Replace detector/audio-amplifier module (A1A2A7).

(9) NOTCH FILTER (A1A1A4).

(a) TEST EQUIPMENT. - To align the notch filter, the following test equipments or their equivalents are required:

1. Electronic Frequency Counter, H-P 5245L.
2. Electronic RF Voltmeter, ME-286/U.
3. RF Signal Generator, AN/URM-25D.

(b) INSTRUCTIONS. - To align the notch filter, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to SSB.
2. Set BANDWIDTH switch on front panel to 8 KC.
3. Set METER FUNCTION switch on front panel to RF IN.
4. Set NOTCH POSITION control on front panel to center of its adjustment.
5. Connect frequency counter to collector of Q4 on 1.5 mc oscillator-amplifier card A1.
6. Adjust transformer T1 on card A1 for reading of 1.5 mc (± 100 cps) on frequency counter.
7. Connect voltmeter to base of Q4 on card A1.
8. Adjust transformer T2 on card A1 for maximum reading on voltmeter.
9. Set NOTCH WIDTH control on front panel to OFF.
10. Tune receiver to any convenient frequency from 2.0000 mc to 29.9999 mc.
11. Connect output from rf signal generator to frequency counter.
12. Adjust generator for unmodulated output frequency selected during performance of step 10. Use frequency counter to measure frequency.
13. Connect generator to 50 Ω ANT connector on front panel.
14. Adjust generator for an indication on signal level meter.

Note

Signal level meter reading may increase during step 15. Reduce output of generator as necessary to maintain usable meter reading.

15. Adjust transformers T2, T3, and T4 on 5.0/3.5 mc mixer-amplifier card A2 for maximum reading on meter.

(10) BEAT FREQUENCY OSCILLATOR (A1A1A2).

(a) TEST EQUIPMENT. - To align the beat frequency oscillator, the following test equipments or their equivalents are required:

1. Electronic Frequency Counter, H-P 5245L.

2. Electronic RF Voltmeter, ME-286/U.

(b) INSTRUCTIONS. - To align the beat frequency oscillator, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to CW.
2. Set BFO ± 3 KC switch on front panel to VAR.
3. Set BFO ± 3 KC control on front panel to center of its range.
4. Connect frequency counter to 5 mc output terminal (E5).
5. Adjust inductor L2 on oscillator card A2 for reading of 5 mc (± 100 cps) on frequency counter.
6. Connect rf voltmeter to 5 mc output terminal (E5).
7. Adjust transformer T1 on amplifier card A1 for maximum reading on voltmeter.

(11) AUDIO DETECTOR/AMPLIFIER (A1A2A7A1).

(a) TEST EQUIPMENT. - To align the audio detector/amplifier, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.
2. Electronic Frequency Counter, H-P 5245L.

(b) INSTRUCTIONS. - To align the audio detector/amplifier, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card and extender.

1. Set MODE switch on front panel to AM.
2. Set BANDWIDTH switch on front panel to 8 KC.
3. Set METER FUNCTION switch on front panel to PHONE LEVEL.
4. Tune receiver to any convenient frequency from 2.0000 mc to 29.9999 mc.
5. Connect output of rf signal generator to frequency counter.

6. Adjust generator for unmodulated output frequency selected during step 4. Use frequency counter to measure frequency.

7. Connect generator to 50 Ω ANT connector on front panel.

8. Modulate generator output 30% at 1000 cps.

9. Adjust generator for indication on signal level meter.

Note

Signal level meter reading may increase during step 10. Reduce output from generator as necessary to maintain usable meter reading.

10. Adjust transformer T1 on audio detector/amplifier card A1 for maximum reading on signal level meter.

(12) FSK CONVERTER (A1A2A7A2).

(a) TEST EQUIPMENT. - To align the fsk converter, the following test equipments or their equivalents are required:

1. RF Signal Generator, AN/URM-25D.

2. Electronic Frequency Counter, H-P 5245L.

3. Electronic RF Voltmeter, ME-286/U.

4. Oscilloscope, Tektronix Type 545A with Head Type 86 C-A.

(b) INSTRUCTIONS. - To align the fsk converter, perform the following steps:

CAUTION

De-energize receiver prior to removal or replacement of card or extender.

1. Connect output of rf signal generator to frequency counter.

2. Adjust generator for unmodulated output of 5.0000 mc (± 10 cps), measured by frequency counter.

3. Adjust generator level for 2 mv output.

4. Remove second i-f amplifier module (A1A2A6).

5. Connect generator to socket terminal A1A2XA6-D.

6. Set MODE switch on front panel to FSK.

7. Connect rf voltmeter to collector Q5 on fsk-converter card

A2.

8. Adjust inductors L2, L4, and L5 and capacitors C23 and C24 on card A2 for maximum voltmeter reading.
9. Connect rf voltmeter to collector of Q6 on card A2.
10. Adjust inductor L8 and capacitor C27 for maximum reading on voltmeter.
11. Connect rf voltmeter to collector of Q7 on card A2.
12. Adjust inductor L9 and capacitor C35 for maximum reading on voltmeter.
13. Adjust generator for unmodulated output of 2 mv at 5.002 mc, ± 10 cps, as measured by frequency counter.
14. Connect rf voltmeter to collector of Q6 on card A2.
15. Adjust C27 for maximum reading on voltmeter.
16. Adjust generator to 5.100 mc as measured by frequency counter.
17. Adjust C28 for minimum reading on voltmeter.
18. Repeat steps (10) thru (13) until no further improvement can be obtained.
19. Adjust generator for unmodulated output of 4.998 mc, ± 10 cps, as measured by frequency counter.
20. Adjust C30 for maximum reading on voltmeter.
21. Adjust generator for 4.900 mc as measured on frequency counter.
22. Adjust C31 for minimum reading on voltmeter.
23. Repeat steps (16) thru (19) until no further improvement can be obtained.
24. Connect oscilloscope to collector of Q8 on card A2.
25. Adjust capacitor C23 on card A2 for oscilloscope waveform, bracketed above and below by horizontal traces of approximately equal intensity.
26. Sketch the oscilloscope waveform for future reference.
27. Connect generator to frequency counter.
28. Adjust generator for unmodulated output of 5.0020 mc (± 10 cps), measured by frequency counter.
29. Adjust generator for output level of 2 mv.

30. Connect generator to socket terminal A1A2XA6-D.

31. Adjust capacitor C24 on card A2 for oscilloscope presentation identical to that of step (26).

32. Repeat step (25) and steps (26) through (32) to optimize adjustments. The required oscilloscope presentation must be obtained for frequency settings of both 4.9980 mc (± 25 cps) and 5.0020 mc (± 25 cps).

33. Replace second i-f amplifier module (A1A2A6) in receiver.

5-3. REPAIR.

a. GENERAL. - Radio Receiver R-1490/GRR-17 is designed and constructed to require a minimum repair effort. The entire receiver is composed of readily accessible and removable subassemblies and modules. Access to most parts is obtained by removing module covers and either extracting plug-in printed circuit cards or unscrewing and unsoldering subassemblies. Paragraph 5-4 contains complete instructions for the removal and replacement of modules and subassemblies within the receiver.

WARNING

Remove primary power from equipment before attempting module removal, replacement, or any repair technique.

b. MODULE REPAIR TECHNIQUES. - Module repair, following the identification of a faulty part or parts, usually consists of removing and replacing the card or part at fault. Good repair techniques, performed by a qualified maintenance technician, are necessary to return the receiver to operation quickly. Some modules will require disassembly to expose parts which must be repaired. Refer to the applicable instructions for module disassembly in this section of the manual.

(1) PRINTED CIRCUIT REPAIR TECHNIQUES. - Radio Receiver R-1490/GRR-17 modules contain printed circuit boards. When removing or replacing parts, observe all precautions applicable for soldering small parts on printed circuit boards. Small parts (resistors, capacitors, diodes, etc.) may be damaged by excessive heat during soldering. Use a heat sink such as long-nose pliers or metal clips between the heat source and the part to be soldered. Solder as rapidly as possible and use as low a wattage soldering iron as possible.

c. USE OF PARTS LOCATION AND SCHEMATIC DIAGRAMS. - When repairing any part of a subassembly of the receiver, refer to the applicable parts location diagram and schematic. The schematics for the receiver are given at the end of this section. The parts location diagrams (figures 5-1 through 5-48) identify and locate all replaceable electrical parts.

5-4. REMOVAL AND REPLACEMENT.

a. GENERAL. - This paragraph contains instructions for the removal of modules and subassemblies from the receiver and their subsequent replacement. The procedures given below should be carefully followed to prevent damaging the equipment. In no case should any module be forced into place; most have multipin connectors which can be damaged if forced.

b. PROCEDURES.

(1) RADIO RECEIVER R-1490/GRR-17. (See figure 5-1.)

(a) DISASSEMBLY. - The receiver must be separated from its transit case and the dust cover removed before any module or subassembly can be removed for repair.

1. Remove the transit case by unscrewing the eight mounting bolts on the front panel of the receiver and the two bolts on the rear of the case.
2. Slide the receiver out of the transit case.
3. Remove the dust cover by loosening 18 captive screws which secure it to the receiver chassis.
4. Slide the dust cover off the receiver.
5. Obtain access to the rear of the hinged front panel assembly by taking out the six mounting screws and the four captive screws on the front panel face.
6. Pull the front panel assembly away from the front deck assembly and fold out at right angles to the rest of the receiver.
7. Obtain access to the hinged rear deck assembly by loosening the four captive screws on each corner of the rear deck.
8. Pull the rear deck assembly away from the front deck assembly and fold out at right angles to the rest of the receiver. Engage two slide fasteners to lock rear deck in position.

(b) REASSEMBLY.

1. Disengage two slide fasteners holding rear deck in position.
2. Fold the front and rear deck assemblies so that the four captive screws on the front deck line up with the holes on the rear deck.
3. Tighten the four captive screws on the rear deck assembly.

CAUTION

Before proceeding with step 4, make sure two switch shafts on front deck line up with their respective couplers on front panel.

4. Fold the front panel assembly and the front deck assembly so that the six mounting screws on the front panel assembly line up with the holes on the front deck assembly.
5. Tighten the six mounting screws and four captive screws on the front panel assembly.

6. Slide dust cover onto receiver and secure by tightening the 18 screws into the receiver chassis.

7. Slide the receiver into the transit case.

8. Replace and tighten the eight case mounting bolts on the front of the receiver, and the two bolts on the rear of the case.

(2) FREQUENCY STANDARD A1A1A1. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Disconnect the rf output cable from frequency standard.
3. Unsolder the ground and B+ leads from frequency standard.
4. Remove the four screws which secure frequency standard to the front panel assembly.

(b) REPLACEMENT.

1. Secure the four screws which hold frequency standard to the front panel assembly.
2. Solder the ground and B+ leads to frequency standard.
3. Connect the rf output cable to frequency standard.

(3) VFO A1A1A3. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Remove the two knobs from the FREQ VERNIER ± 150 CPS control on the front panel by loosening the two Allen set screws in each knob.
3. Remove the four front panel face screws from around the FREQ VERNIER ± 150 CPS control.
4. Unsolder the wires from the top of the vfo module. Note labels on unsoldered connections for proper reassembly.
5. Remove the vfo module from the front panel assembly.
6. Remove the 10 screws which secure the two halves of the vfo module cover. Remove the cover.

7. Remove the two printed circuit boards (A1 oscillator, A2 trimmer) from the module chassis by unsoldering the interconnection wires and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Place printed circuit boards A1 and A2 on module chassis.
2. Solder interconnection wires and install the mounting screws.
3. Place both halves of the module cover over the module chassis and secure together with 10 screws.
4. Position the module in place on rear of front panel assembly.
5. Solder connections to rear of the module.
6. Secure the module to the front panel with four screws through the panel face.
7. Install the two knobs on FREQ VERNIER ± 150 CPS shaft.

Note

Rotate shaft and sleeve fully clockwise. Index large knob at VAR, small knob at (+) mark. Tighten set screws.

(4) BFO A1A1A2. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Remove the two knobs from the BFO ± 3 KC control on the front panel by loosening the two Allen set screws in each knob.
3. Remove the four front panel face screws securing the bfo module.
4. Unsolder connections and pull the bfo module away from the front panel assembly.
5. Remove the bfo module cover by removing the eight screws which mount it to the bfo chassis.
6. Remove the two printed circuit boards (oscillator A2 and amplifier A1) from the module chassis by unsoldering the interconnection wires and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Place printed circuit boards A1 and A2 on the module chassis.
2. Solder the interconnection wires and install the mounting screws.
3. Place the module cover on the module chassis and secure with the eight mounting screws.
4. Position the module in place on rear of the front panel assembly.
5. Secure the module to the front panel with four screws through the panel face. Resolder connections.
6. Install the two knobs on the bfo shaft.

Note

Rotate shaft and sleeve fully clockwise. Index large knob at VAR, small knob at (+) mark. Tighten set screws.

(5) NOTCH FILTER A1A1A4. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Remove the six front panel face screws securing the notch filter module.
3. Unsolder connections and pull the module away from the front panel assembly.
4. Remove the nine screws which secure the two halves of the module cover and take off the module cover.
5. Remove the two printed circuit boards (amplifier-mixer A2 and oscillator-mixer A1) from the module chassis by unsoldering the interconnection wires and removing the mounting screws. Note label for proper reassembly.

(b) REPLACEMENT.

1. Place printed circuit boards A1 and A2 on the module chassis.
2. Solder the interconnection wires and install the mounting screws.
3. Place the two halves of the module cover on the module chassis and secure them with nine screws.

4. Position the module in place on rear of front panel assembly.

5. Secure the module to the front panel with six screws through the panel face. Resolder connections.

(6) FREQUENCY SELECTOR A1A1A5. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Set MEGACYCLES controls to 02.0000. Note position of the mc switch S8 on rear of front panel assembly with relation to the mc dial setting.

3. Remove the five knobs from the MEGACYCLES controls on the front panel by loosening the two set screws in each knob.

4. Remove the five front panel face screws securing the frequency selector assembly.

5. Remove the toothed plastic belt from its position on switch S8.

CAUTION

The positions of switch S8 (on the panel) and the mc dial (on the selector assembly) must not be changed. To do so will alter the receiver frequency calibration.

6. Unsolder all interconnection wires between frequency selector assembly and front panel assembly.

7. Remove the frequency selector assembly from the front panel section.

(b) REPLACEMENT.

1. Position the frequency selector assembly in place on the rear of the front panel assembly.

2. Solder all interconnections between frequency selector and front panel.

3. Place the toothed plastic belt in position on the panel switch S8.

4. Secure the frequency selector assembly to the front panel with five mounting screws through the panel face.

5. Install the five knobs on the MEGACYCLES controls.

(7) INPUT FILTER A1A2A1. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Loosen the four captive mounting screws which secure the input filter module to the front deck assembly.
3. Remove the input filter module from socket A2XA1 on the front deck assembly.
4. Loosen the two captive screws on the cover of the input filter module. Remove the cover.
5. Remove four screws on the small cover on side of input filter module. Remove the cover.
6. Remove the overload protection printed-circuit board by unsoldering interconnections. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Place the overload protection printed-circuit board in position in module chassis.
2. Solder the interconnections.
3. Secure cover over overload protection board with four screws.
4. Secure the module cover to the module by tightening the two captive screws on the cover.
5. Plug the module into socket A2XA1 of the front deck assembly. Make sure that the input filter selector switch (which protrudes through bottom of module) fits through access hole on front deck assembly and locating pin mates with shaft coupling.
6. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(8) FRONT END A1A2A2. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Loosen the four captive mounting screws which secure the front end module to the front deck assembly.
3. Remove the front end module from socket A2XA2 on the front deck assembly.

4. Loosen the two captive screws on the cover of the front end module. Remove the cover.

5. Remove phase-locked loop card A1 from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between card A1 and the module.

2. Install the card on the module with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A2XA2 of the front deck assembly.

5. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(9) FIRST I-F AMPLIFIER A1A2A3. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the four captive mounting screws which secure the first i-f module to the front deck assembly.

3. Remove the first i-f module from socket A2XA3 on the front deck assembly.

4. Loosen the two captive screws on the cover of the first i-f module. Remove the cover.

5. Remove the three printed circuit boards (112 mc i-f/mixer A1, second i-f/reserve gain amplifier A2, and 117 mc buffer amplifier A3) from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between cards A1, A2, and A3 and the module.

2. Install the cards on the module with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A2XA3 of the front deck assembly.

5. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(10) NOISE BLANKER A1A2A4. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the four captive mounting screws which secure the noise blanker module to the front deck assembly.

3. Remove the noise blanker module from socket A2XA4 on the front deck assembly.

4. Loosen the two captive screws on the cover of the noise blanker module. Remove the cover.

5. Remove the two cards (5 mc amplifier A1 and detector/gated amplifier A2) from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between cards A1 and A2 and the module.

2. Install the printed circuit boards on the module with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A2XA4 of the front deck assembly.

5. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(11) INTELLIGENCE FILTER A1A2A5. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the two captive mounting screws which secure the intelligence filter module to the front deck assembly.

3. Remove the intelligence filter module from socket A2XA5 on the front deck assembly.

4. Loosen the captive screw on the cover of the intelligence filter module. Remove the cover.

(b) REPLACEMENT.

1. Secure the module cover to the module by tightening the captive screw on the cover.

2. Plug the module into socket A2XA5 of the front deck assembly.

3. Secure the module to the front deck assembly by tightening the two captive mounting screws.

(12) SECOND I-F/AGC-AMPLIFIER A1A2A6. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the four captive mounting screws which secure the second i-f/agc module to the front deck assembly.

3. Remove the second i-f/agc module from socket A2XA6 on the front deck assembly.

4. Loosen the two captive screws on the cover of the second i-f/agc module. Remove the cover.

5. Remove the two cards (5 mc i-f amplifier A1 and agc amplifier A2) from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between cards A1, A2, and the module.

2. Install the printed circuit boards on the module with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A2XA6 of the front deck assembly.

5. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(13) DETECTOR/AF AMPLIFIER A1A2A7. (See figure 5-5.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the four captive mounting screws which secure the detector/af amplifier module to the front deck assembly.

3. Remove the detector/af amplifier module from socket A2XA7 on the front deck assembly.

4. Loosen the two captive screws on the cover of the detector/af amplifier module. Remove the cover.

5. Remove the two cards (detector/amplifier A1 and fsk converter A2) from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between cards A1, A2, and the module chassis.

2. Install the printed circuit boards on the module with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A2XA7 of the front deck assembly.

5. Secure the module to the front deck assembly by tightening the four captive mounting screws.

(14) FRONT DECK DECOUPLING BOARD A1A2A8. (See figure 5-4.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Unsolder the interconnections between the decoupling board and the front deck assembly. Label unsoldered connections for proper reassembly.

3. Remove the three mounting screws which secure the decoupling board to the front deck assembly.

(b) REPLACEMENT.

1. Secure the decoupling board to the front deck assembly with the three mounting screws.

2. Solder the interconnections between the decoupling board and the front deck assembly.

(15) SYNTHESIZER A1A3A1. (See figure 5-7.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Loosen the four captive mounting screws which secure the synthesizer module to the rear deck assembly.
3. Remove the synthesizer module from sockets A3XA1P1 and A3XA1P2 on the rear deck assembly.
4. Remove the thirteen screws and nut which secure the top cover to the synthesizer module. Remove the cover.
5. Use the card puller to remove cards A1 (rf #1(A)), A4 (rf #1(B)), A3 (digital #2), A2 (rf #3), A5 (rf #2), A6 (digital #3), and A7 (digital #1) from the module.

CAUTION

Card A1 (rf #1(A)) must be partially withdrawn from pocket to expose connector J2. Remove rf cable before completely removing card.

(b) REPLACEMENT.

1. Insert printed circuit cards A1 through A7 into their proper sockets. (Connect rf cable at J2 before inserting card A1A3A1A1.)
2. Place the top cover on the module. Secure the cover to the module with the thirteen mounting screws and nut.
3. Plug the module into sockets A3XA1P1 and A3XA1P2 of the rear deck assembly.
4. Secure the module to the rear deck assembly by tightening the four captive mounting screws.

(16) MIXER/MULTIPLIER A1A3A2. (See figure 5-7.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Loosen the four captive mounting screws which secure the mixer/multiplier module to the rear deck assembly.
3. Remove the mixer/multiplier module from socket A3XA2 of the rear deck assembly.
4. Loosen the two captive screws which secure the cover of the mixer/multiplier module. Remove the cover.

5. Remove the two cards (X4 multiplier A1 and X10 multiplier A2) from the module by unsoldering the interconnections and removing the mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Solder the interconnections between cards A1, A2, and the module chassis.

2. Install the cards in the module chassis with the mounting screws.

3. Secure the module cover to the module by tightening the two captive screws on the cover.

4. Plug the module into socket A3XA2 of the rear deck assembly.

5. Secure the module to the rear deck assembly by tightening the four captive mounting screws.

(17) POWER SUPPLY A1A3PS1. (See figure 5-7.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Loosen the five captive mounting screws which secure the power supply module to the rear deck assembly.

3. Remove the power supply module from socket A3XPS1 of the rear deck assembly.

4. Loosen the two captive screws which secure the cover of the power supply module. Remove the cover.

5. Remove the regulator section (A3) which contains printed circuit boards A1 (+5 volt and +18 volt regulator), A2 (+15 volt regulator), and A3 (fuses and test points) by removing the four screws which attach the section to the module chassis and the screw on the bracket which is affixed to printed circuit board A1.

6. Separate the printed circuit boards by unsoldering interconnection wires and removing mounting screws. Label unsoldered connections for proper reassembly.

(b) REPLACEMENT.

1. Solder the interconnecting wires between the printed circuit boards.

2. Assemble the printed circuit boards together with the mounting screws.

3. Install the assembled printed circuit board section A3 in the module chassis.

4. Secure the module cover to the module by tightening the two captive screws on the cover.

5. Plug the module into socket A2XPS1 of the rear deck assembly.

6. Secure the module to the rear deck assembly by tightening the five captive mounting screws.

(18) REAR DECK DECOUPLING BOARD A1A3A3. (See figure 5-6.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Unsolder the interconnections between the decoupling board and the rear deck assembly. Label unsoldered connections for proper reassembly.

3. Remove the six mounting screws which secure the decoupling board to the rear deck assembly.

(b) REPLACEMENT.

1. Secure the decoupling board to the rear deck assembly with the six mounting screws.

2. Solder the interconnections between the decoupling board and the rear deck assembly.

(19) TTY POWER SUPPLY A1A3Z1. (See figure 5-6.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.

2. Unsolder the interconnections between the TTY power supply and the rear deck assembly. Label unsoldered connections for proper reassembly.

3. Remove the four nuts from the studs which secure the TTY power supply to the bottom of rear deck assembly.

(b) REPLACEMENT.

1. Locate the TTY power supply over the four studs on the bottom of rear deck assembly. Secure with the four nuts.

2. Solder the interconnections between the TTY power supply and the rear deck assembly.

(20) ANTENNA TRIMMING CIRCUIT A1A1A6. (See figure 5-3.)

(a) REMOVAL.

1. Refer to paragraph 5-4b(1) for receiver disassembly instructions.
2. Disconnect the two rf cables from the antenna trimming circuit module. Label for proper reassembly.
3. Remove the two knobs from the REACT TRIM, HI/MED/LOW controls by loosening the two Allen set screws in each knob.
4. Remove the knob from the BAND MC switch by loosening the two Allen set screws in the knob.
5. Remove the two front panel face screws which secure the module to the front panel assembly.
6. Remove the module from the front panel assembly.
7. Remove the six screws which secure the module cover to the module. Remove the cover.

(b) REPLACEMENT.

1. Place the cover on the module and secure it with the six mounting screws.
2. Place the module on the front panel assembly and secure it with the two front panel face screws.
3. Install the knobs on the REACT TRIM, HI/MED/LOW controls and the BAND MC switch.
4. Connect the two rf cables to the modules.

5-5. MAINTENANCE ILLUSTRATIONS.

The illustrations contained in this section of the manual are for use by the technician to maintain, trouble shoot, and repair the receiving set. They consist of parts location illustrations, schematic diagrams of the modules and plug-in cards, and a primary power distribution diagram.

a. PART LOCATION ILLUSTRATIONS. - Figures 5-1 through 5-51 are the part location illustrations. They identify, by means of call-outs, the relative location of all circuit elements and test points.

Note

Part location illustrations are primarily for ready reference for technical manual purposes. The call-outs and markings on these illustrations do not necessarily reflect the actual markings on the equipment. The actual equipment markings may be greatly reduced in legibility due to standard manufacturing processes such as soldering and coating.

b. PRIMARY-POWER DISTRIBUTION DIAGRAM. - Figure 5-52 shows the distribution of primary power in the receiving set. It is an across-the-line type diagram showing the circuit elements directly related to the distribution of ac or dc primary power within the set.

c. SCHEMATIC DIAGRAMS. - Schematic diagrams of each module or card in the receiving set, together with the module interconnection diagrams, are provided in figures 5-53 through 5-80. Primary signal flow is indicated by a heavy-weight line with arrowheads to indicate the direction of flow. Secondary signal paths, where applicable, are indicated by light-weight lines with arrowheads. Circuit sections which are not a part of the module or card but are included to clarify the circuit functions are enclosed in individual dotted-line blocks. The following information applies to all schematic diagrams in this section of the manual:

(1) All part values are given in ohms, picofarads, and microhenries unless otherwise indicated.

(2) The dc resistance of inductors and transformer windings is omitted if less than one ohm.

(3) All resistors are rated 1/4 watt unless otherwise indicated.

(4) All dc voltages are measured between card terminals and the set chassis using a 20,000 ohm-per-volt meter, unless otherwise indicated. All ac voltage measurements, with the exception of rf signal measurements, are performed using a 1000 ohm-per-volt meter unless otherwise indicated.

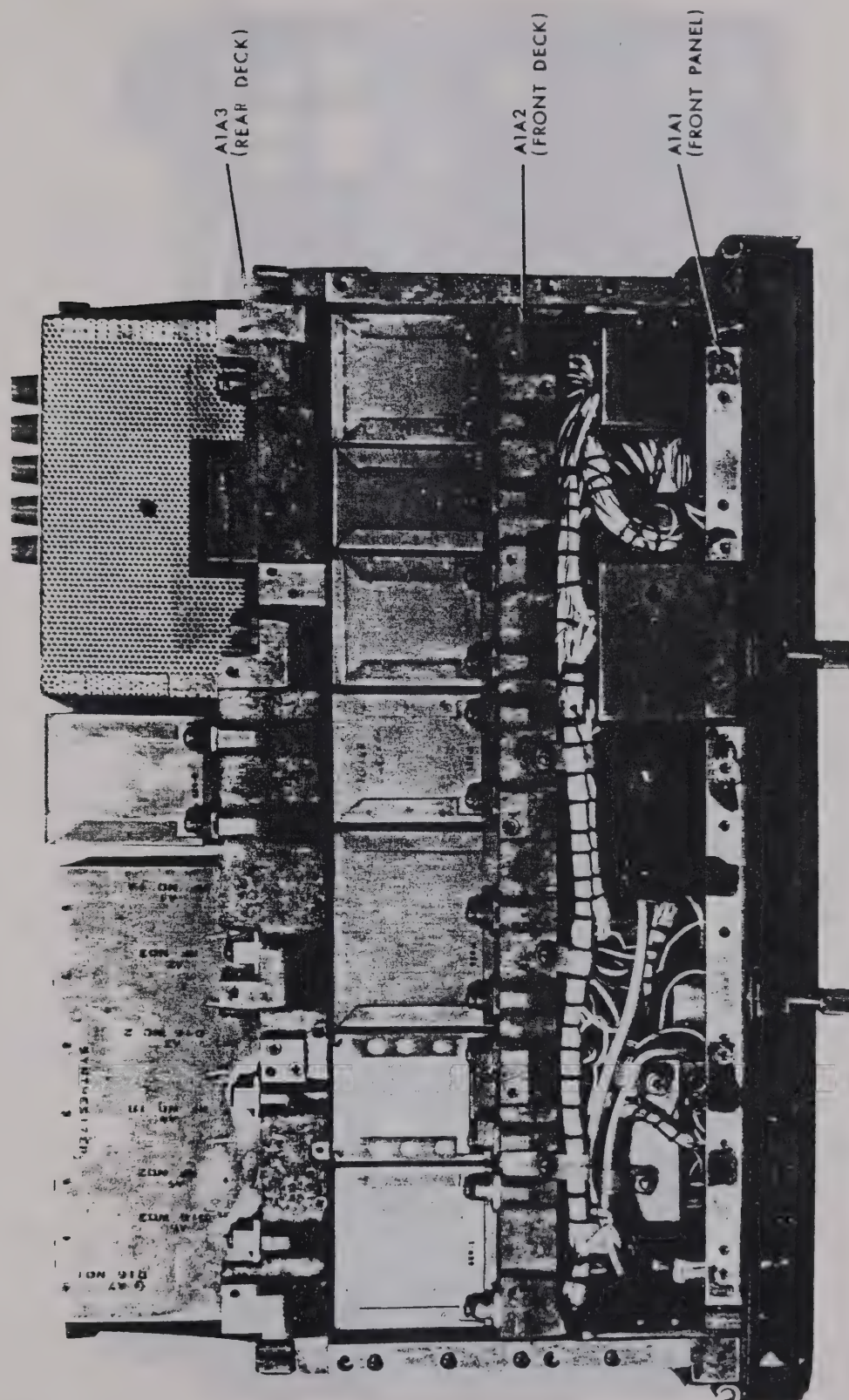


Figure 5-1. Receiver, Radio R-1490/GRR-17, Top View with Transit Case Removed

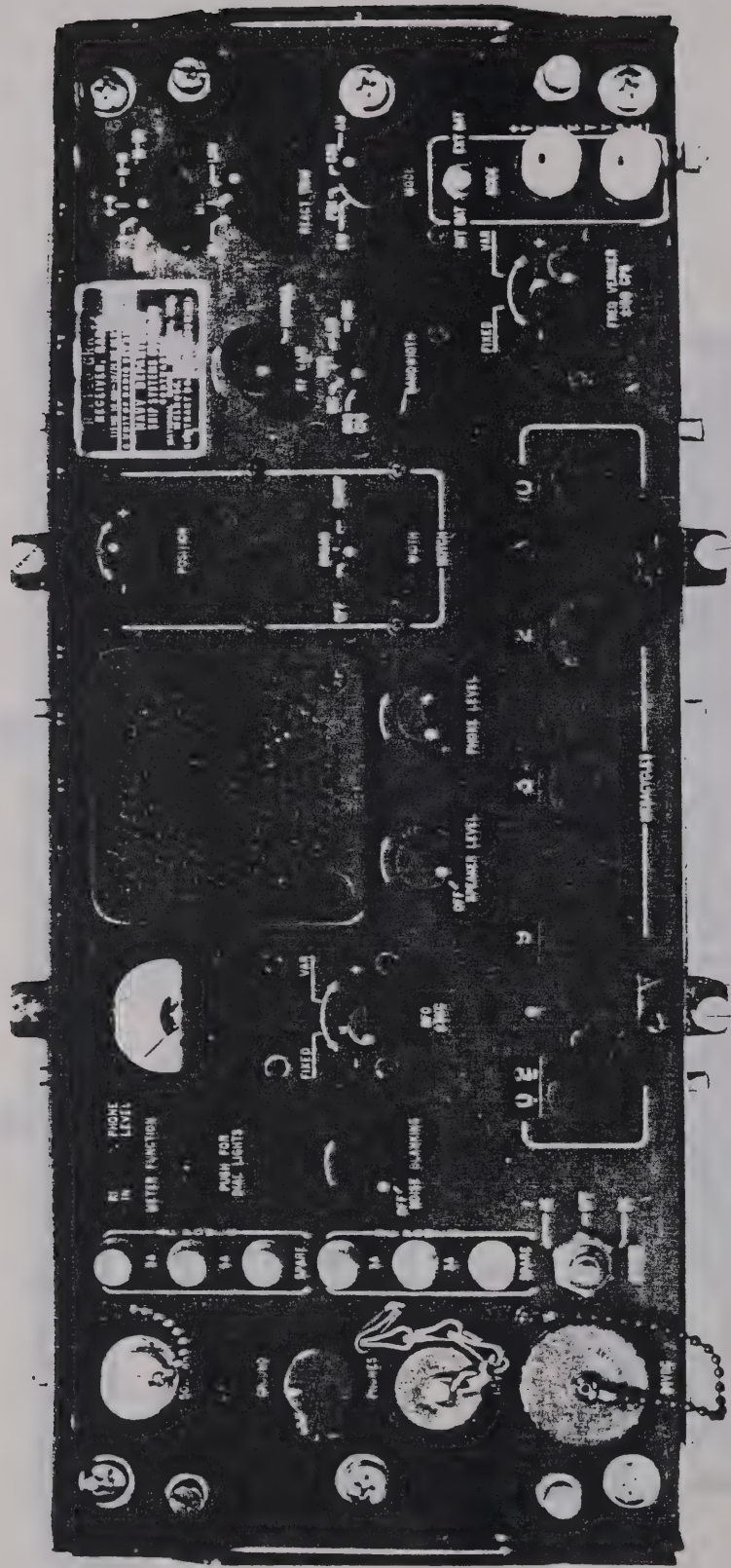


Figure 5-2. Front Panel A1A1, Front View

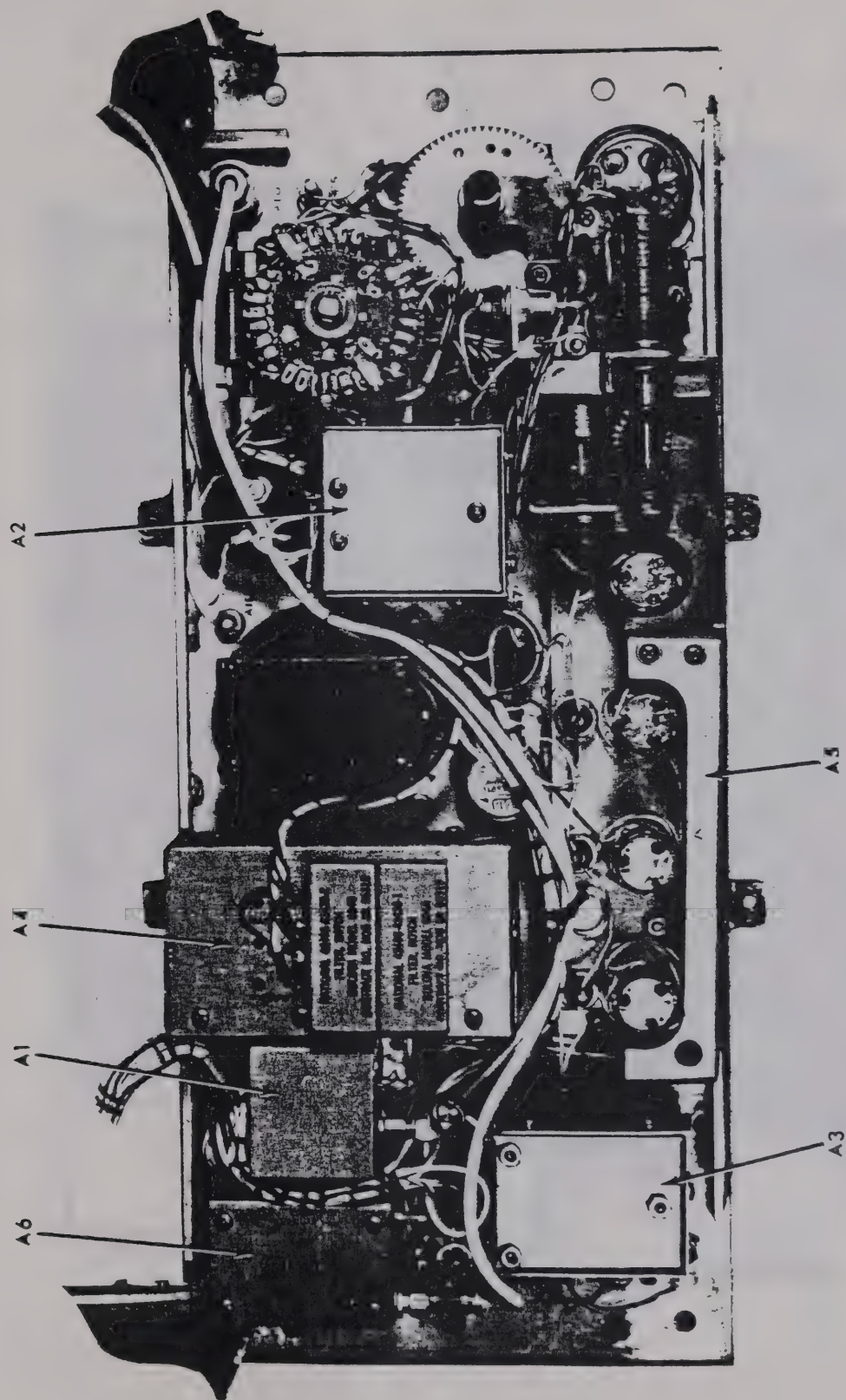


Figure 5-3. Front Panel A1A1, Rear View

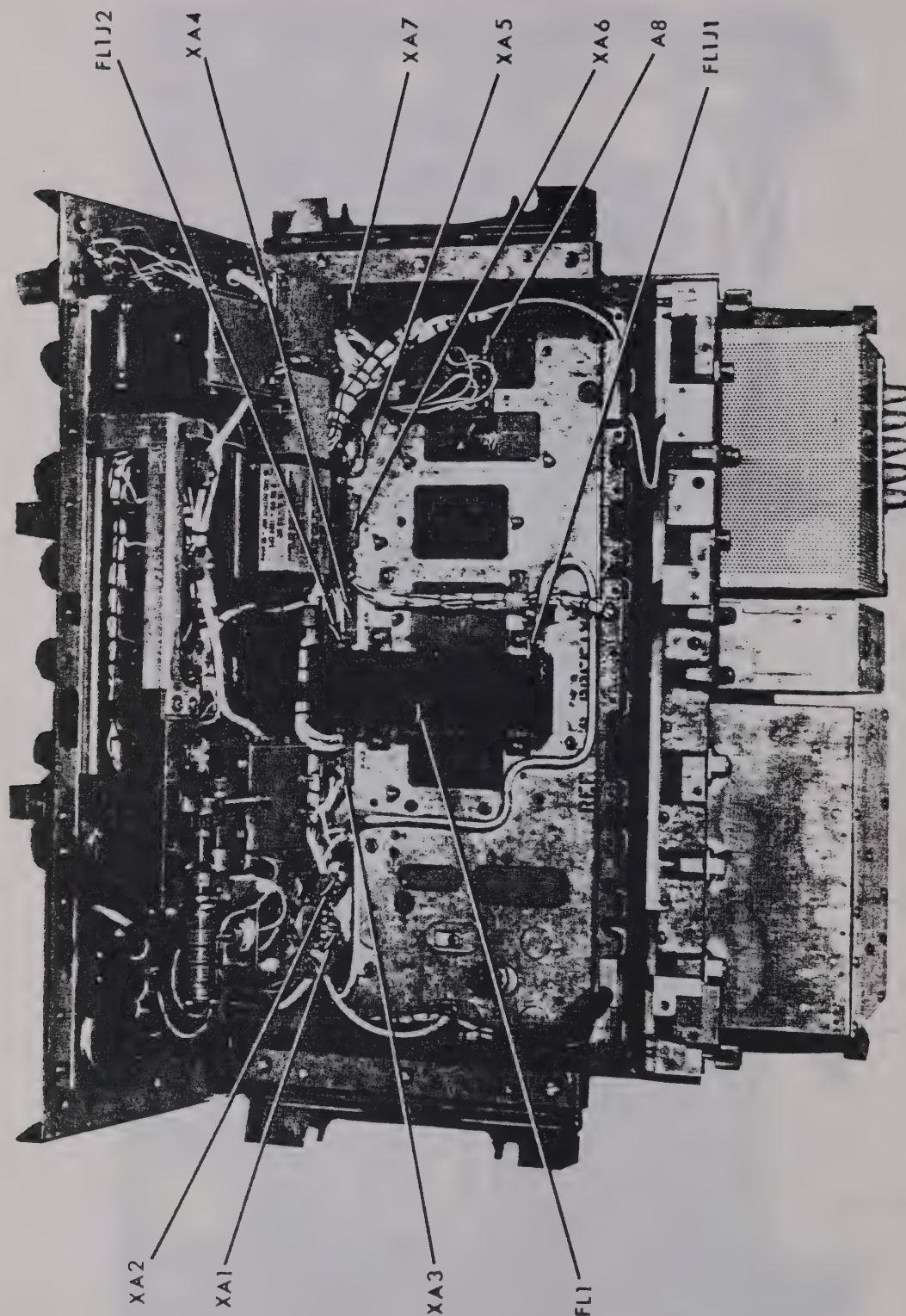


Figure 5-4. Front Deck A1A2, Bottom View

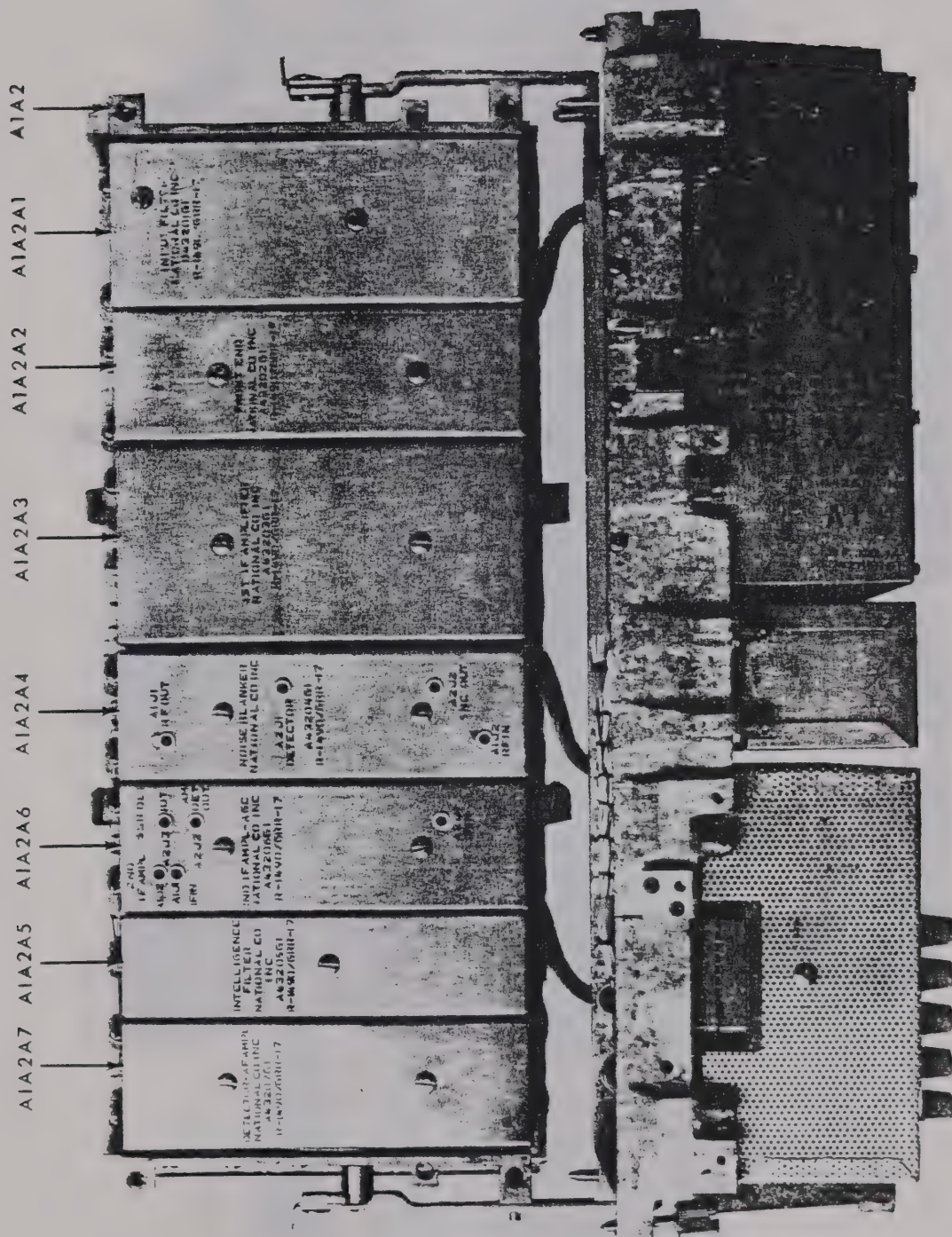


Figure 5-5. Front Deck A1A2, Top View

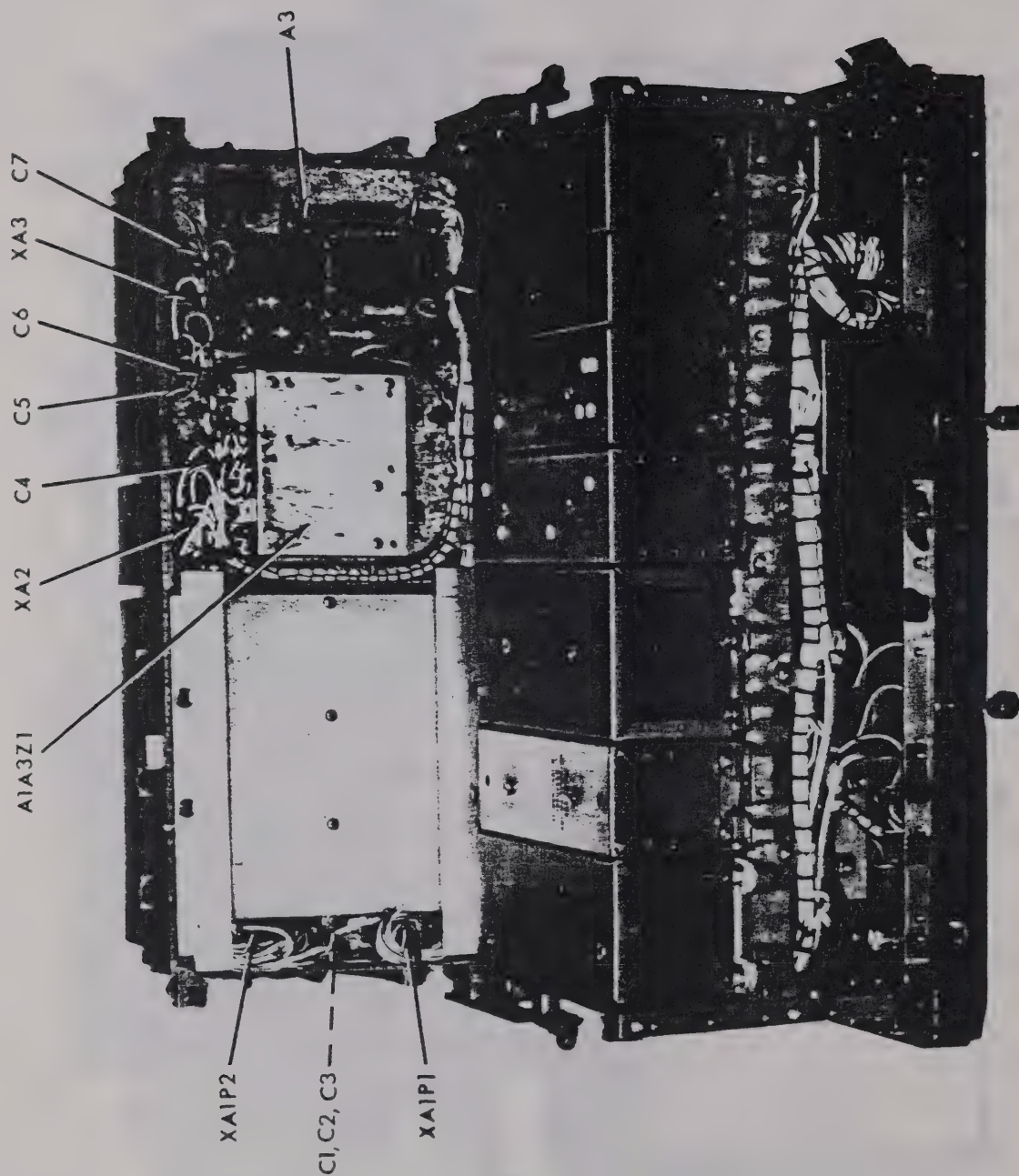
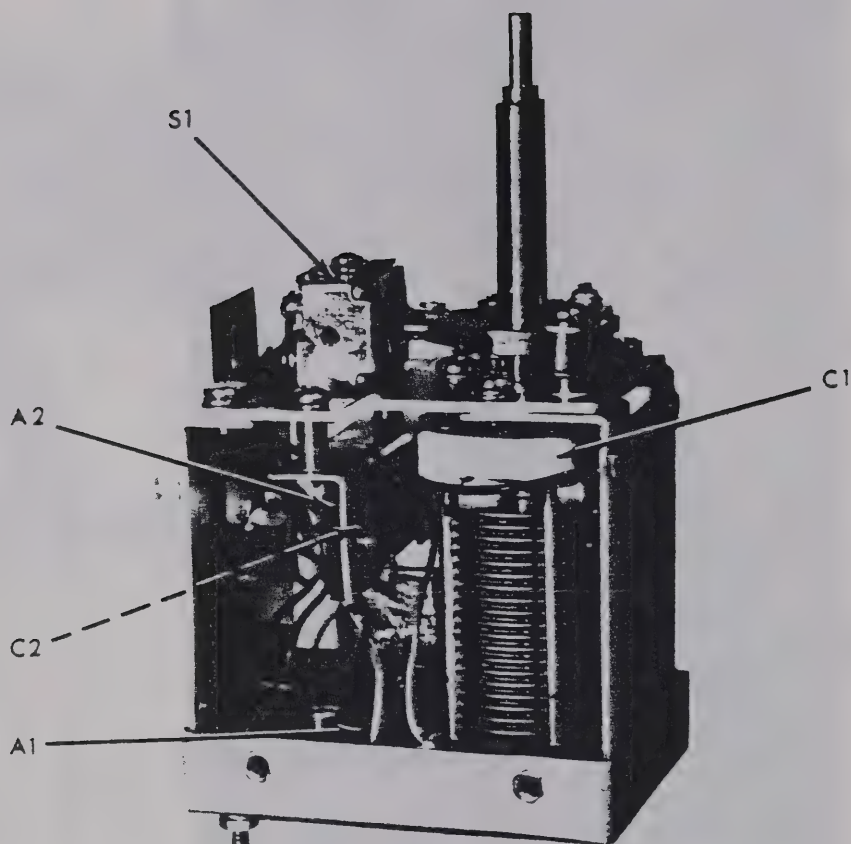


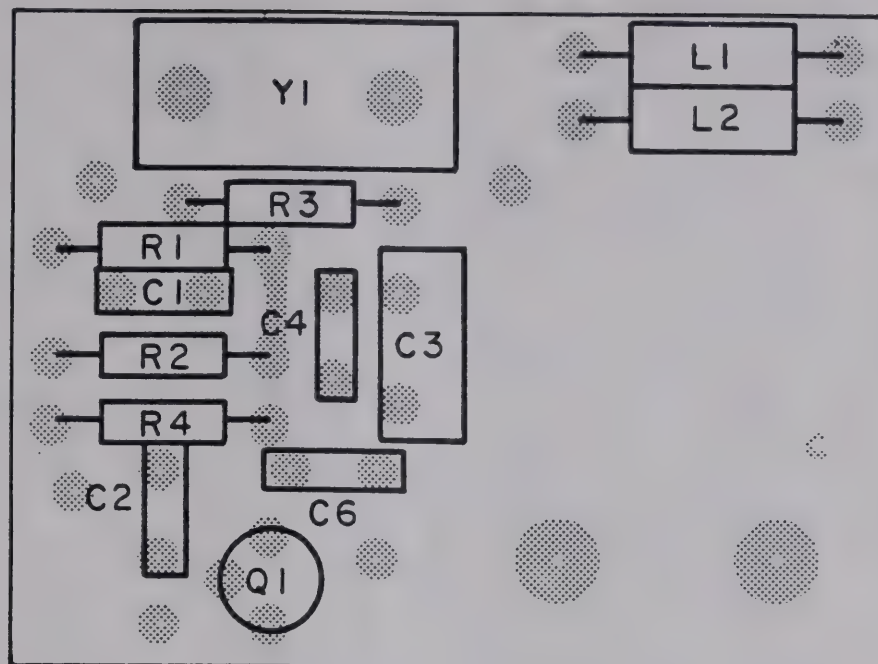
Figure 5-6. Rear Deck A1A3, Bottom View

Figure 5-7. Rear Deck A1A3, Top View

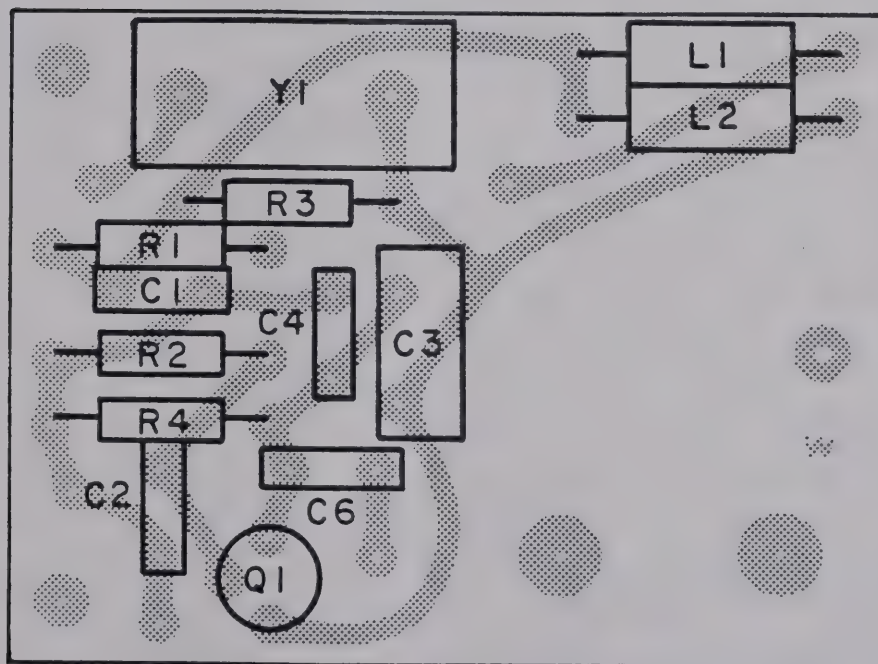


REF DES PREFIX:
A1A1A3

Figure 5-8. VFO A1A1A3, Parts Location



Component Side



Wire Side

Figure 5-9. VFO A1A1A3, Oscillator A1, Parts Location

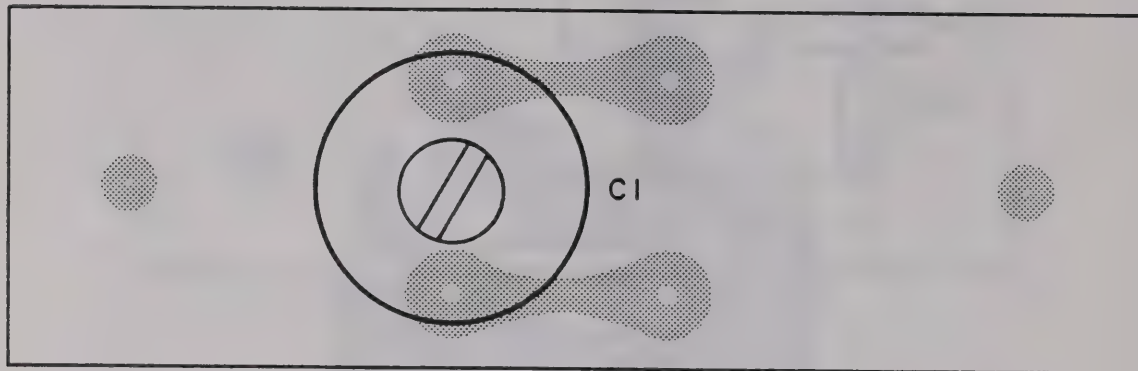
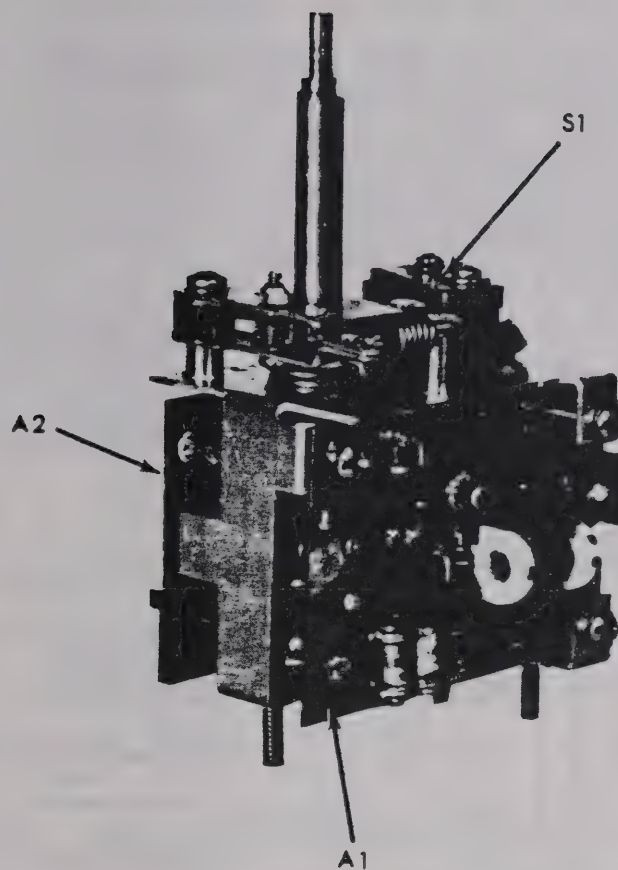


Figure 5-10. VFO A1A1A3, Tuning A2, Parts Location



REF DES PREFIX:
A1A1A2

Figure 5-11. BFO A1A1A2, Parts Location

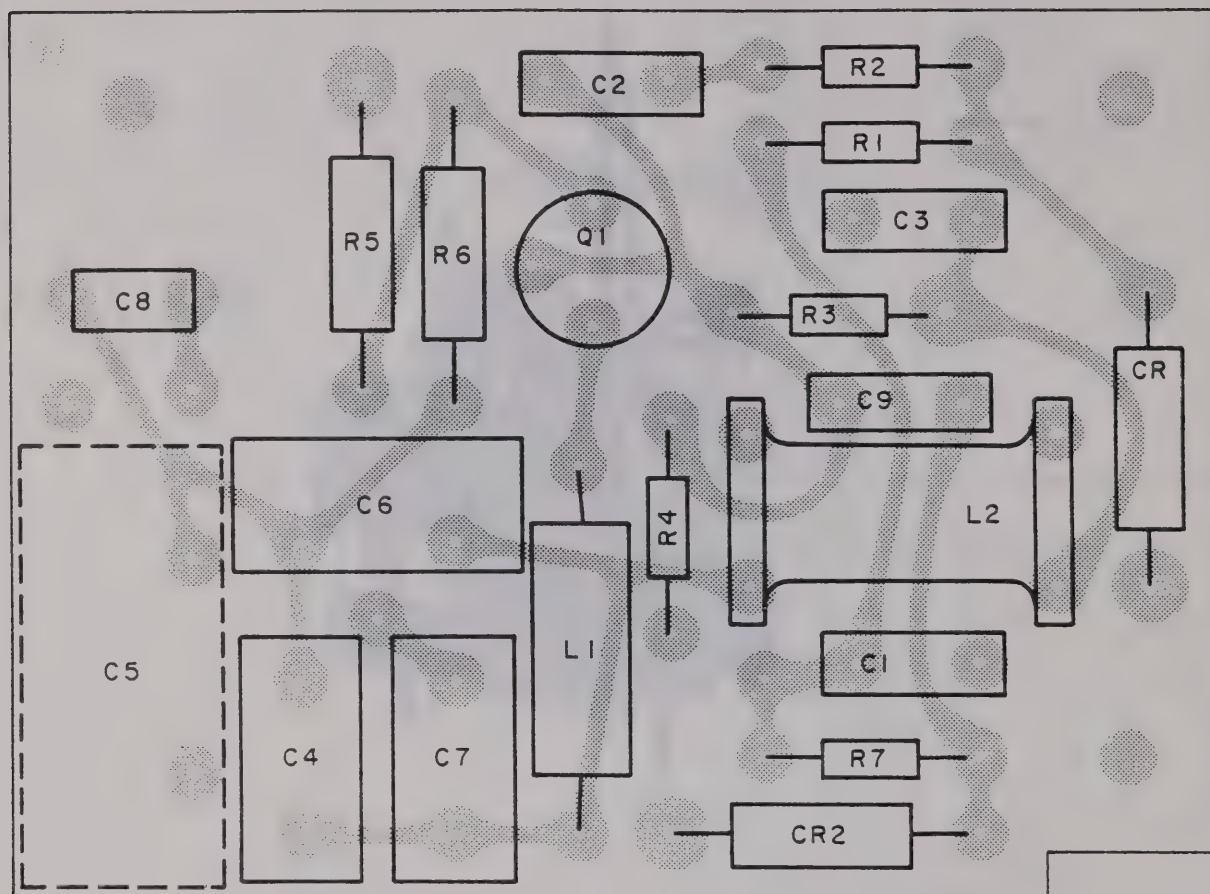
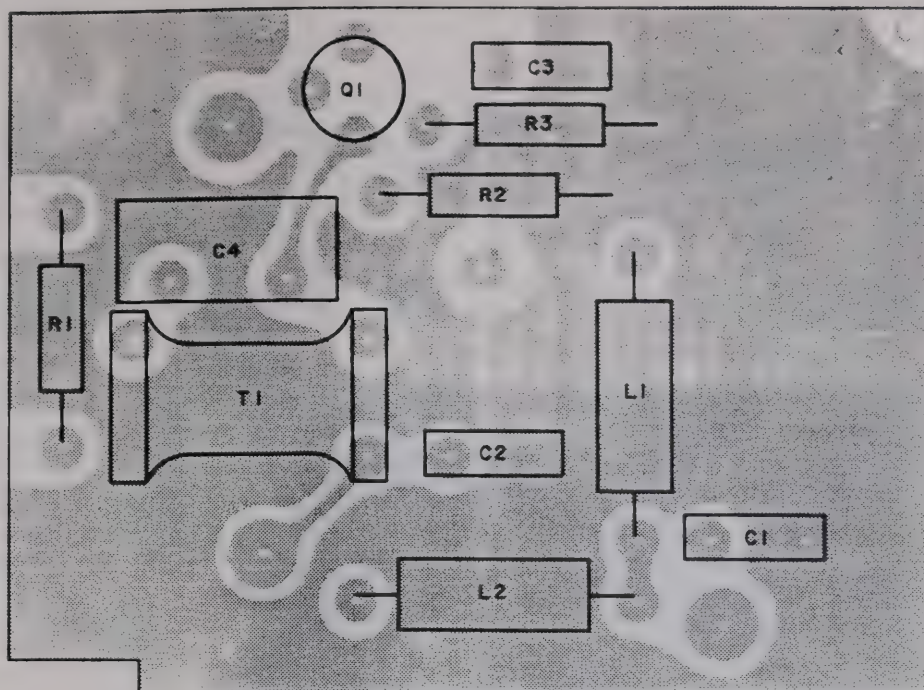
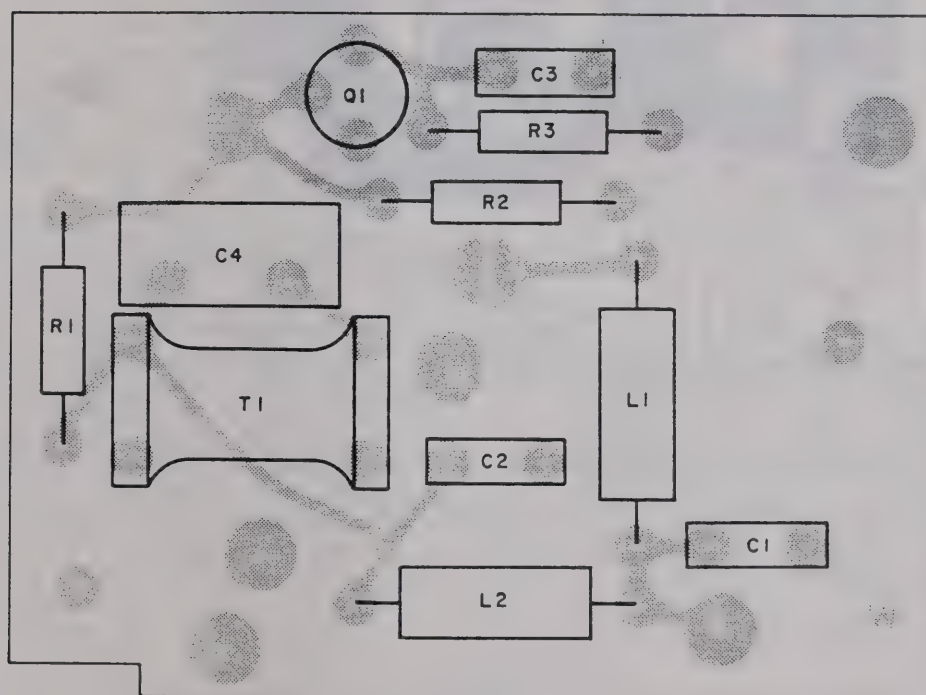


Figure 5-12. BFO A1A1A2, Oscillator A2, Parts Location



Component Side



Wire Side

Figure 5-13. BFO A1A1A2, Amplifier A1, Parts Location

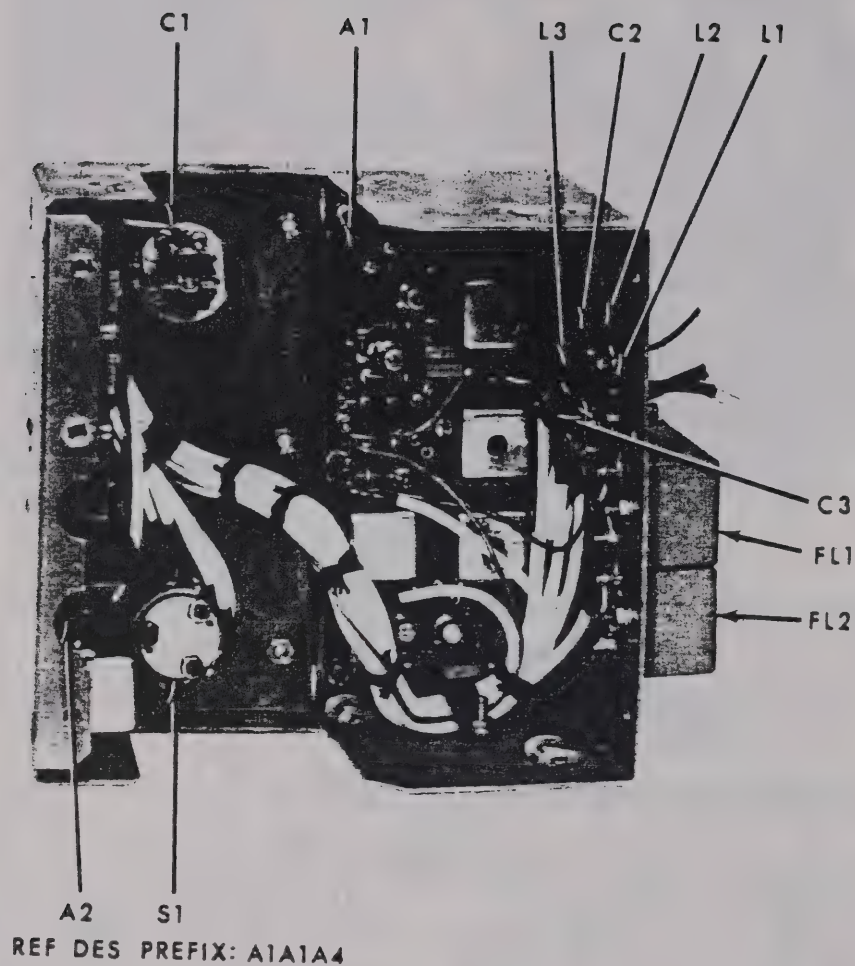
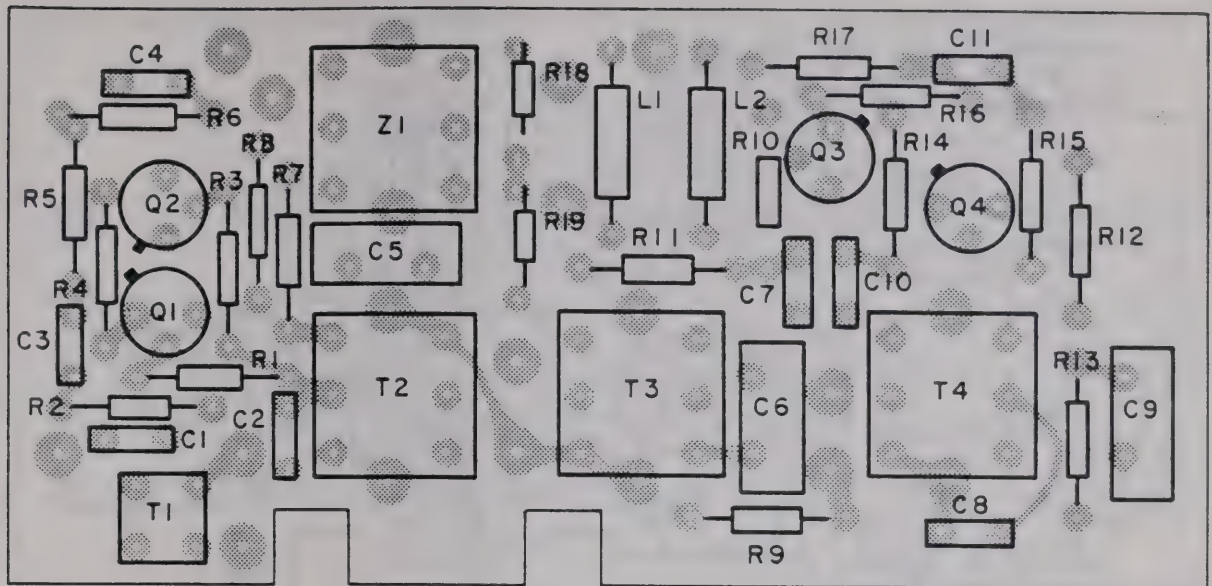
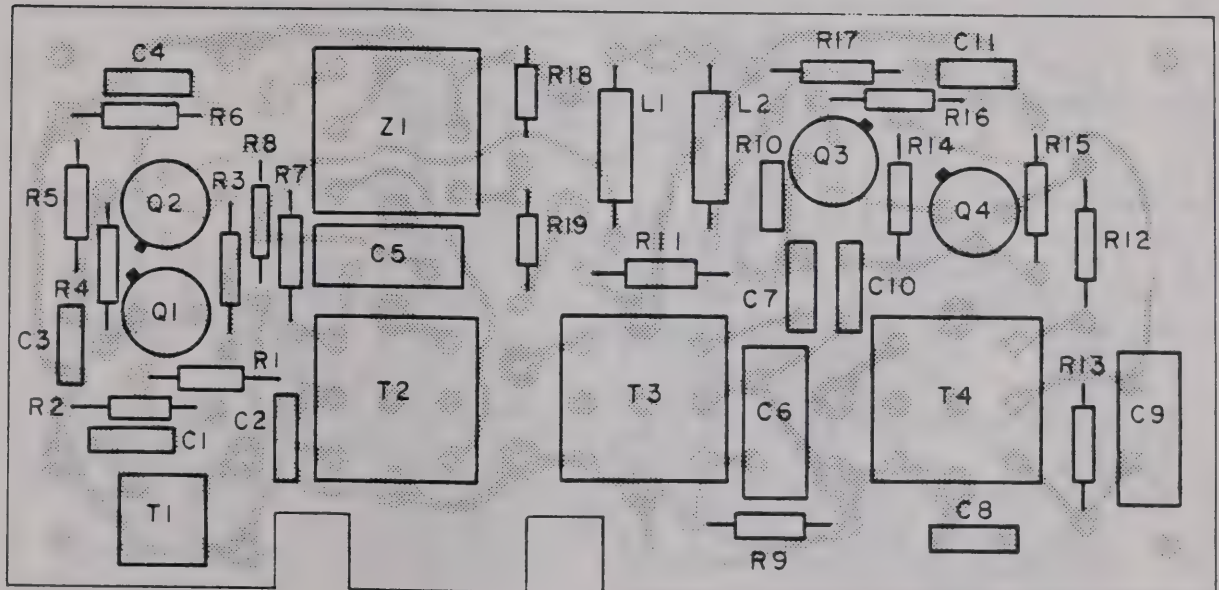


Figure 5-14. Notch Filter A1A1A4, Parts Location

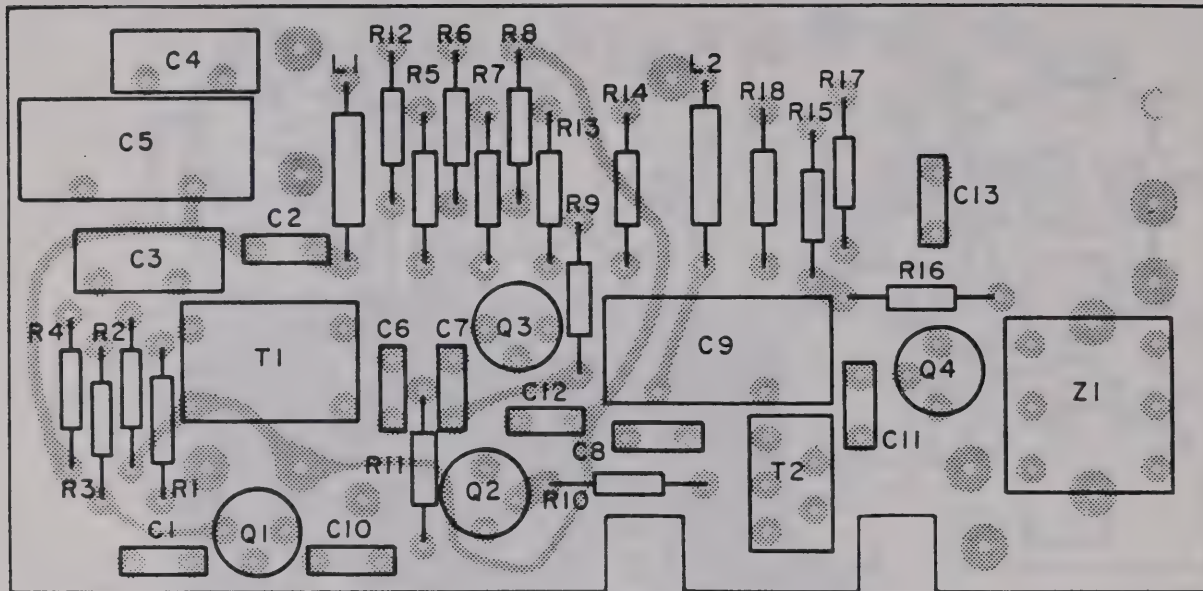


Component Side

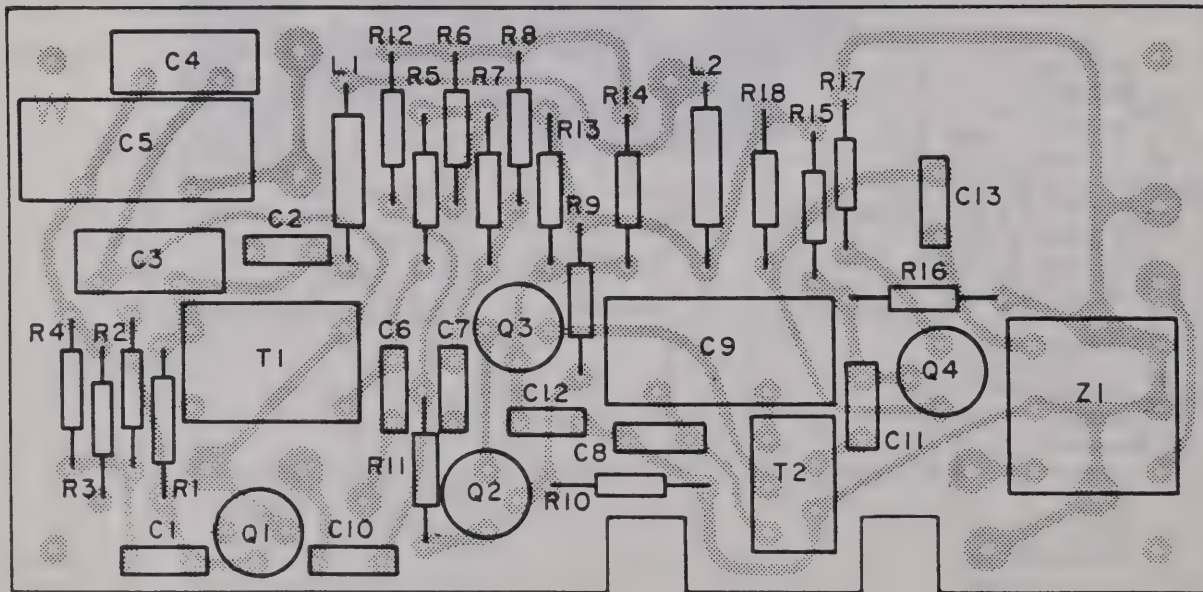


Wire Side

Figure 5-15. Notch Filter A1A1A4, Amplifier-Mixer A2, Parts Location



Component Side



Wire Side

Figure 5-16. Notch Filter A1A1A4, Oscillator-Mixer A1, Parts Location

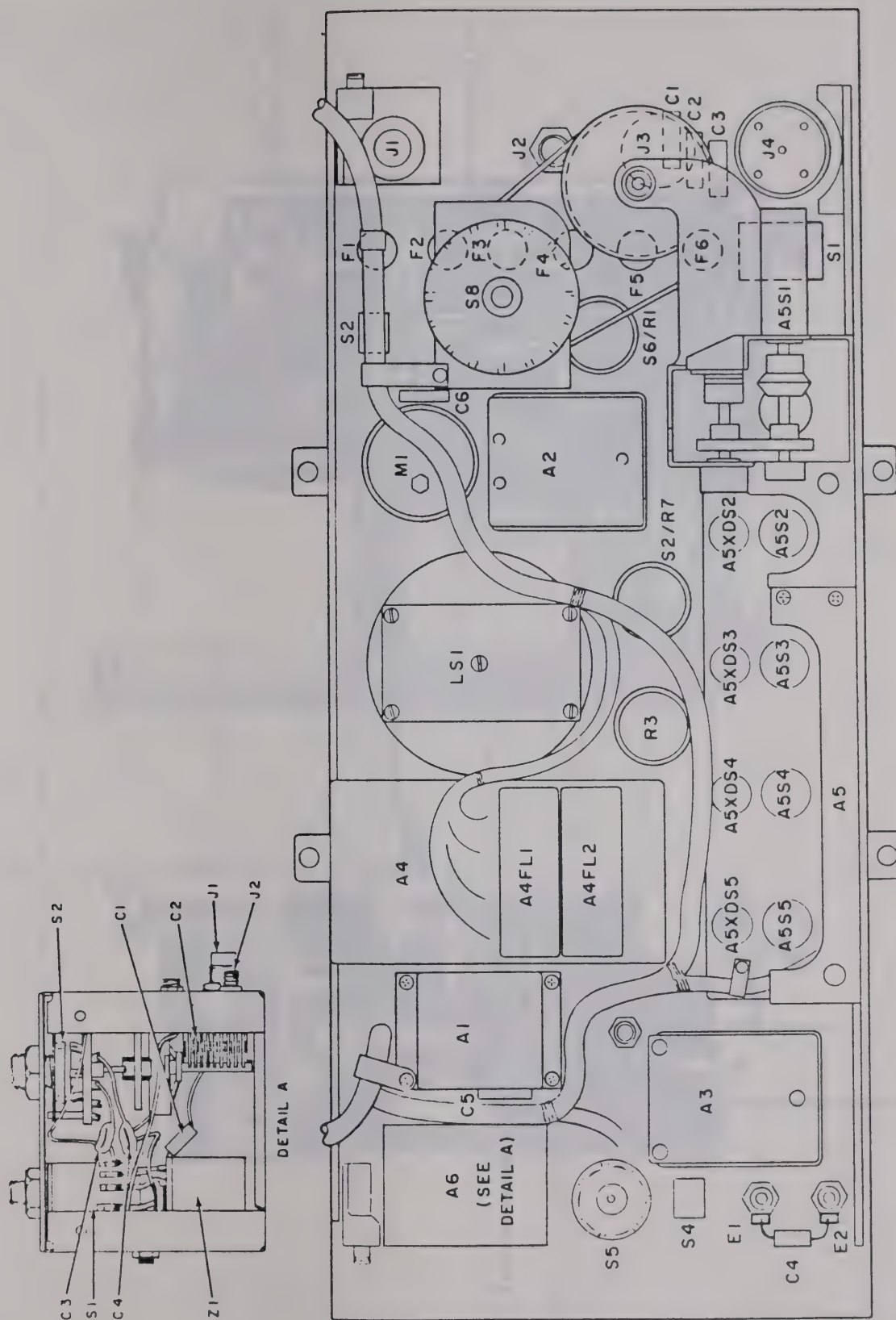


Figure 5-17. MEGACYCLES Frequency Selector A1A5, Parts Location

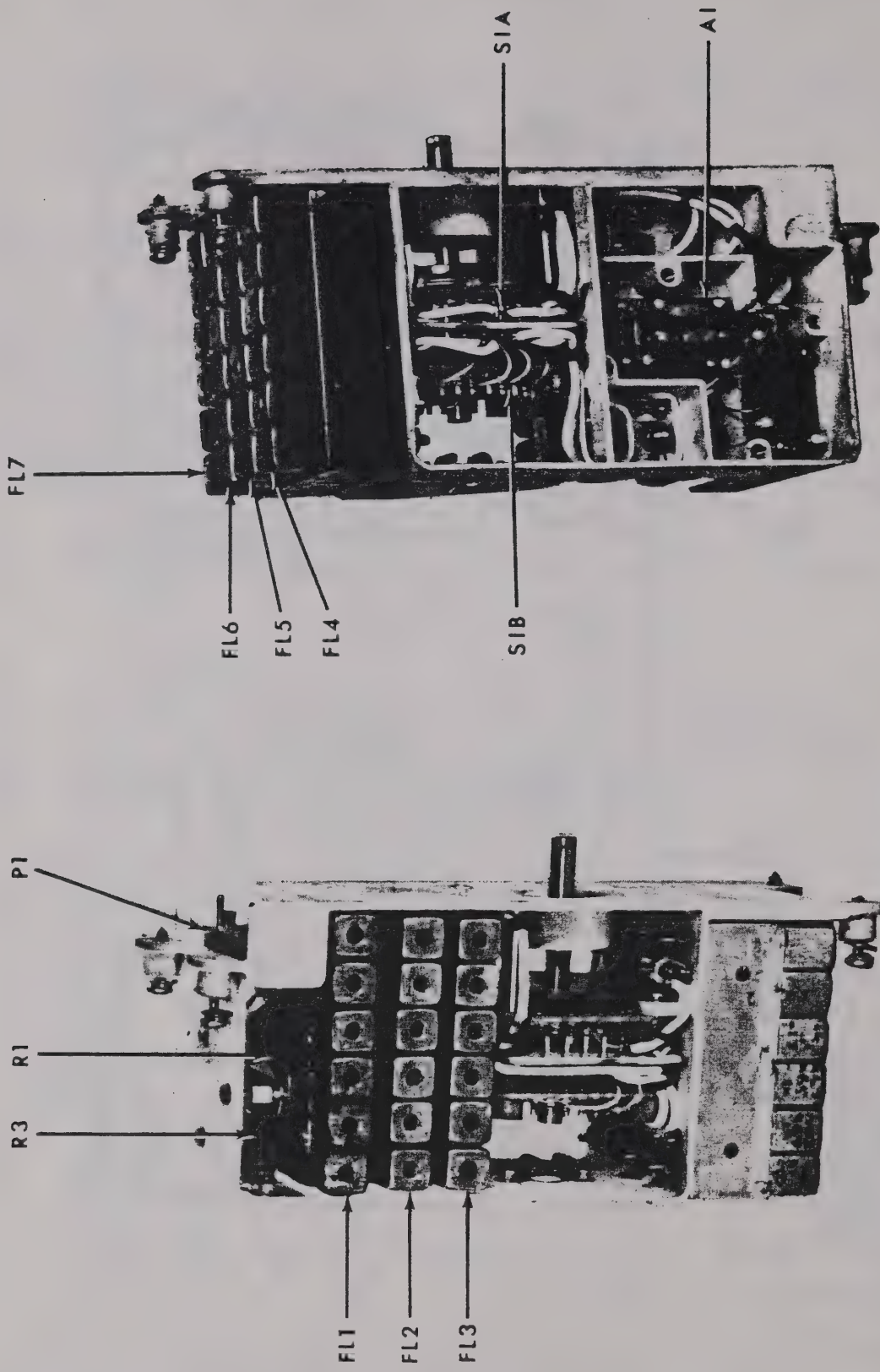
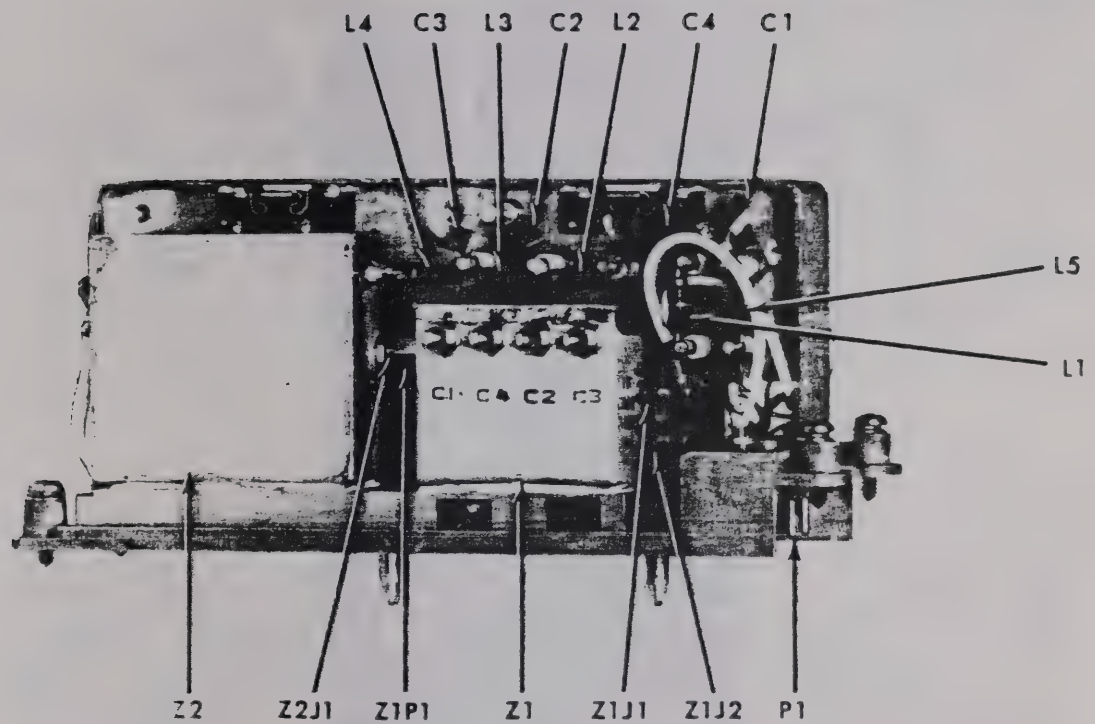
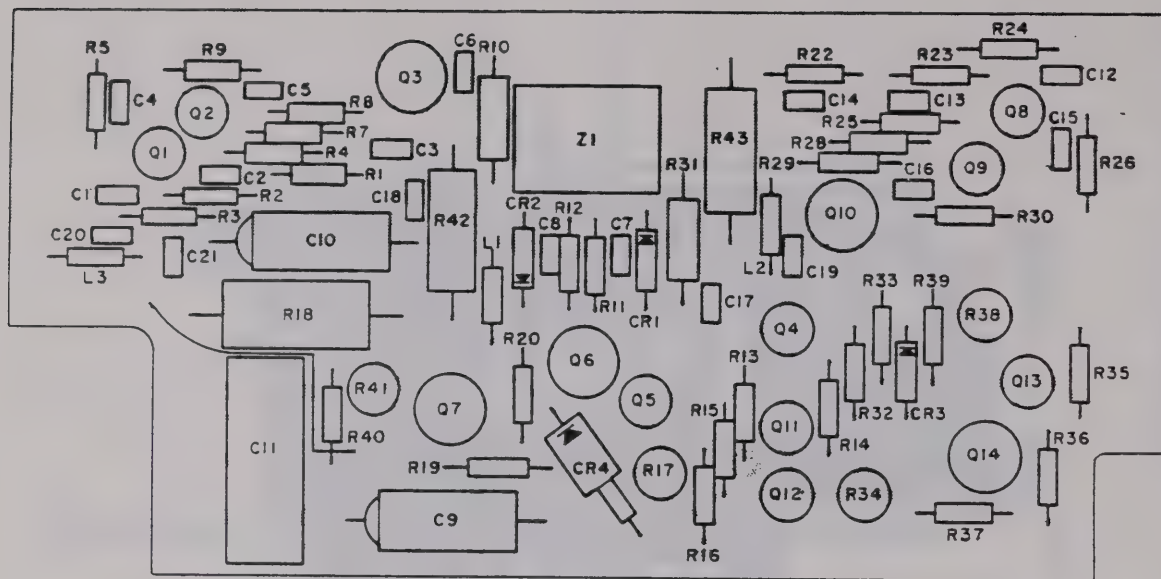


Figure 5-18. Input Filter ALA2A1, Parts Location

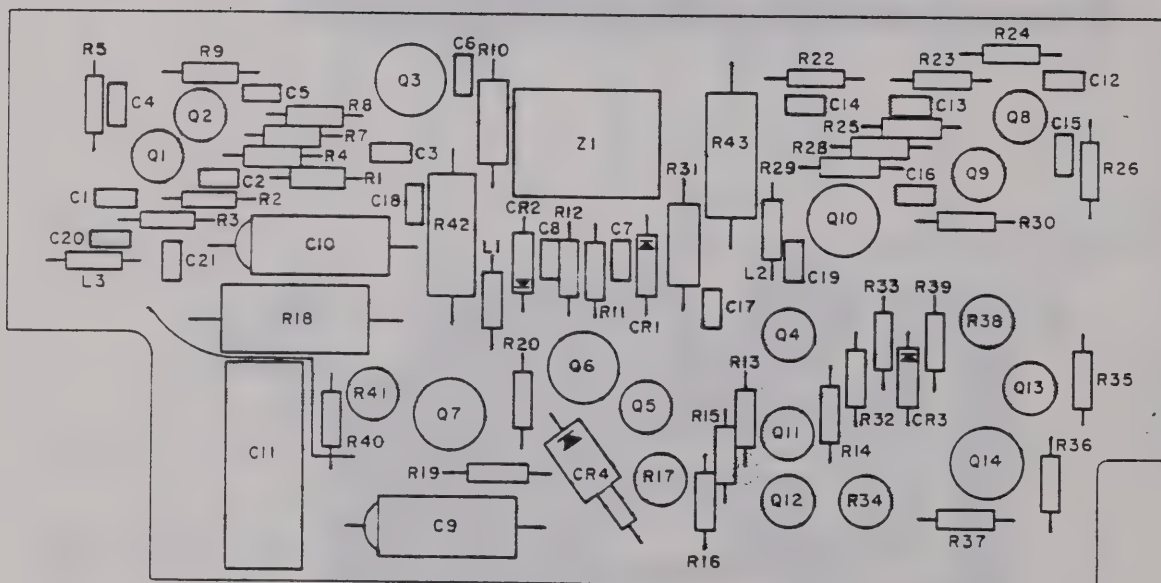


REF DES PREFIX: A1A2A2

Figure 5-19. Front End A1A2A2, Parts Location

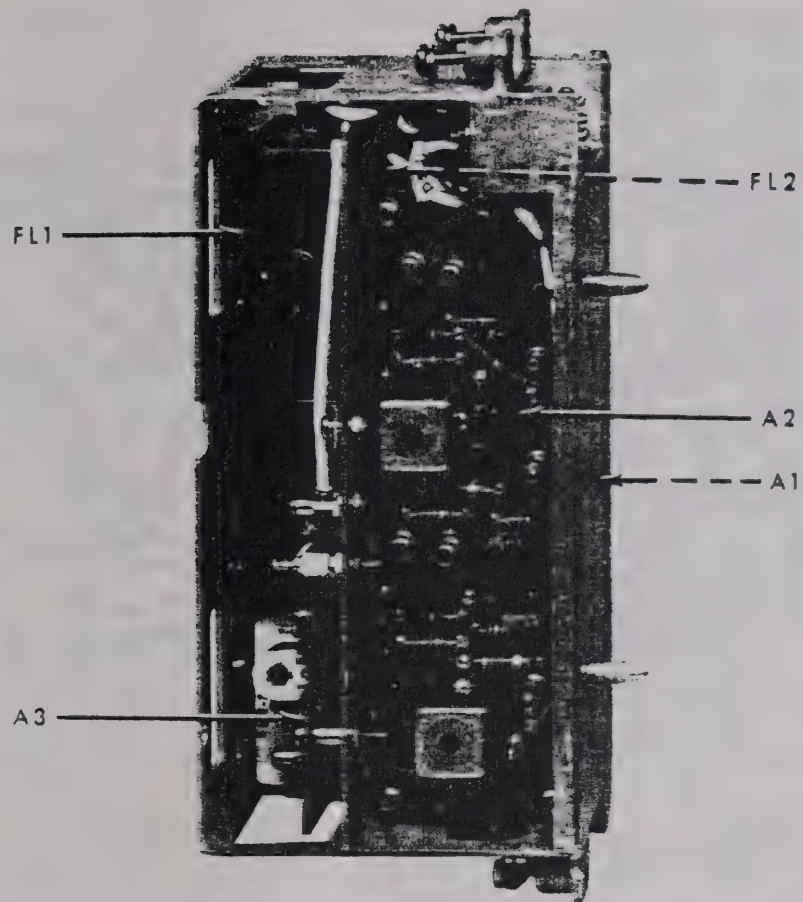


Component Side



Wire Side

Figure 5-20. VHF Oscillator Phase-Locked Loop AlA2A2A1, Parts Location



REF DES PREFIX: A1A2A3

Figure 5-21. First I-F Amplifier A1A2A3, Parts Location

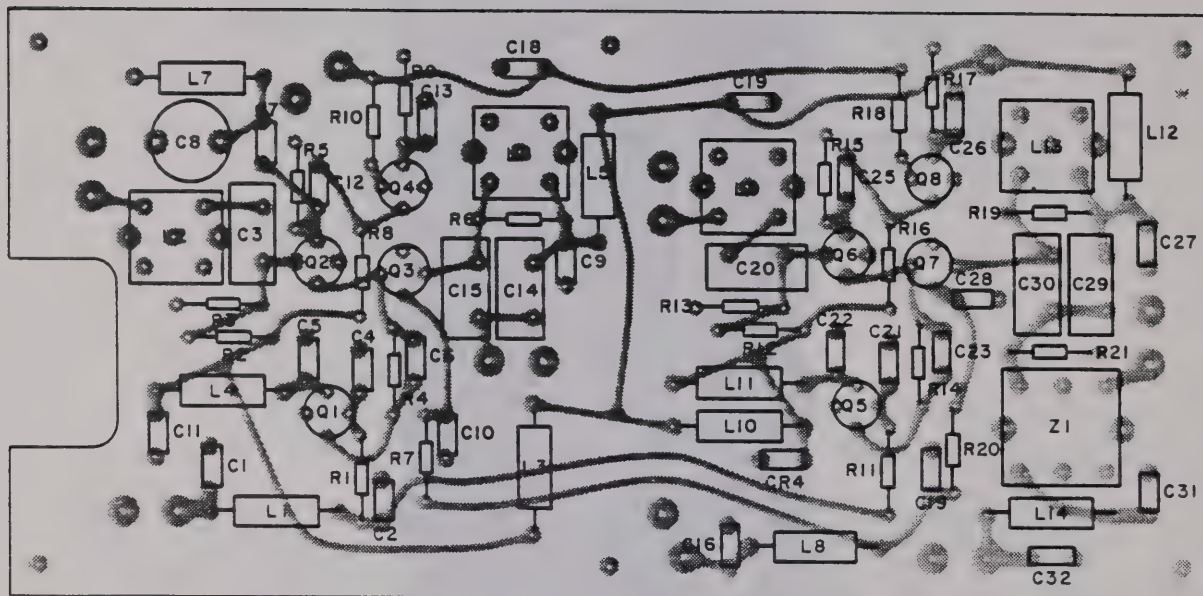
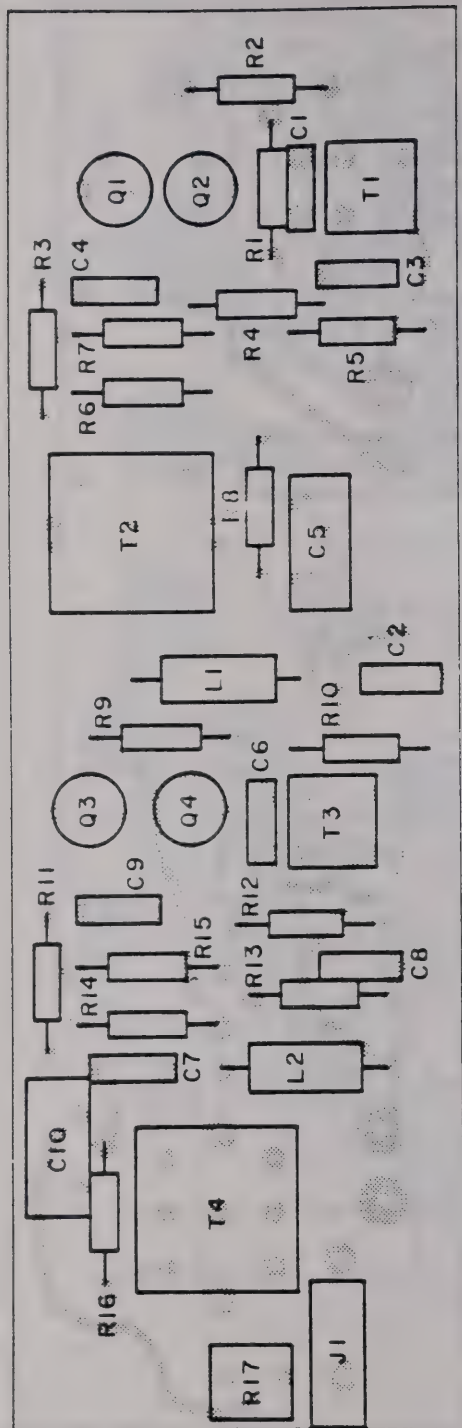
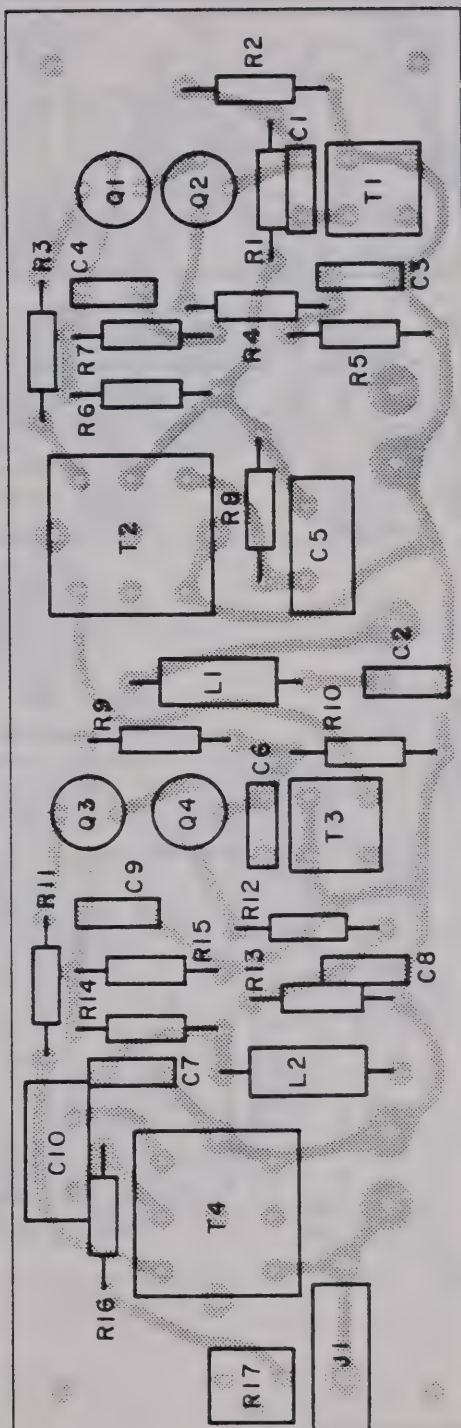


Figure 5-22. First I-F Amplifier AlA2A3, 112 MC I-F Amplifier A1,
Parts Location



Component Side



Wire Side

Figure 5-23. First I-F Amplifier A1A2A3, Reserve Gain Amplifier A2, Parts Location

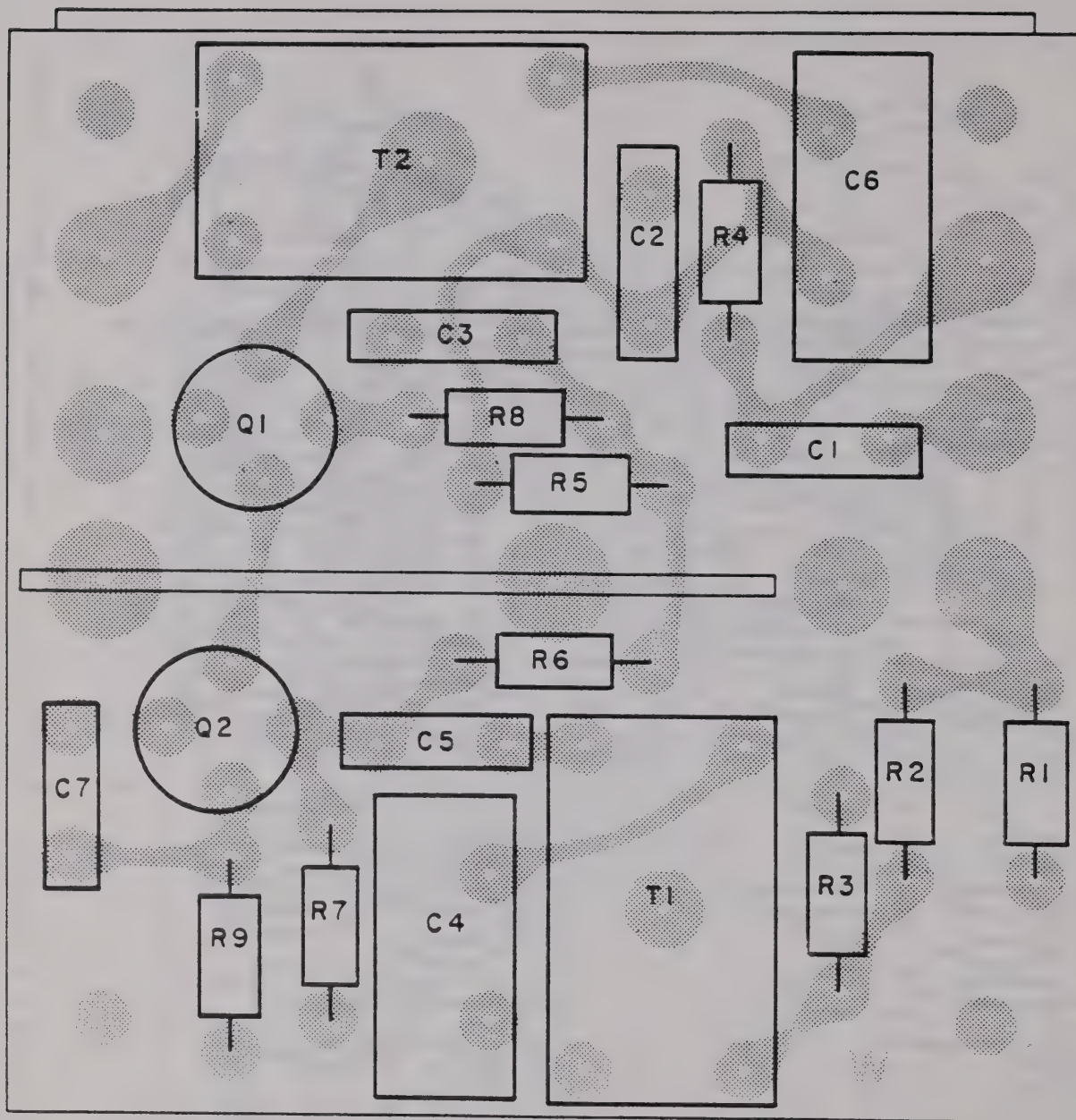
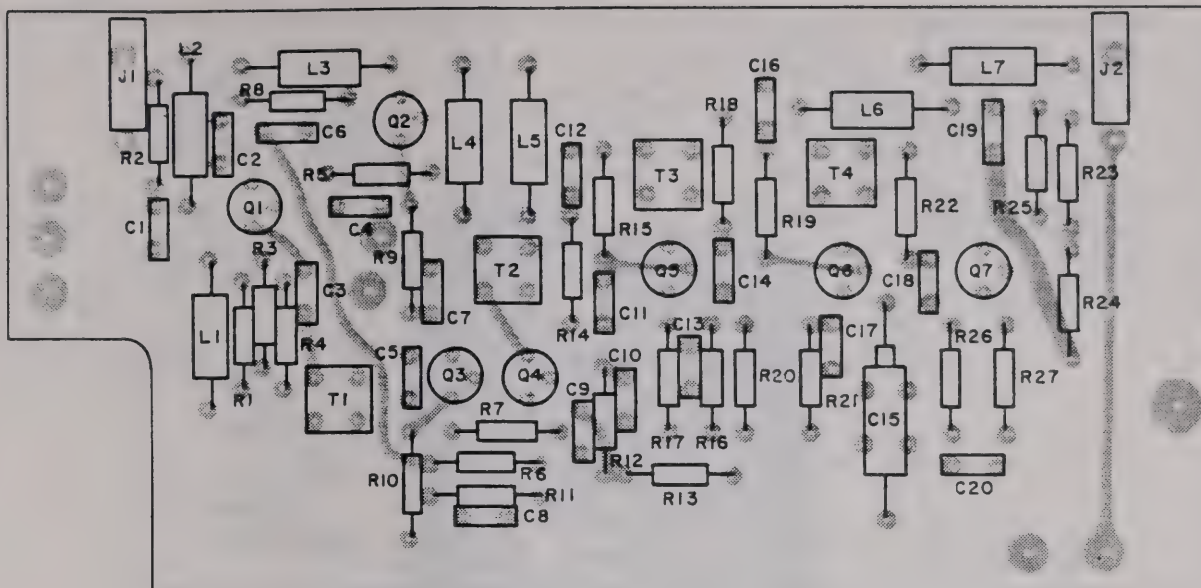
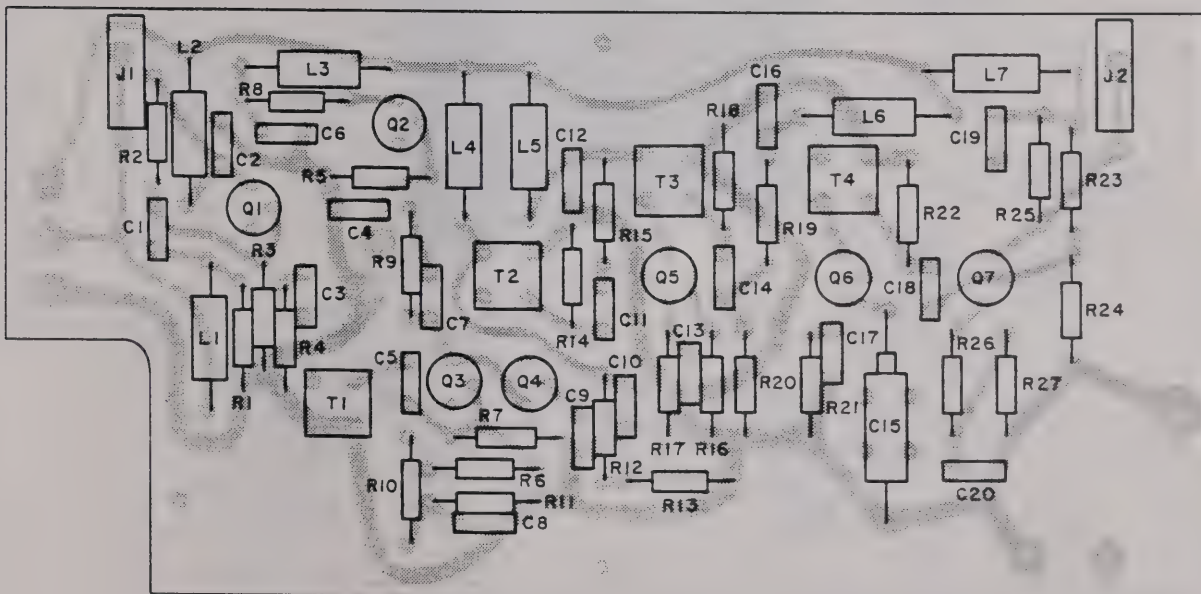


Figure 5-24. First I-F Amplifier A1A2A3, 117 MC Buffer Amplifier A3,
Parts Location

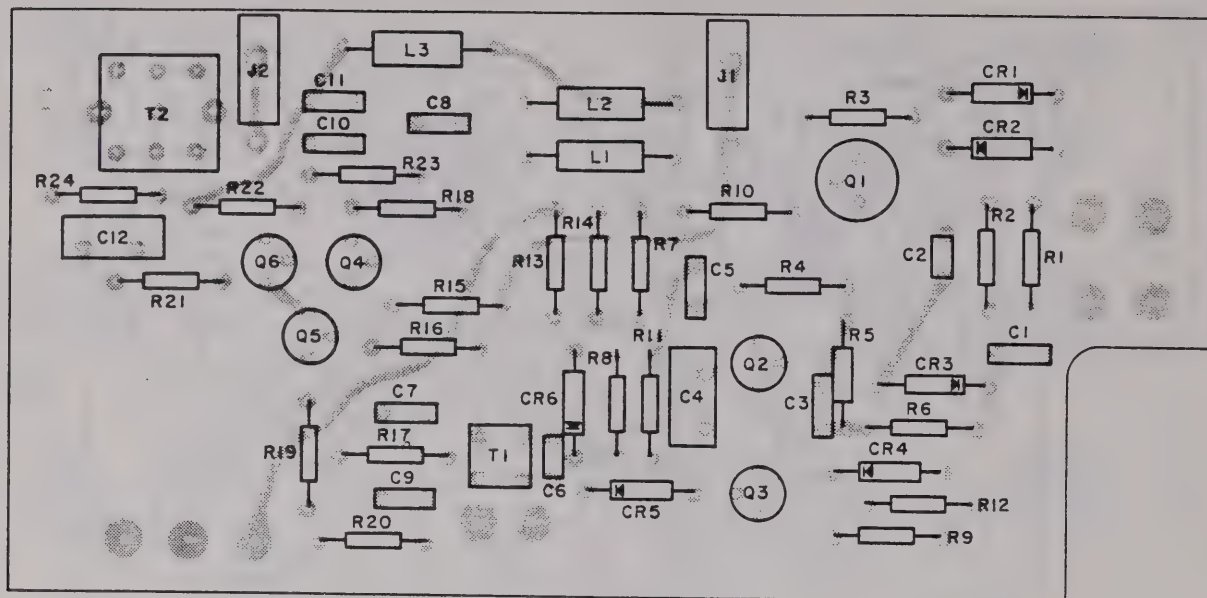


Component Side

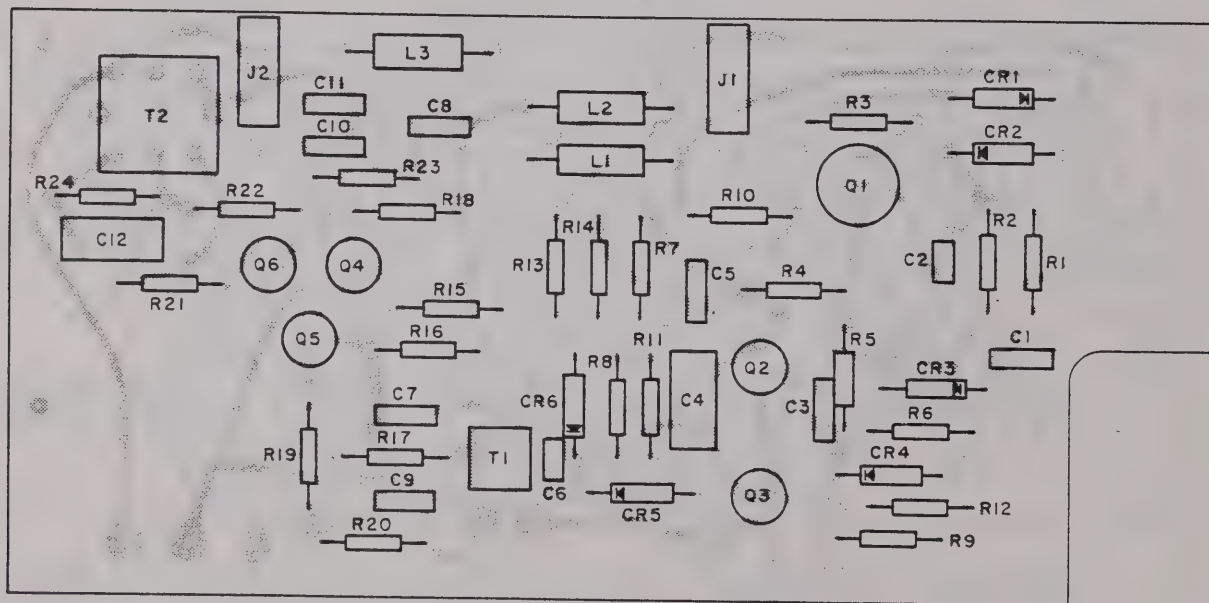


Wire Side

Figure 5-25. Noise Blanker A1A2A4, 5 MC Amplifier A1, Parts Location

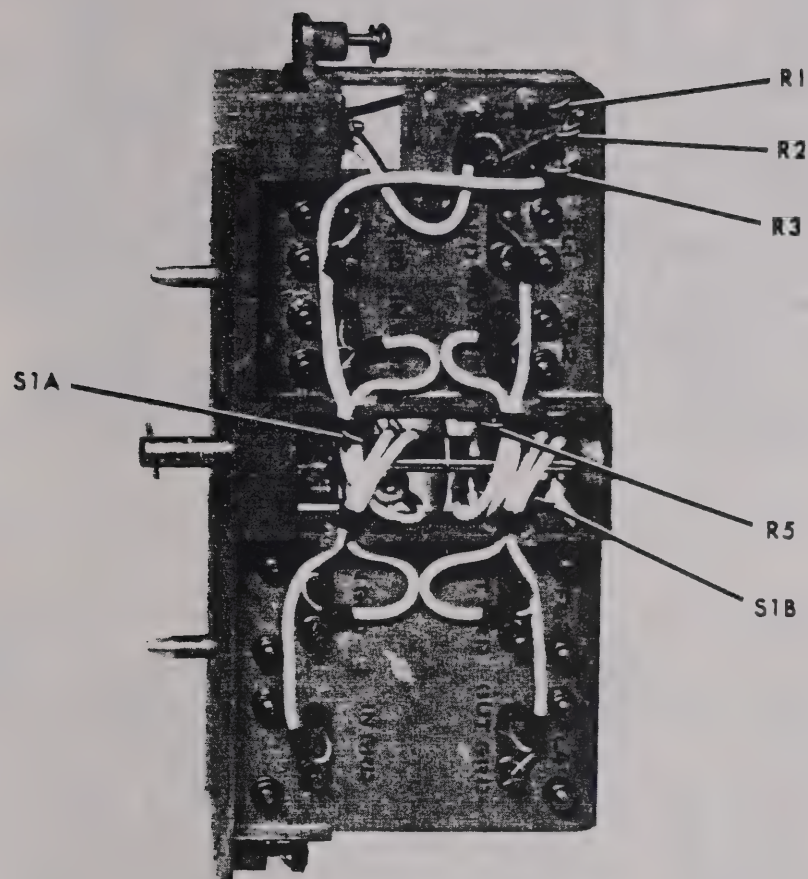


Component Side



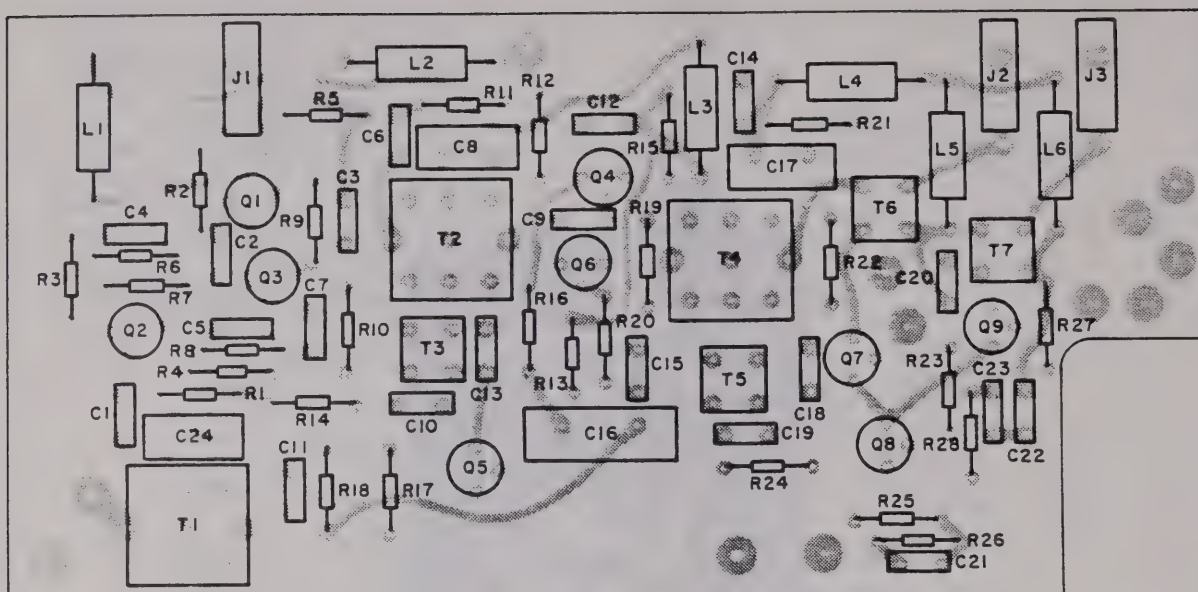
Wire Side

Figure 5-26. Noise Blanker A1A2A4, Detector/Gated Amplifier A2, Parts Location

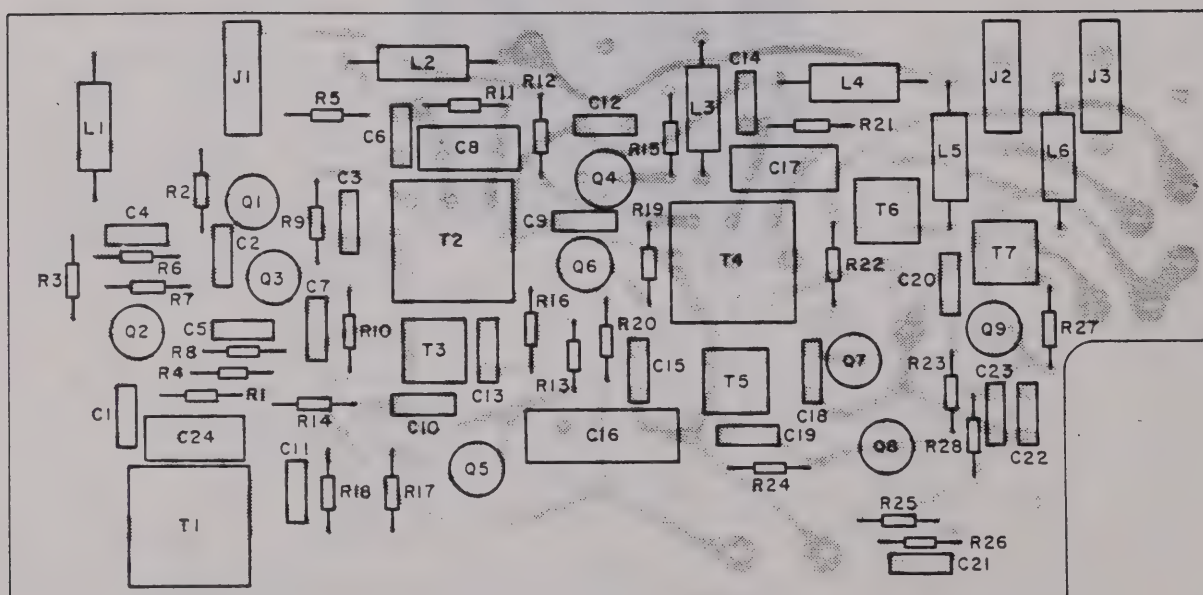


REF DES PREFIX: A1A2A5

Figure 5-27. Intelligence Filter A1A2A5, Parts Location

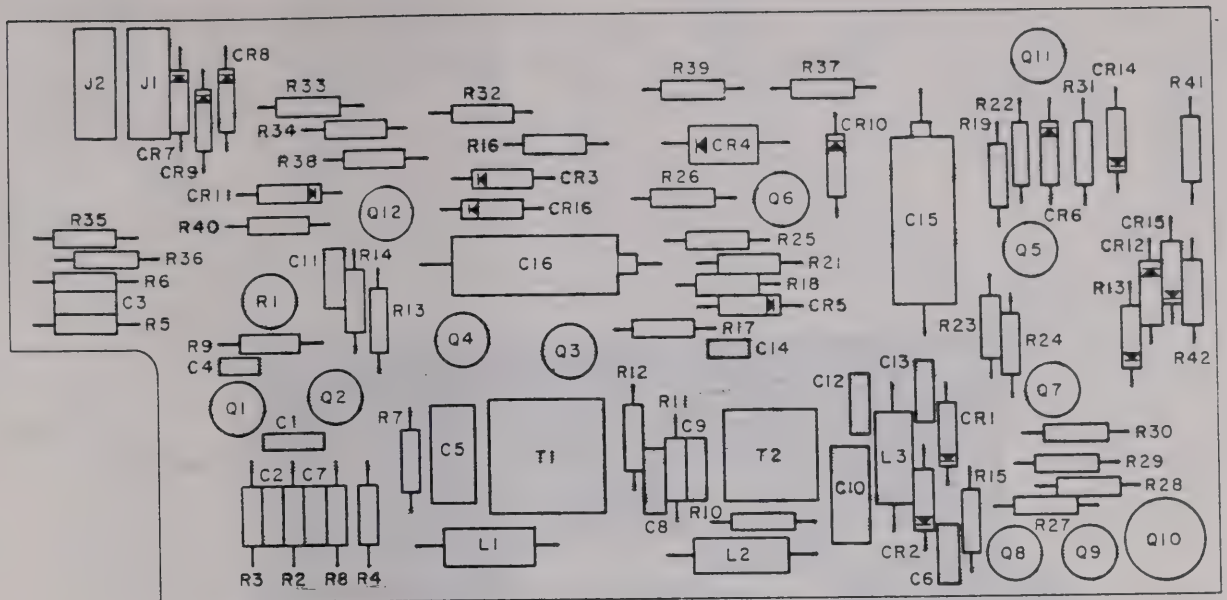


Component Side

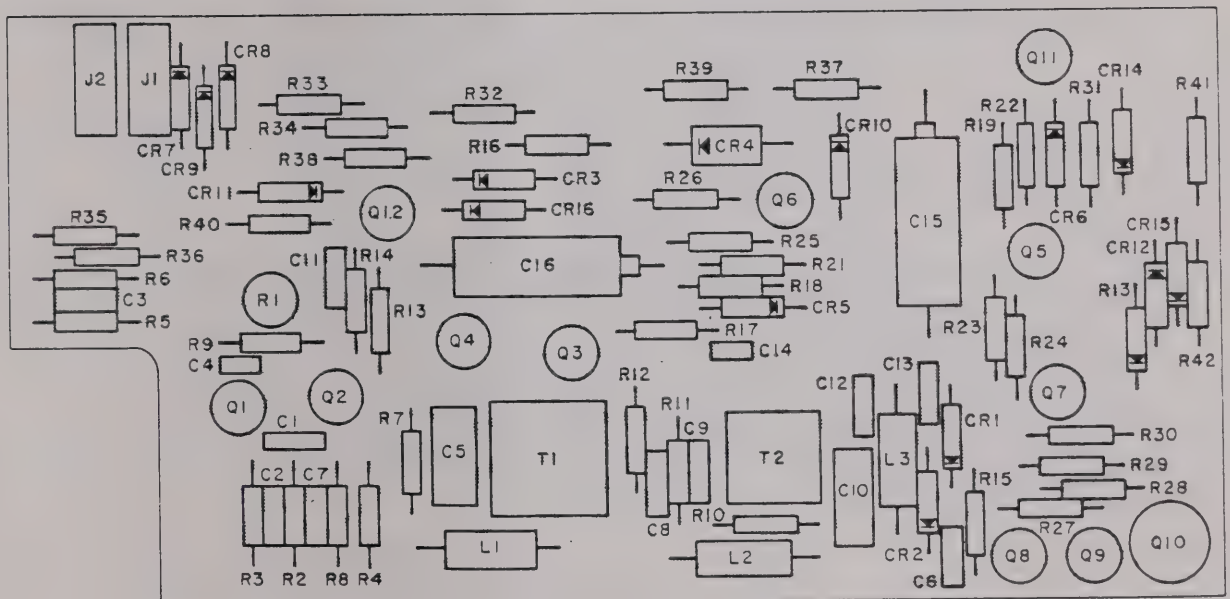


Wire Side

Figure 5-28. Second I-F Amplifier A1A2A6A1, Parts Location

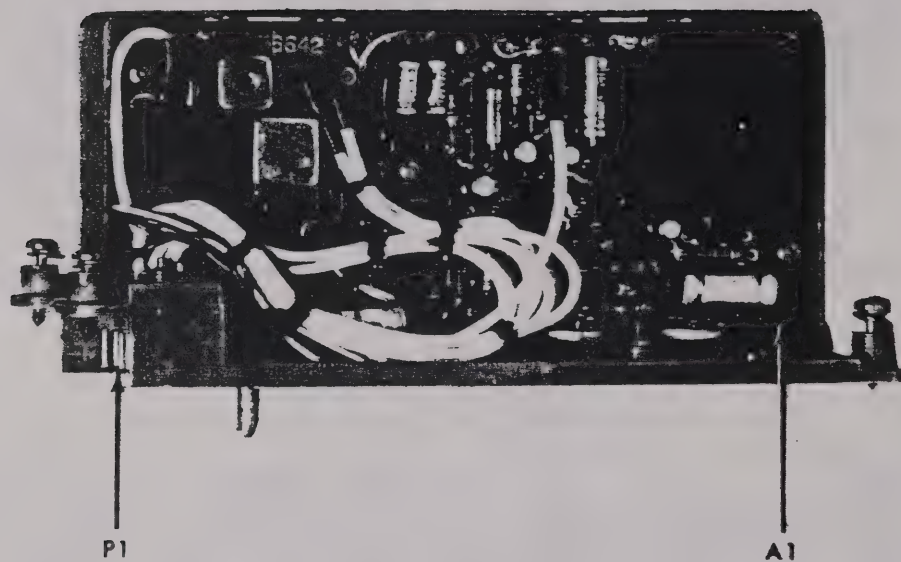


Component Side



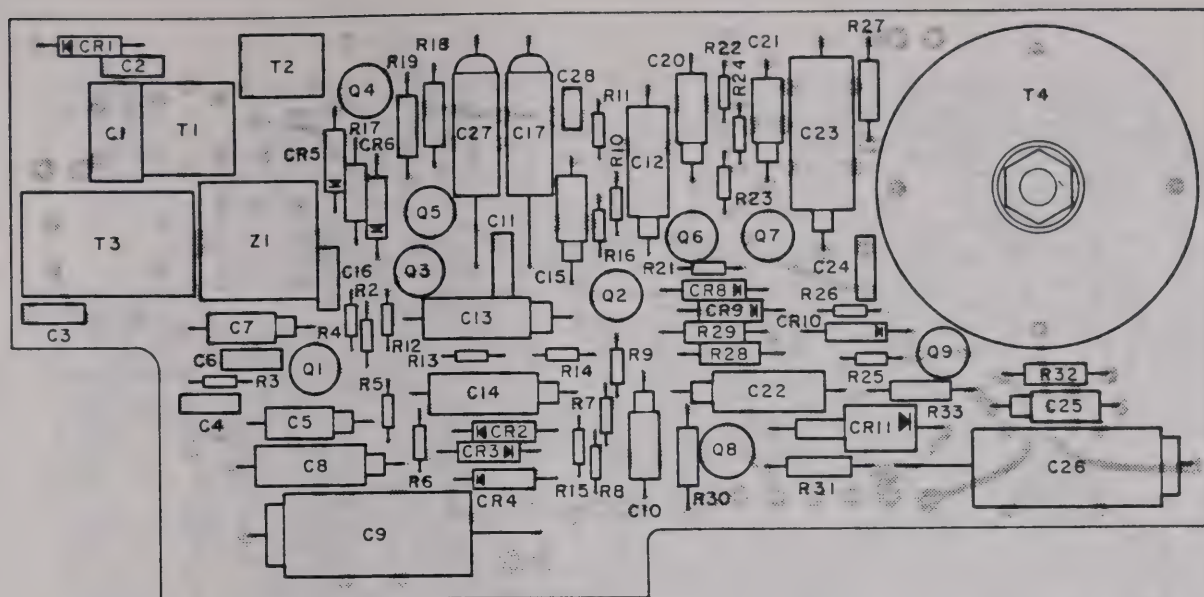
Wire Side

Figure 5-29. AGC Amplifier A1A2A6A2, Parts Location

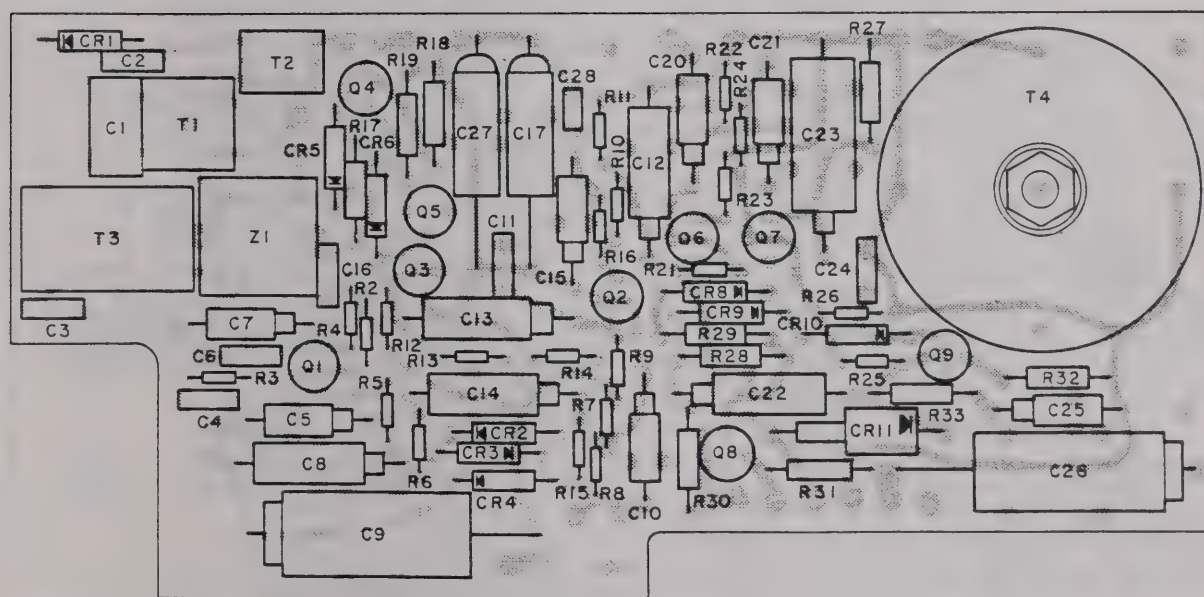


REF DES PREFIX: A1A2A7

Figure 5-30. Detector/AF Amplifier A1A2A7, Parts Location

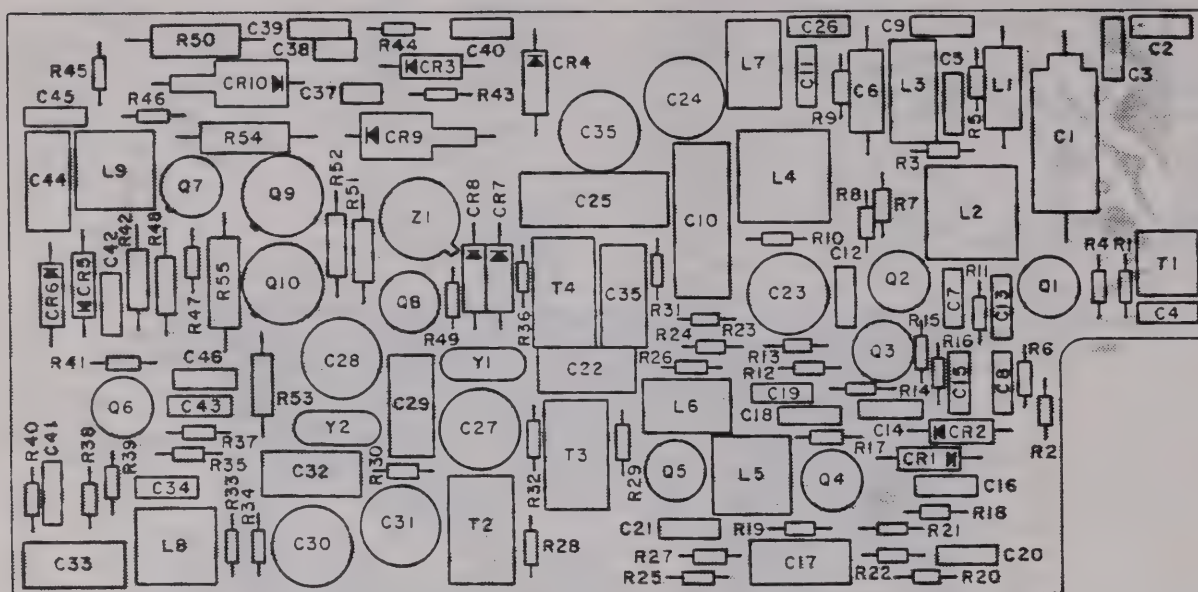


Component Side

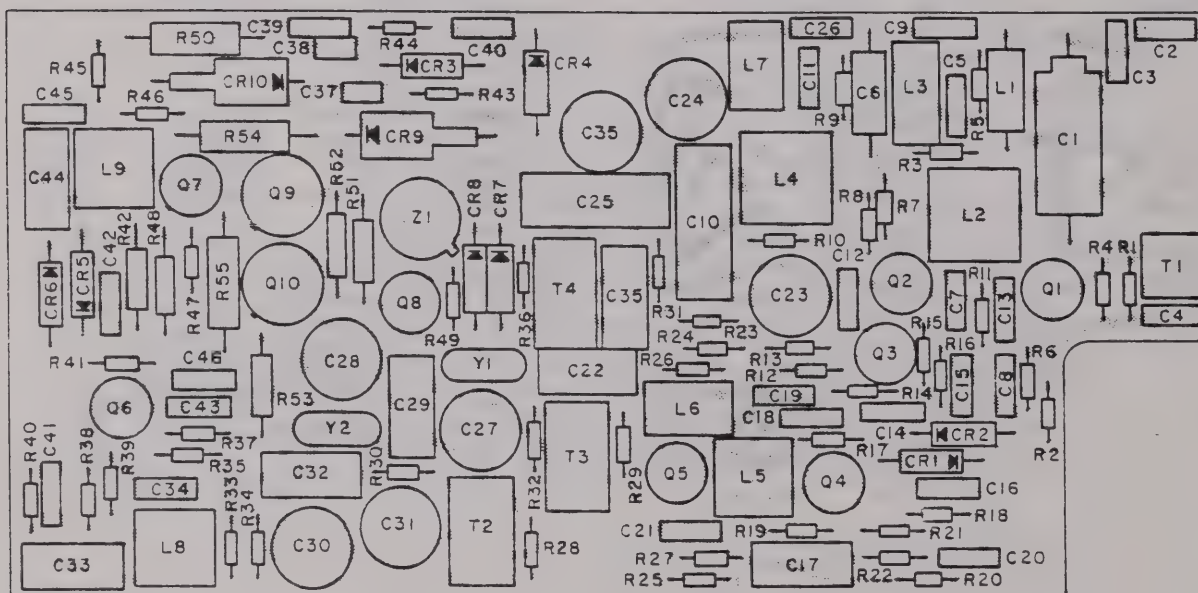


Wire Side

Figure 5-31. Detector/AF Amplifier A1A2A7, Detector/Audio Amplifier A1,
Parts Location



Component Side



Wire Side

Figure 5-32. Detector/AF Amplifier A1A2A7, FSK Converter A2, Parts Location

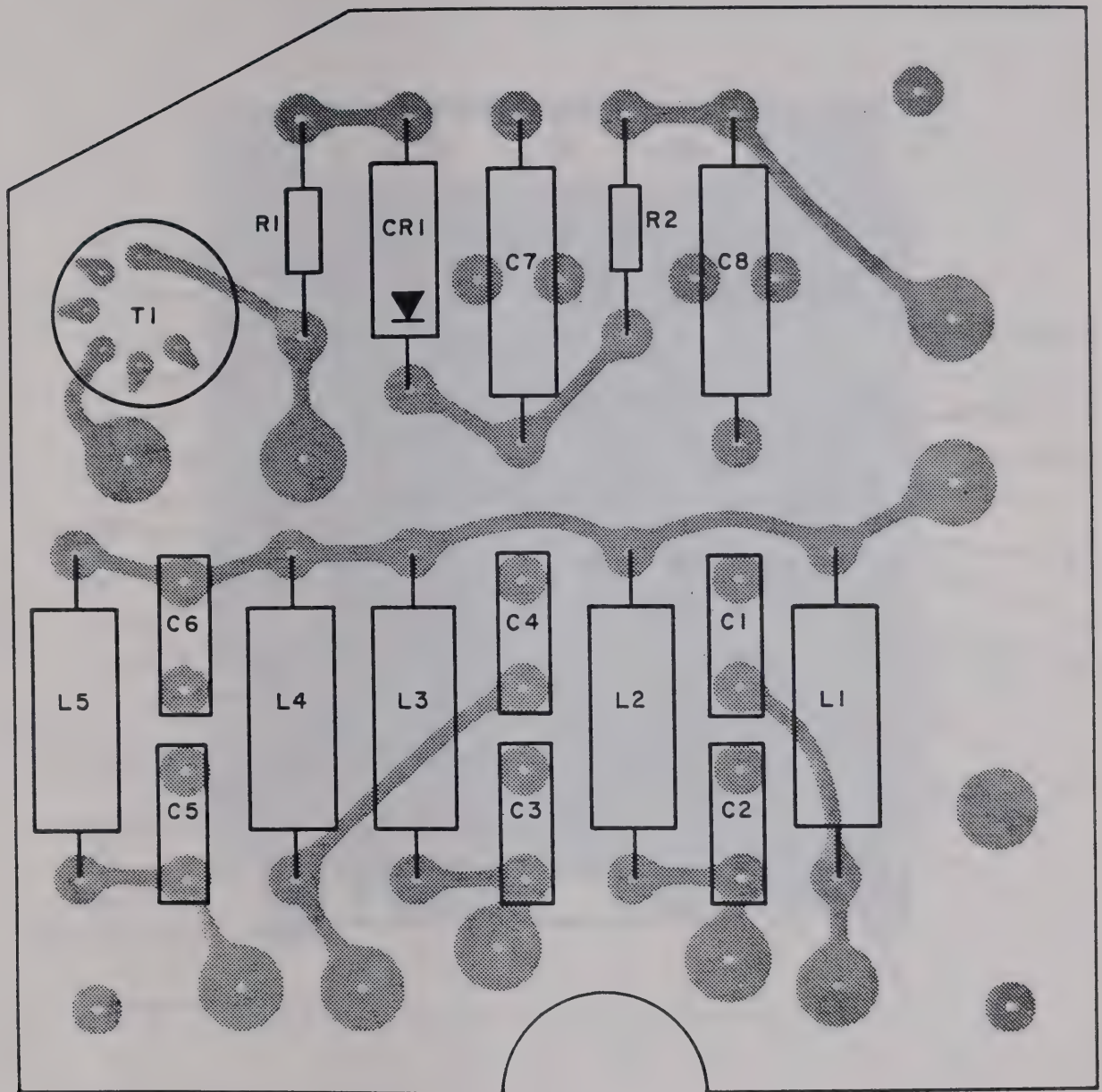


Figure 5-33. Front-Deck Supply Decoupling Board A1A2A8, Parts Location

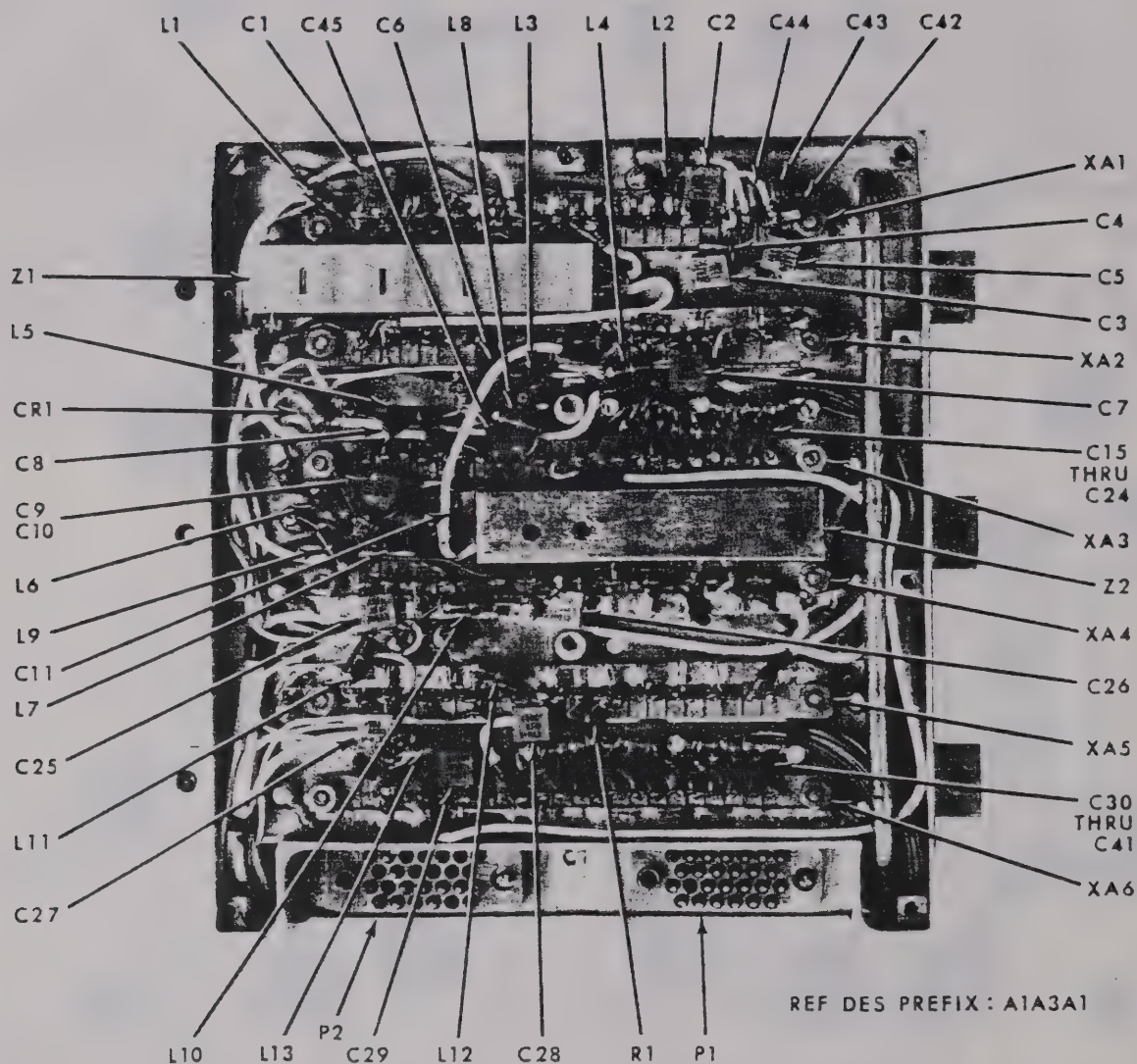
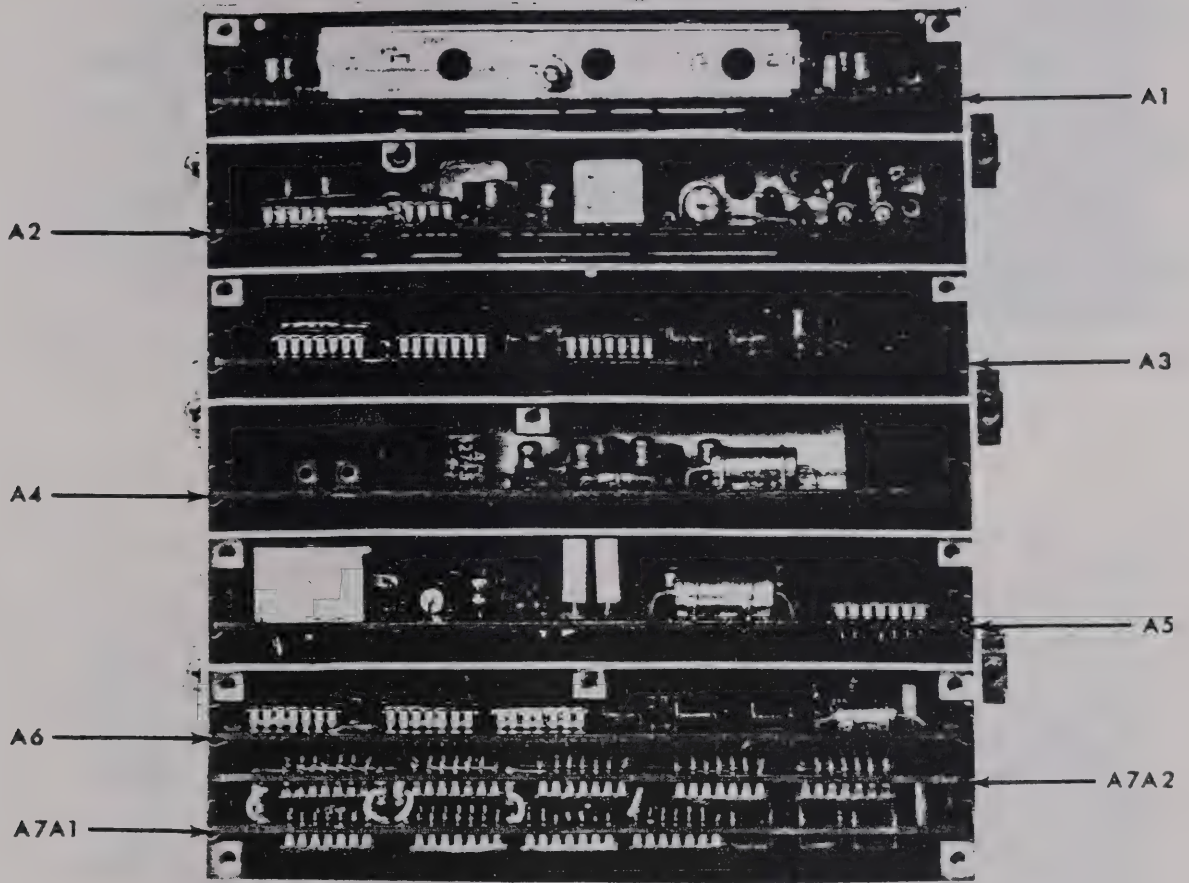
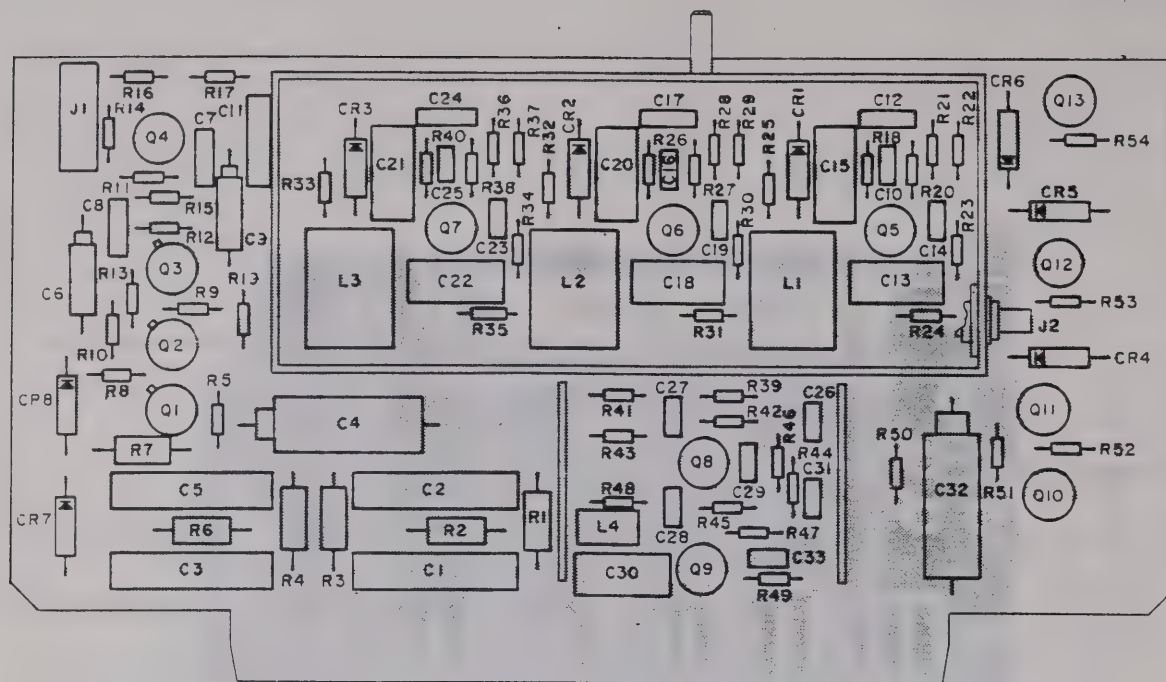


Figure 5-34. Synthesizer A1A3A1, Decoupling Components Location

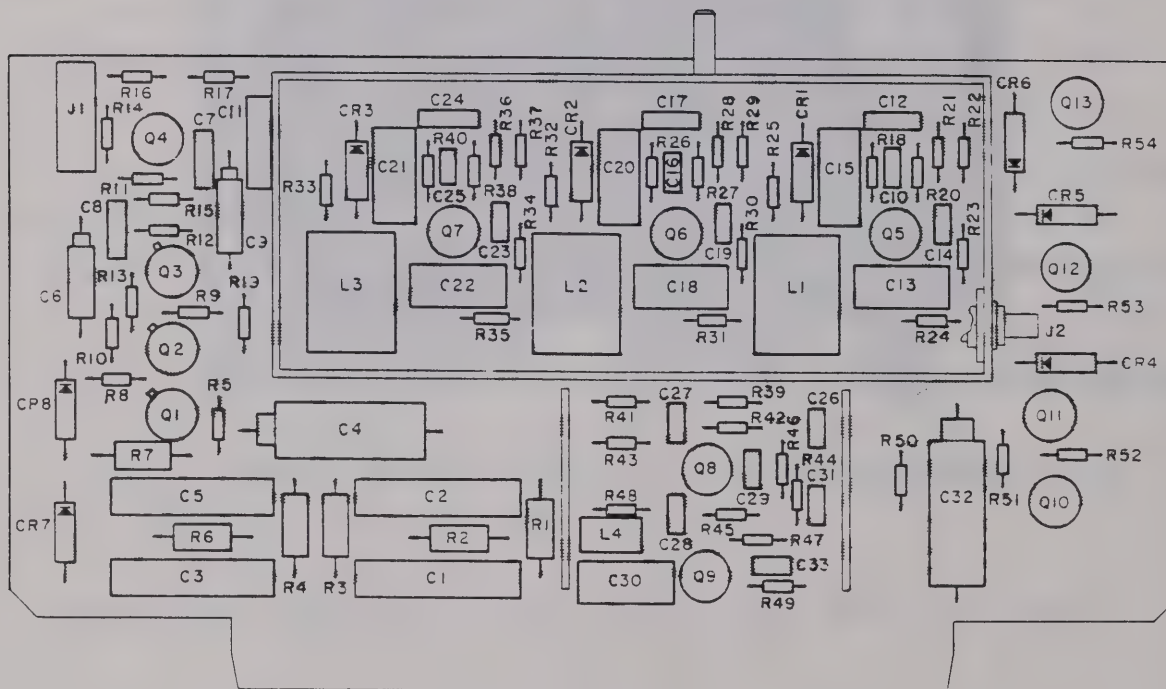


REF DES PREFIX: A1A3A1

Figure 5-35. Synthesizer A1A3A1, Module Location

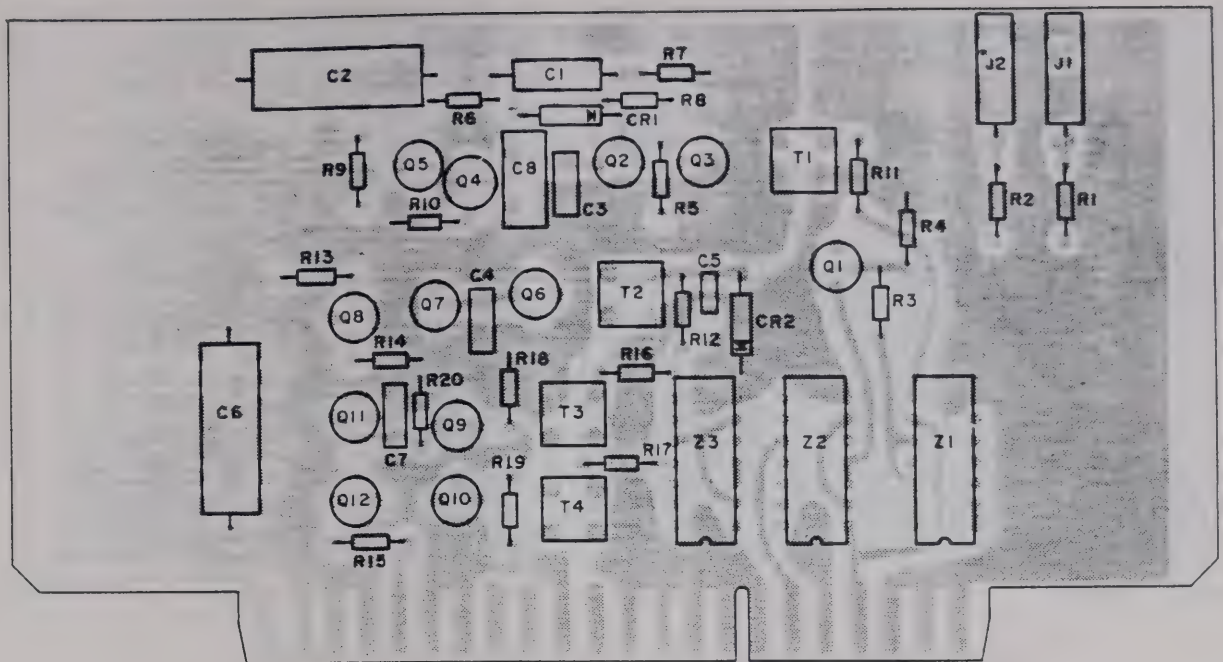


Component Side

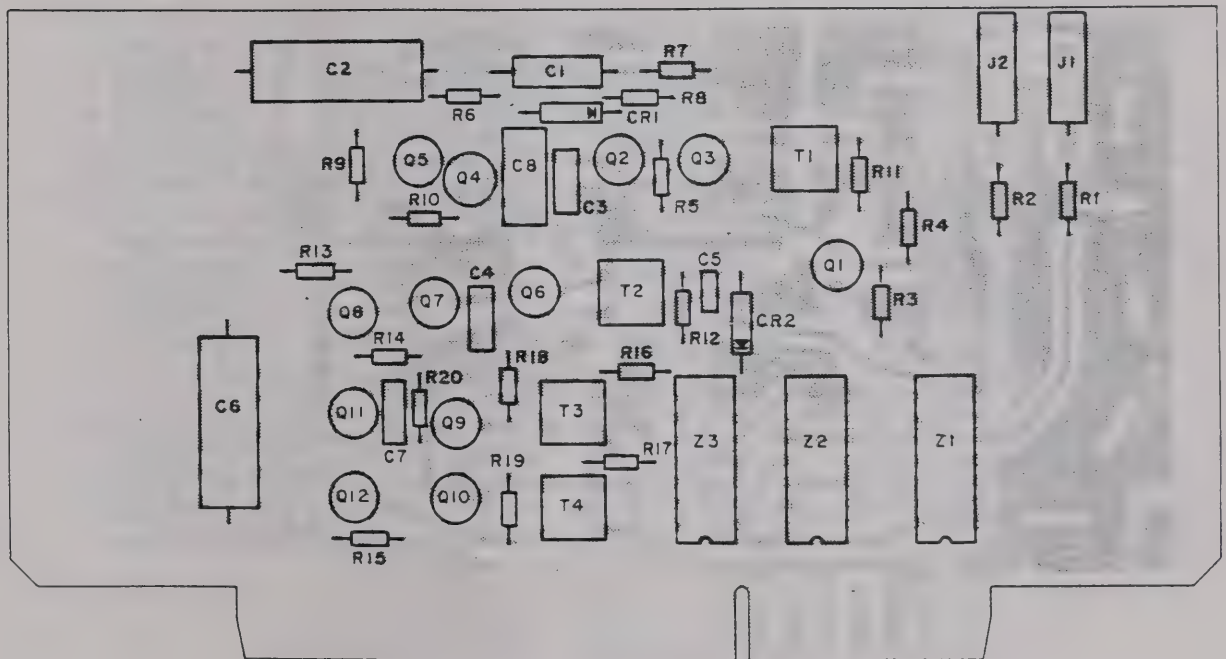


Wire Side

Figure 5-36. RF #1(A) AlA3AlAl, Parts Location

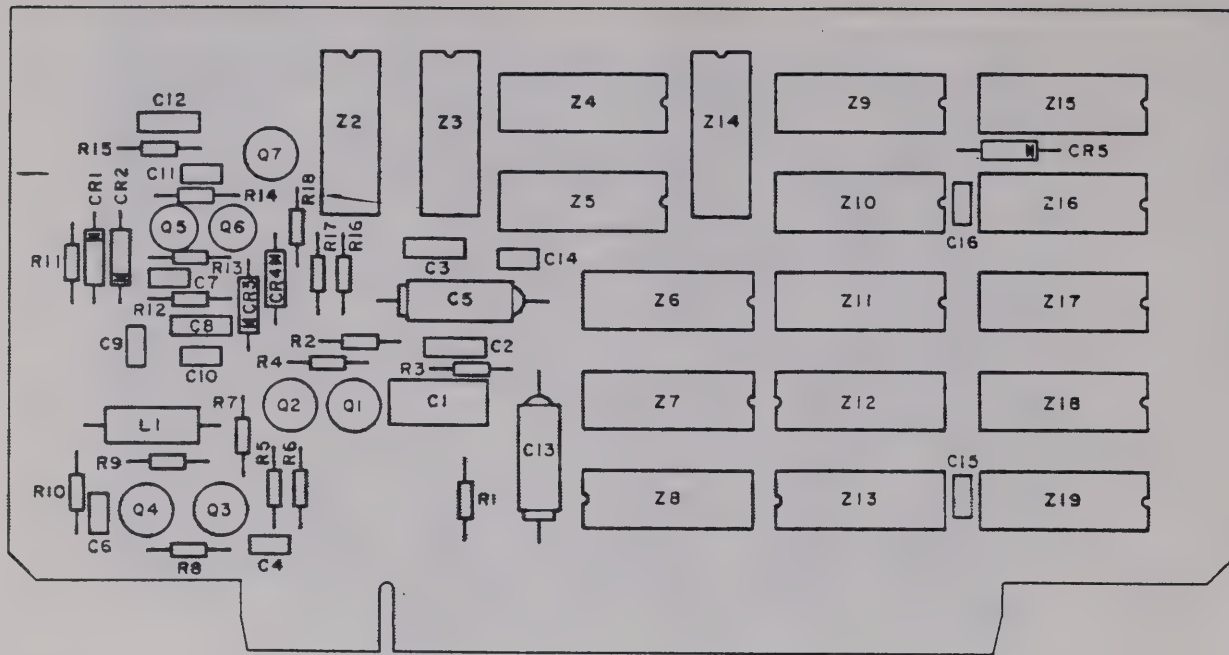


Component Side

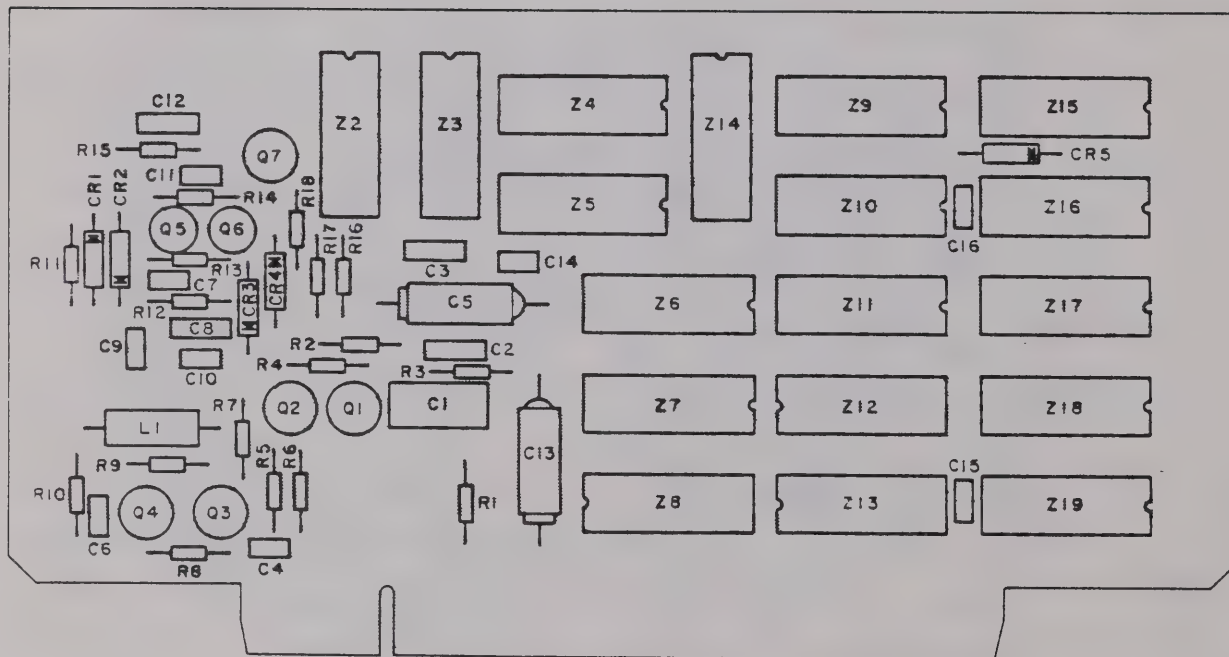


Wire Side

Figure 5-37. RF #1(B) AlA3AlA4, Parts Location

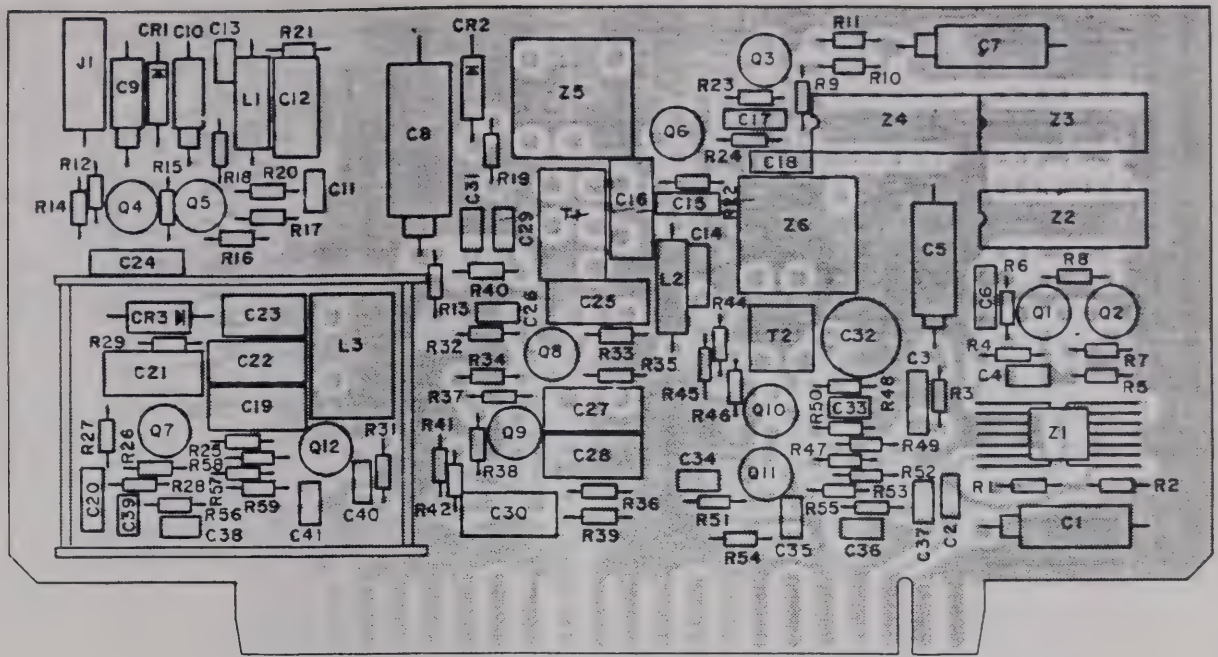


Component Side

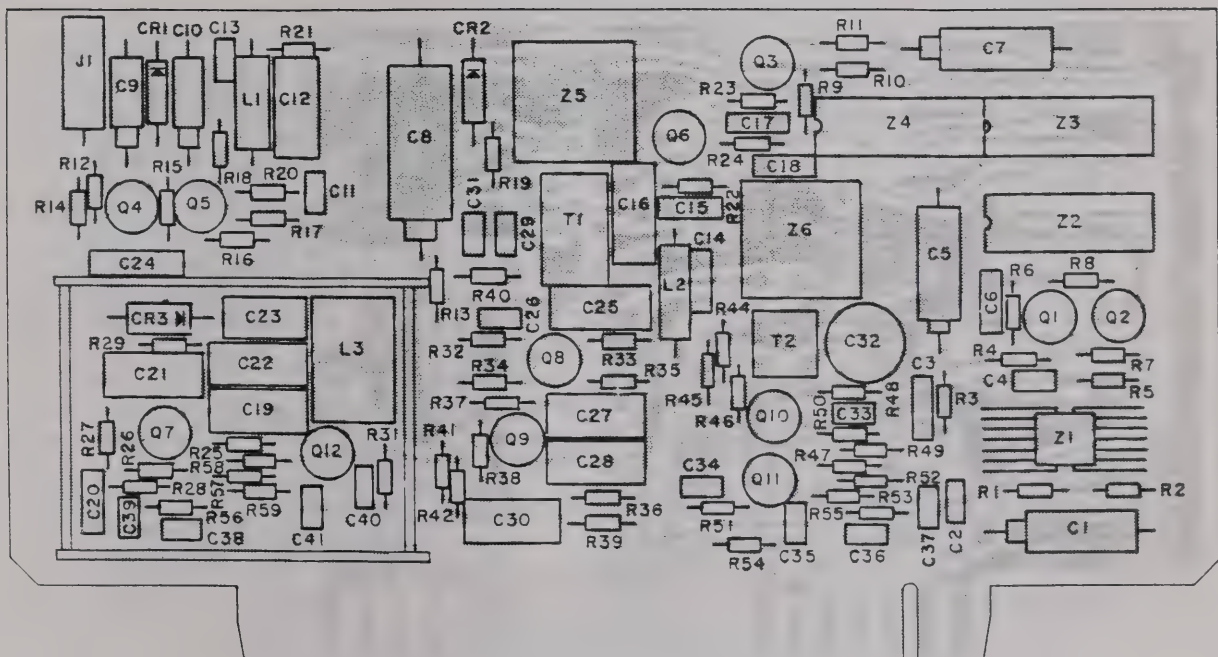


Wire Side

Figure 5-38. Digital #2 AlA3AlA3, Parts Location

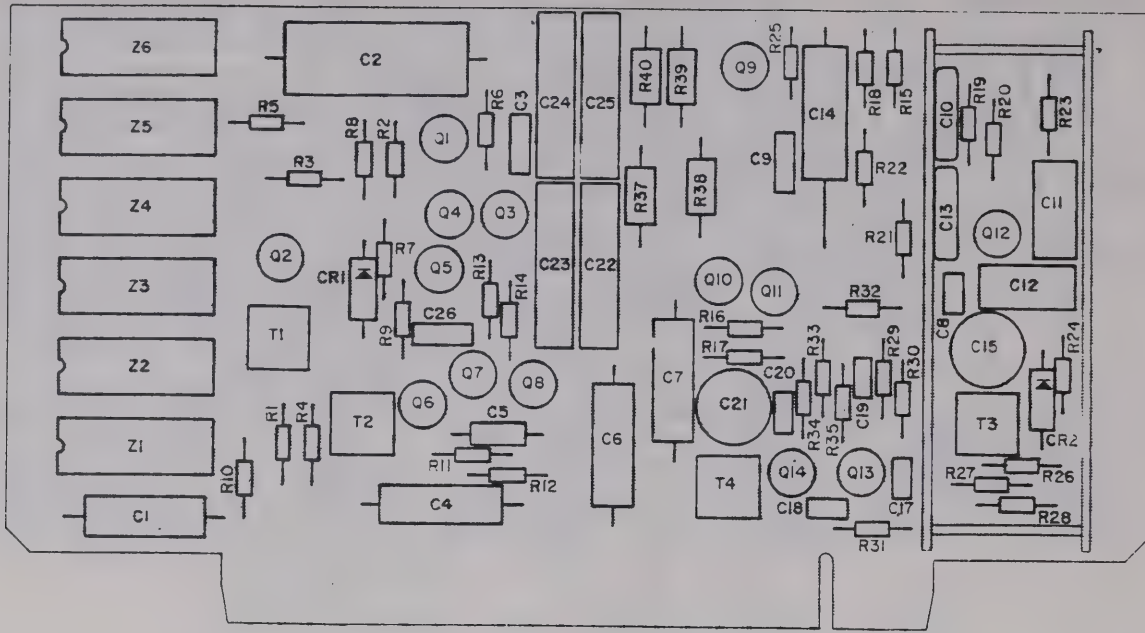


Component Side

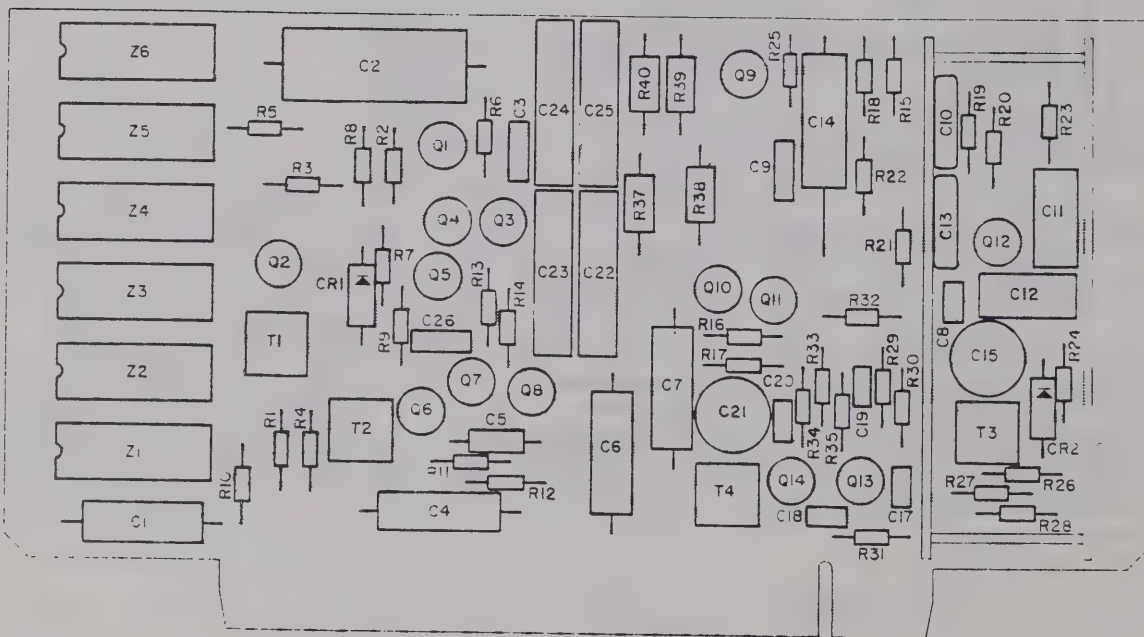


Wire Side

Figure 5-39. RF #3 A1A3A1A2, Parts Location

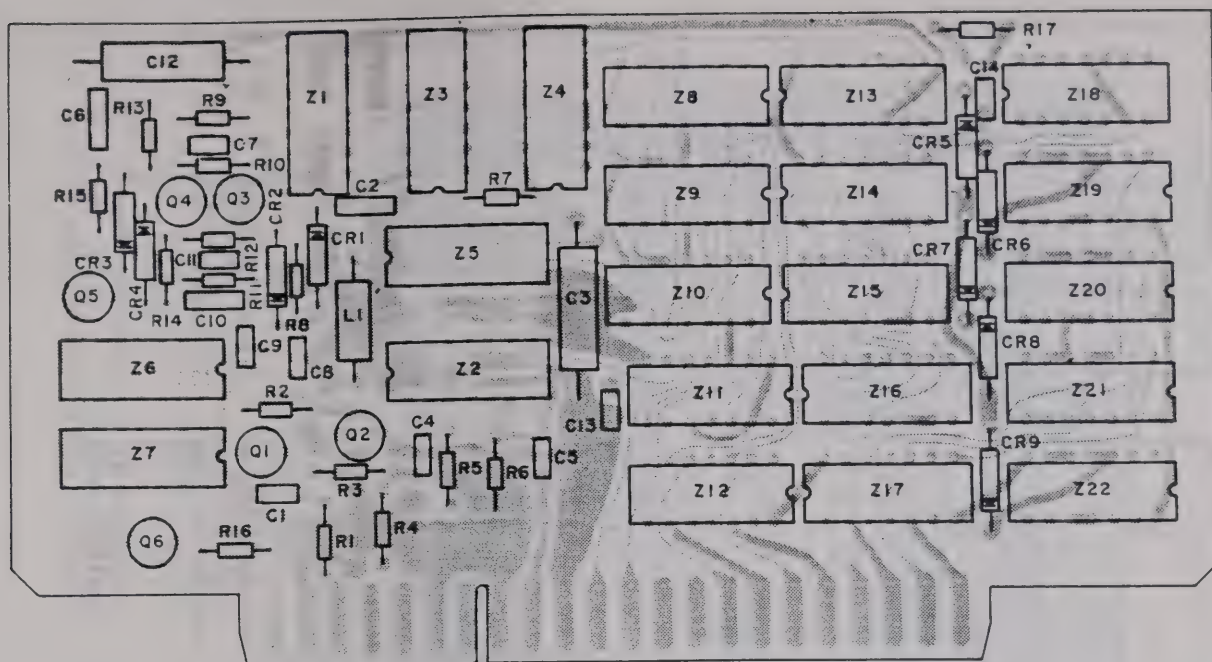


Component Side

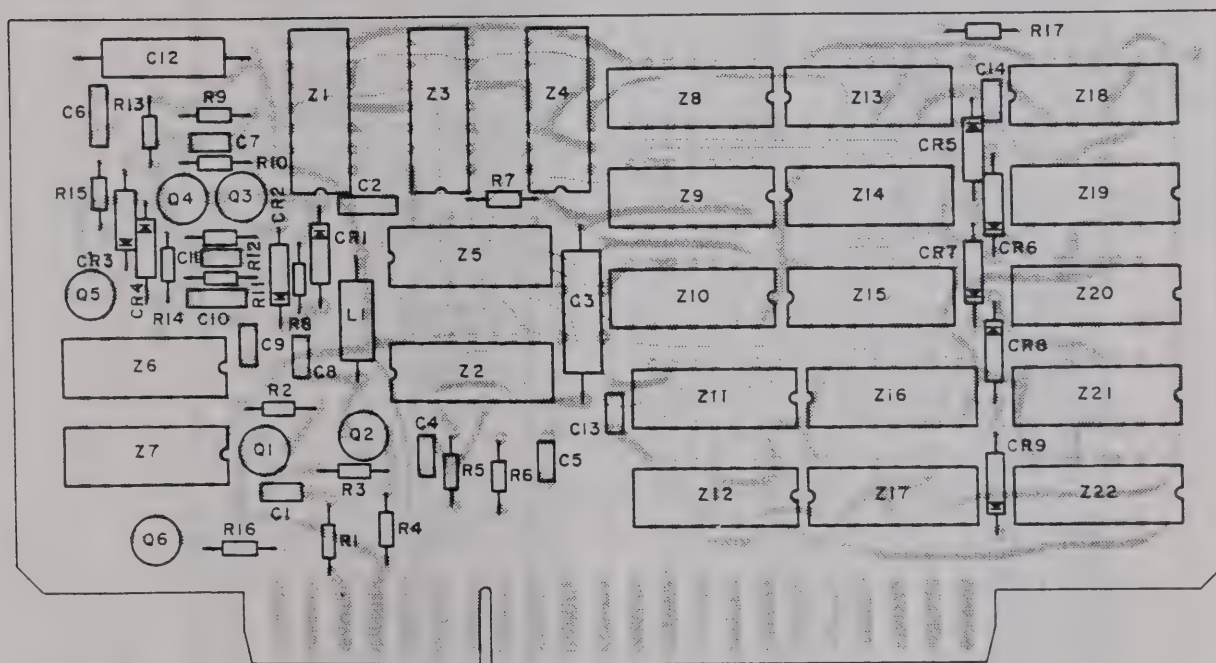


Wire Side

Figure 5-40. RF #2 A1A3A1A5, Parts Location



Component Side



Wire Side

Figure 5-41. Digital #3 A1A3A1A6, Parts Location

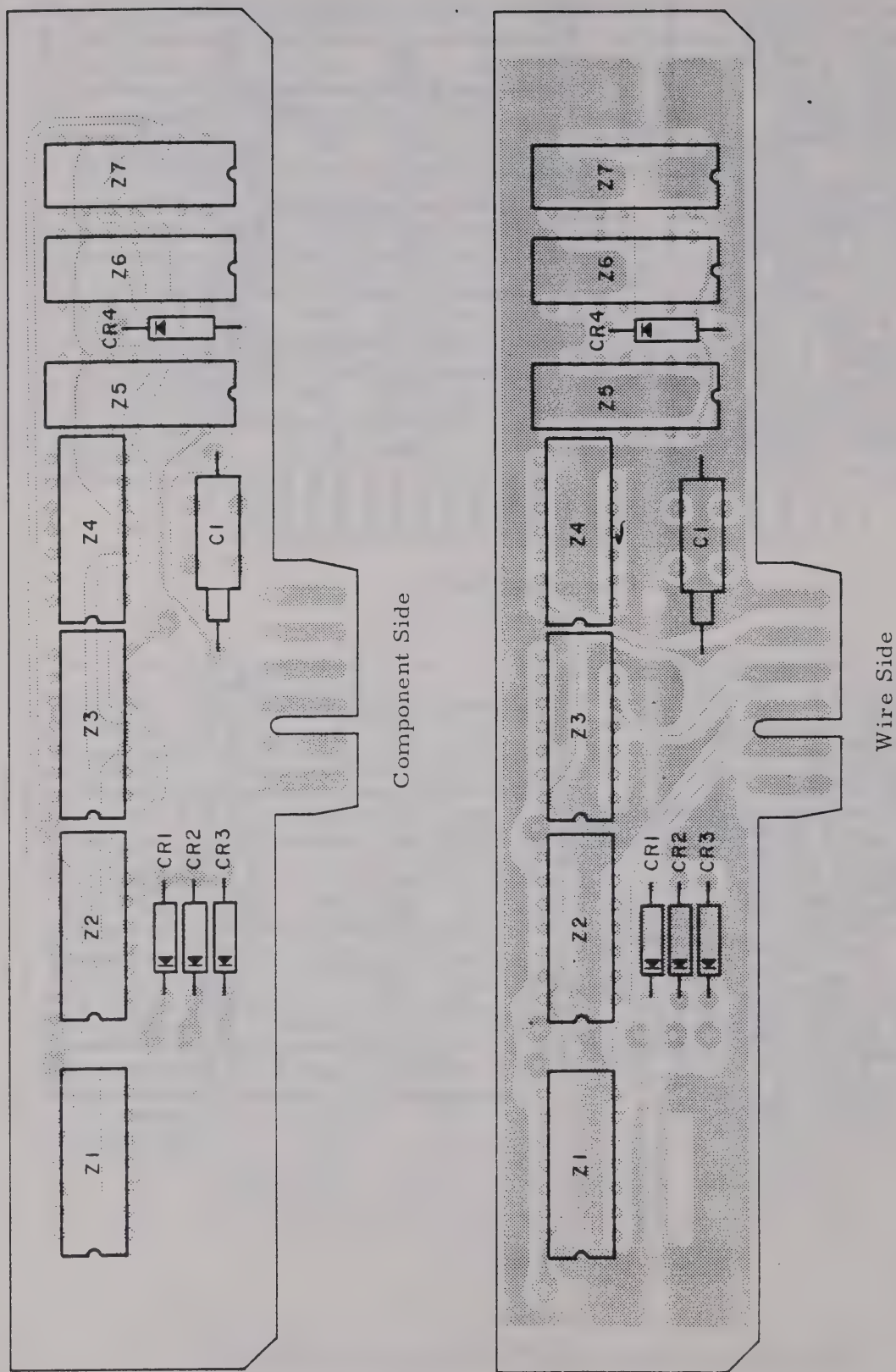
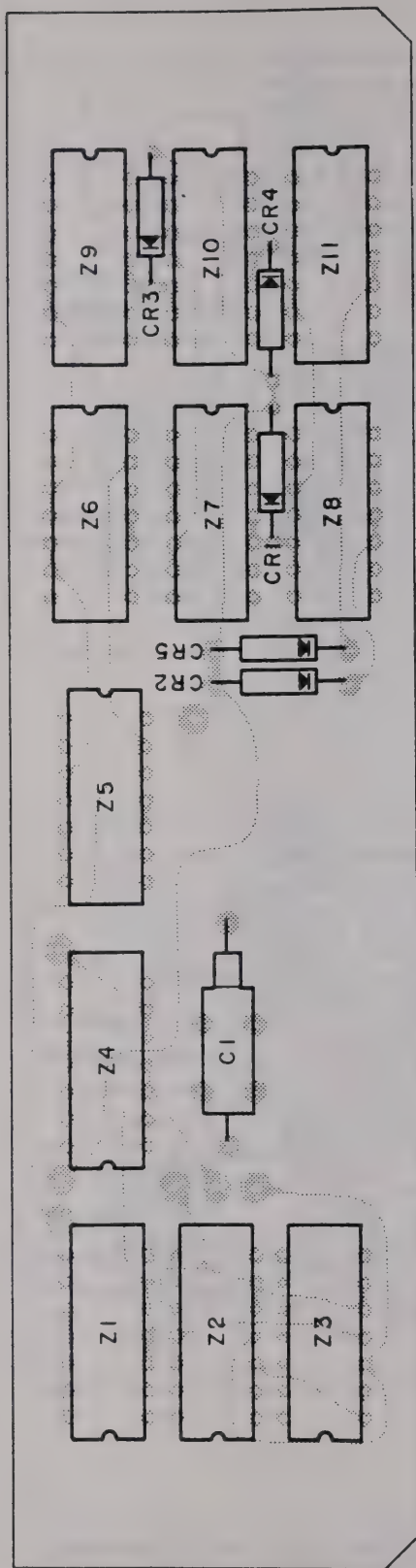
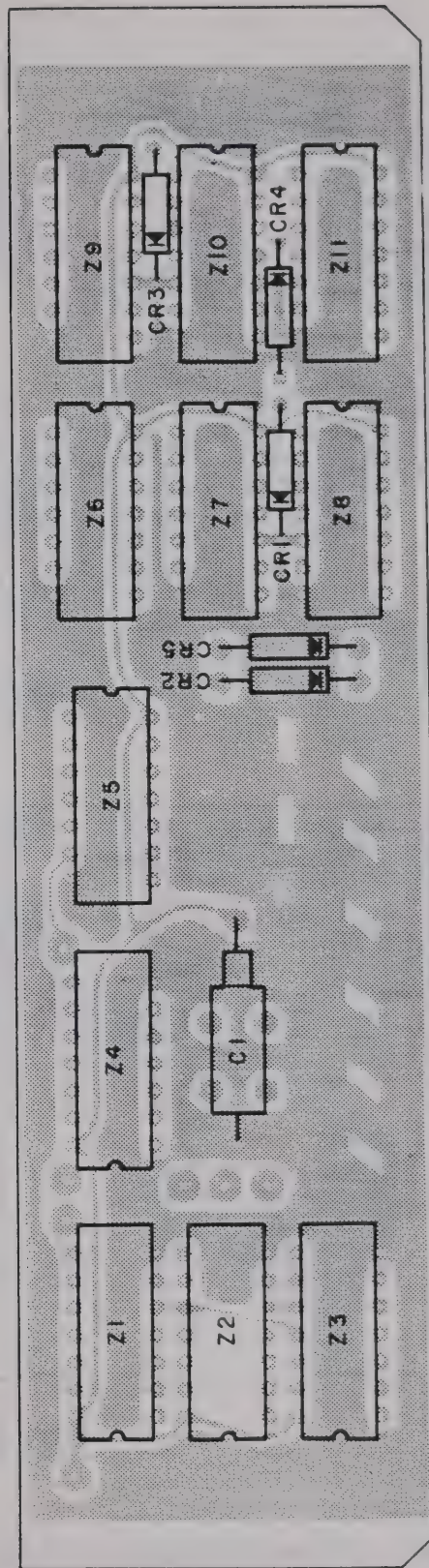


Figure 5-42. Digital #1(A) ALA3A1A7A1, Parts Location

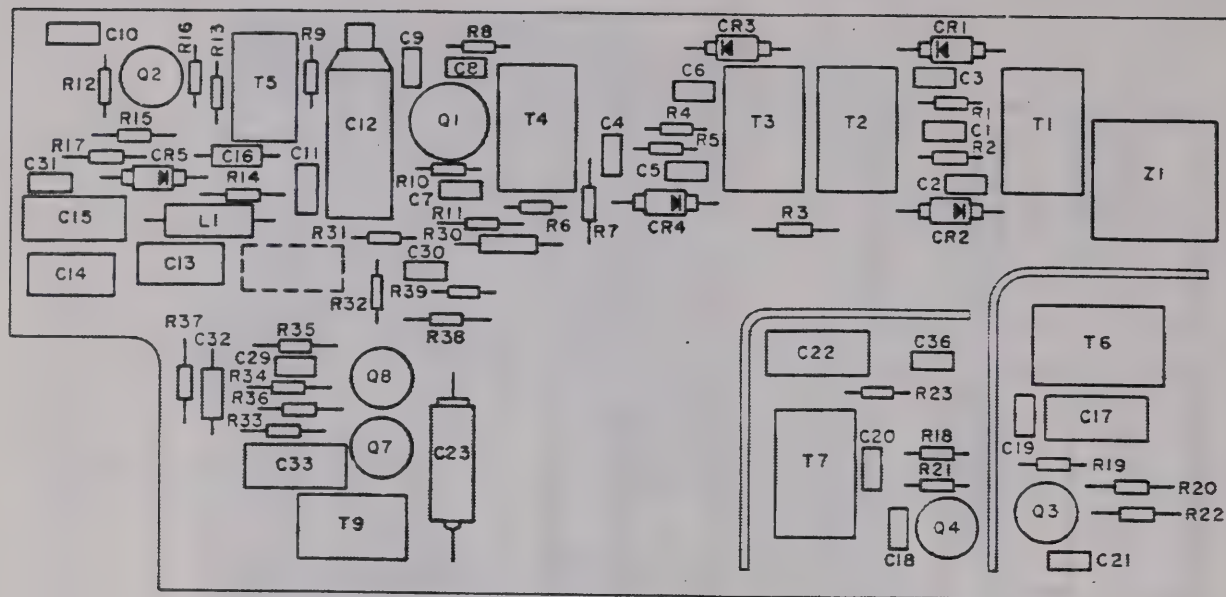


Component Side

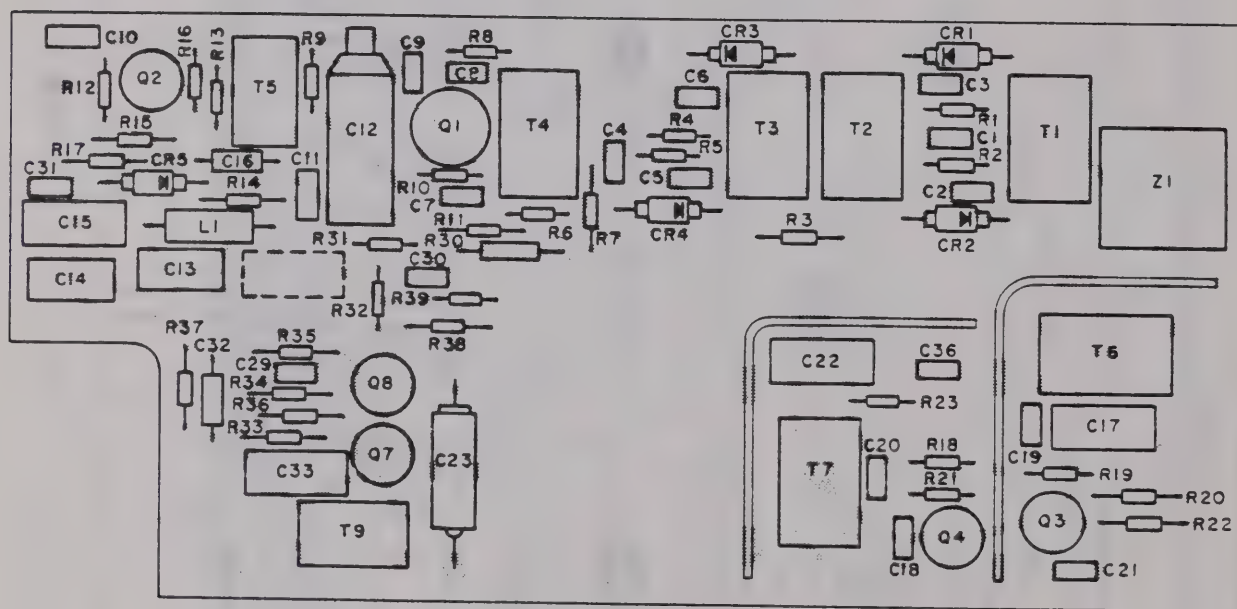


Wire Side

Figure 5-43. Digital #1(B) A1A3A1A7A2, Parts Location

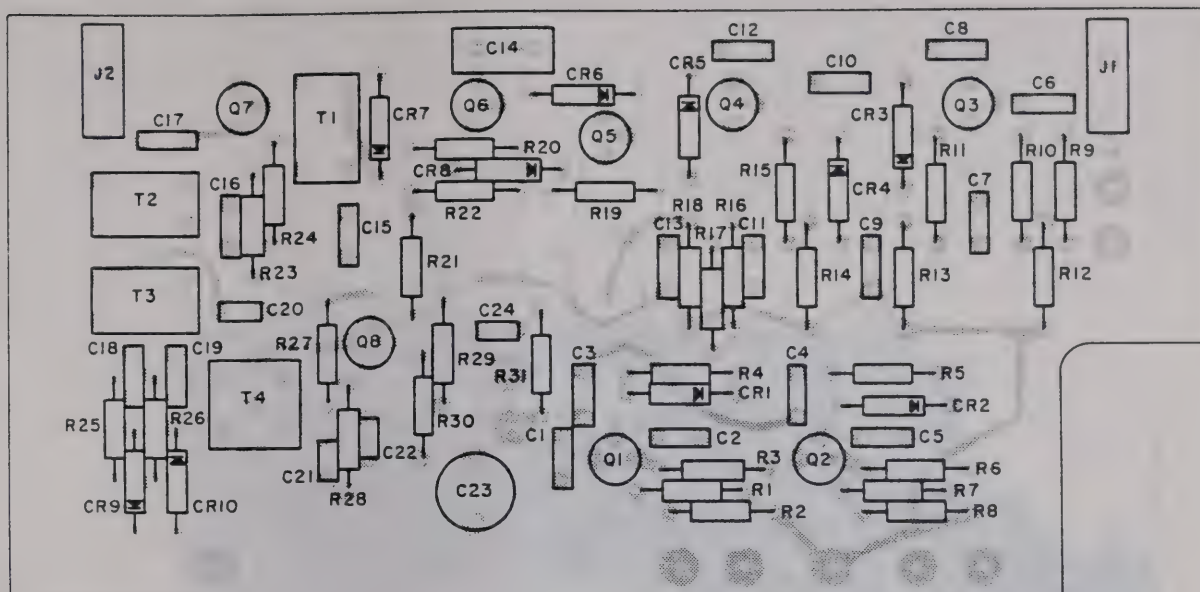


Component Side

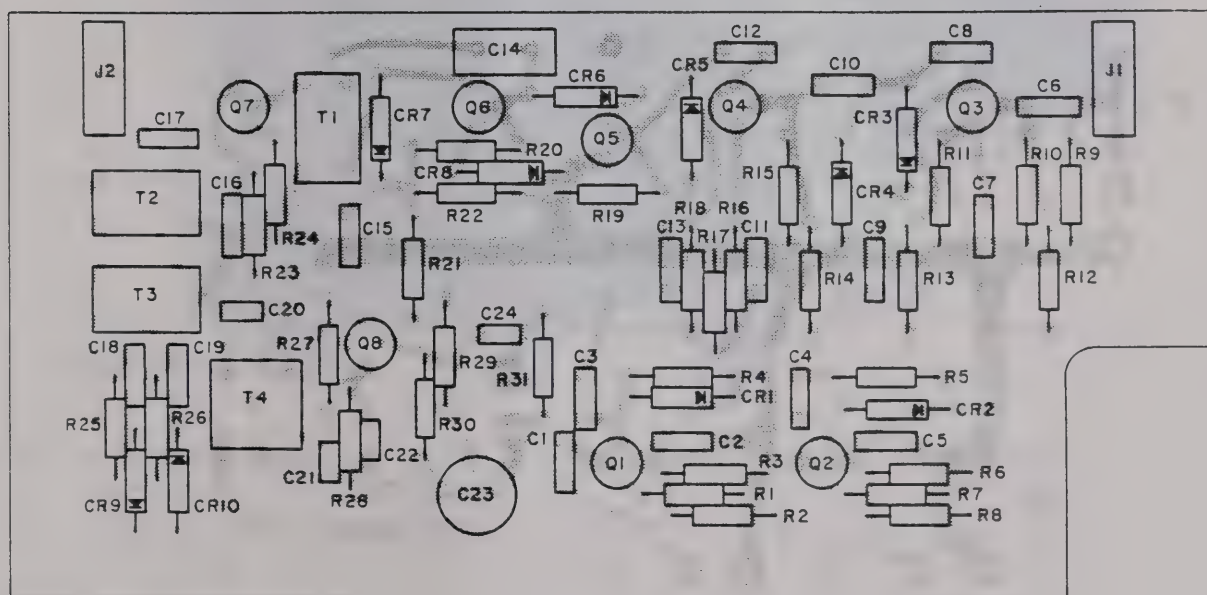


Wire Side

Figure 5-44. Mixer/Multiplier A1A3A2, X4 Multiplier A1, Parts Location



Component Side



Wire Side

Figure 5-45. Mixer/Multiplier A1A3A2, X10 Multiplier A2, Parts Location

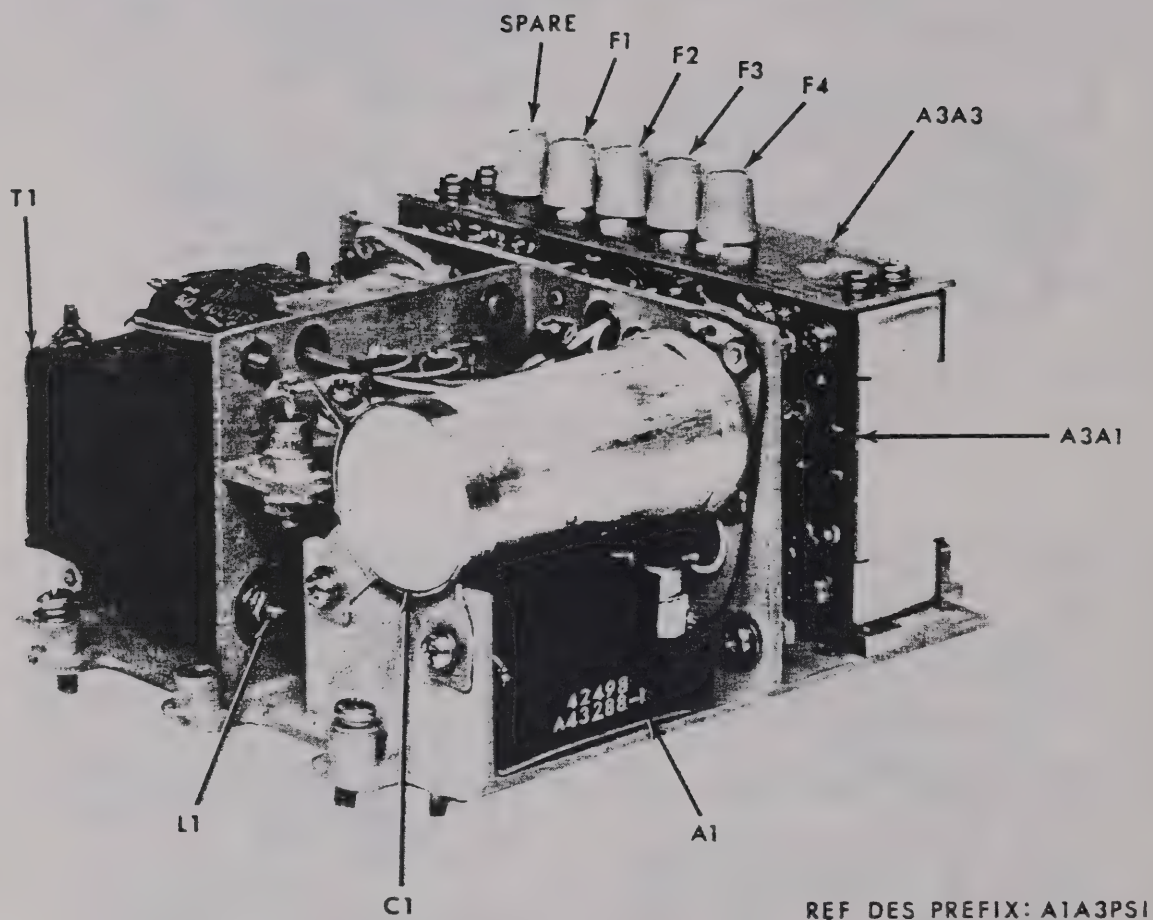
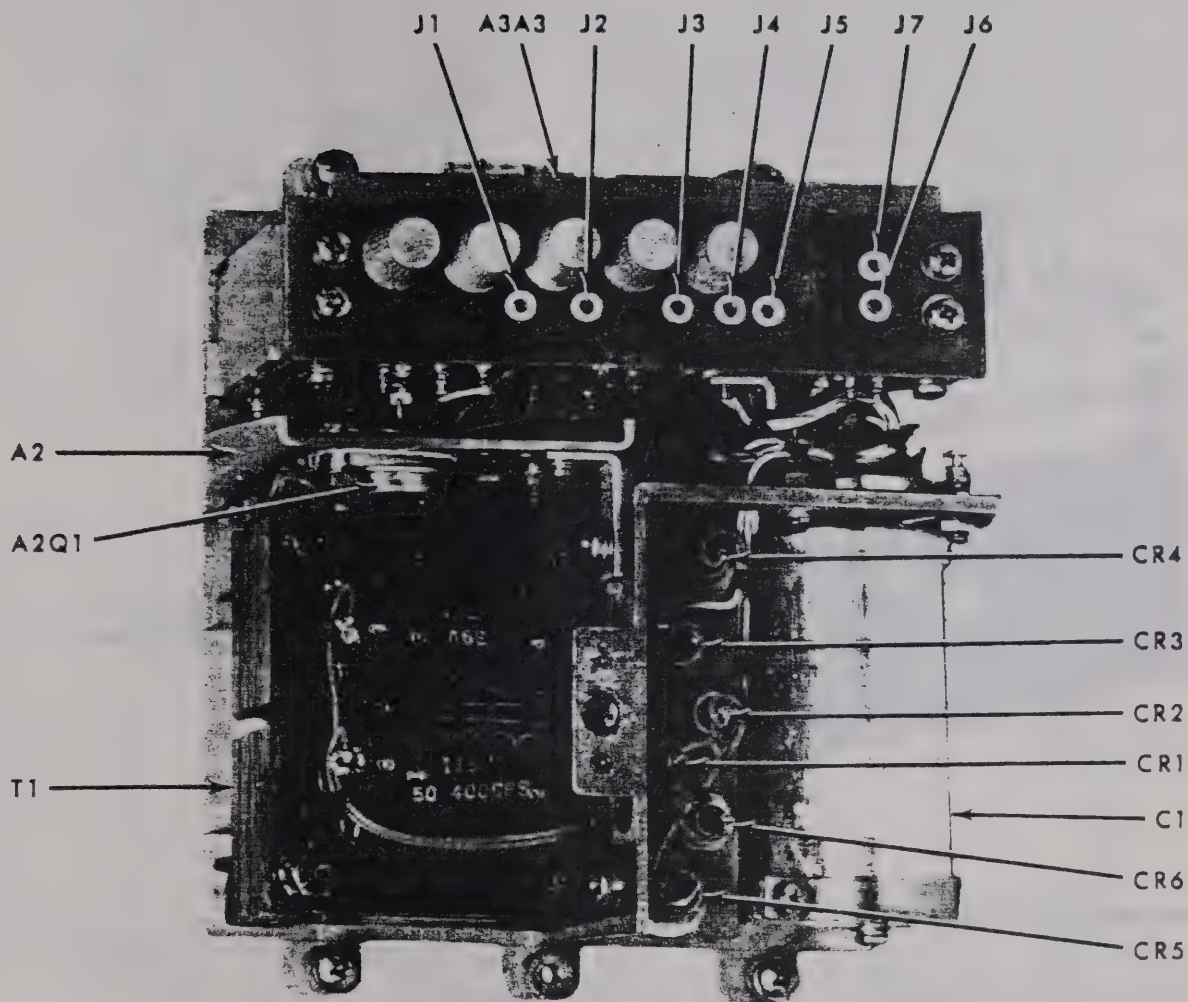
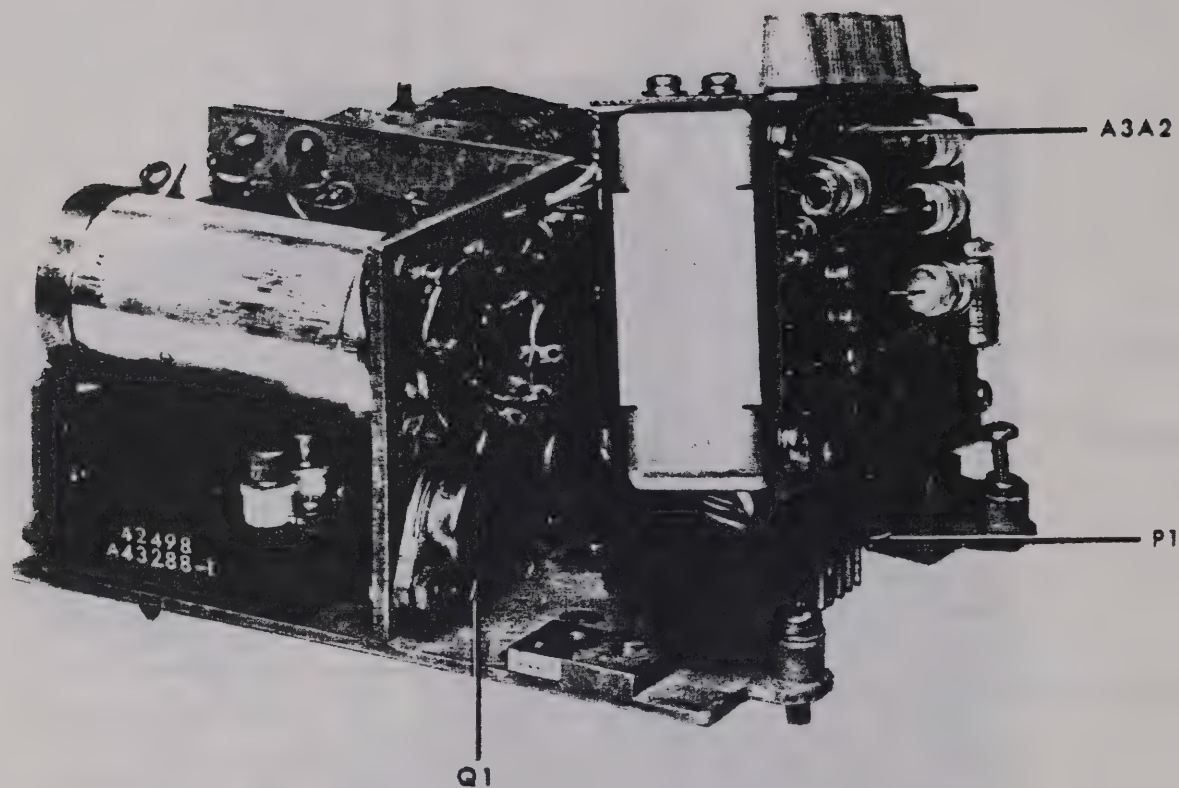


Figure 5-46. Power Supply A1A3PS1, Parts Location (Sheet 1)



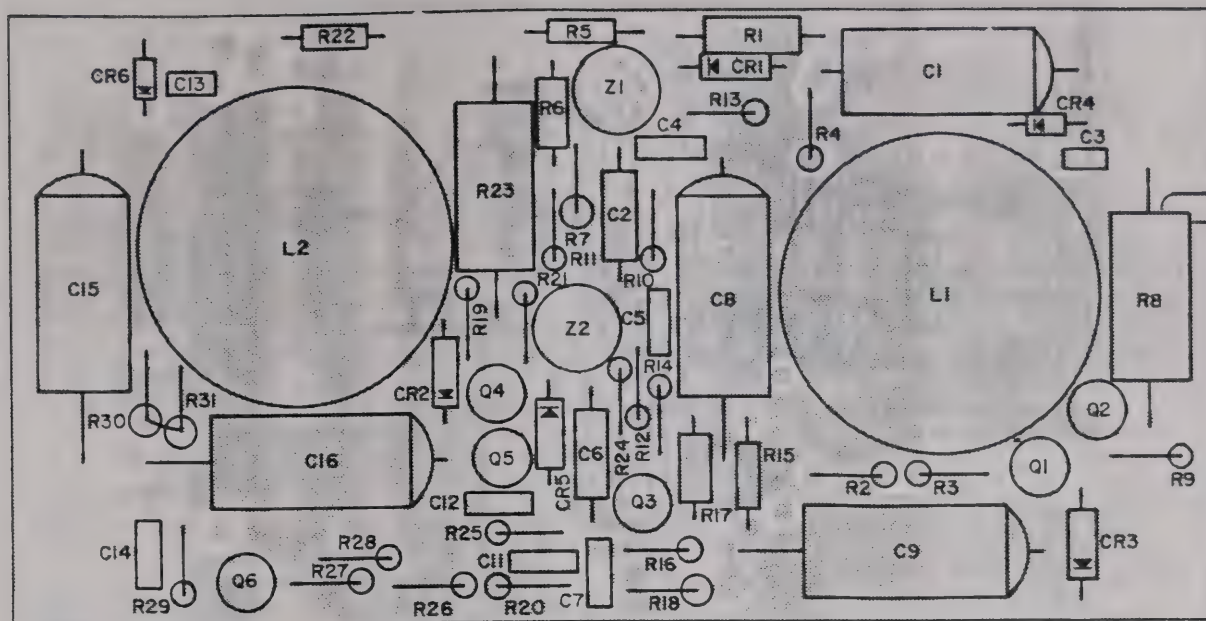
REF DES PREFIX: A1A3PS1

Figure 5-47. Power Supply A1A3PS1, Parts Location (Sheet 2)

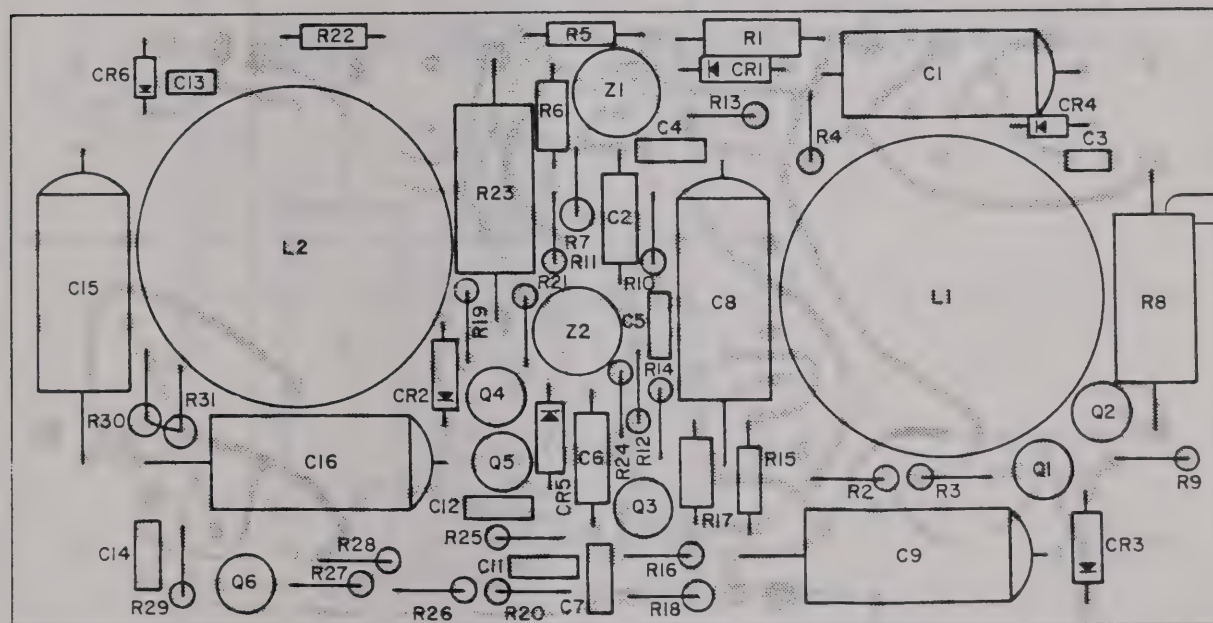


REF DES PREFIX: A1A3PS1

Figure 5-48. Power Supply A1A3PS1, Parts Location (Sheet 3)



Component Side



Wire Side

Figure 5-49. Power Supply A1A3PS1; +5 Volt and +18 Volt Regulators (A3A1),
Parts Location

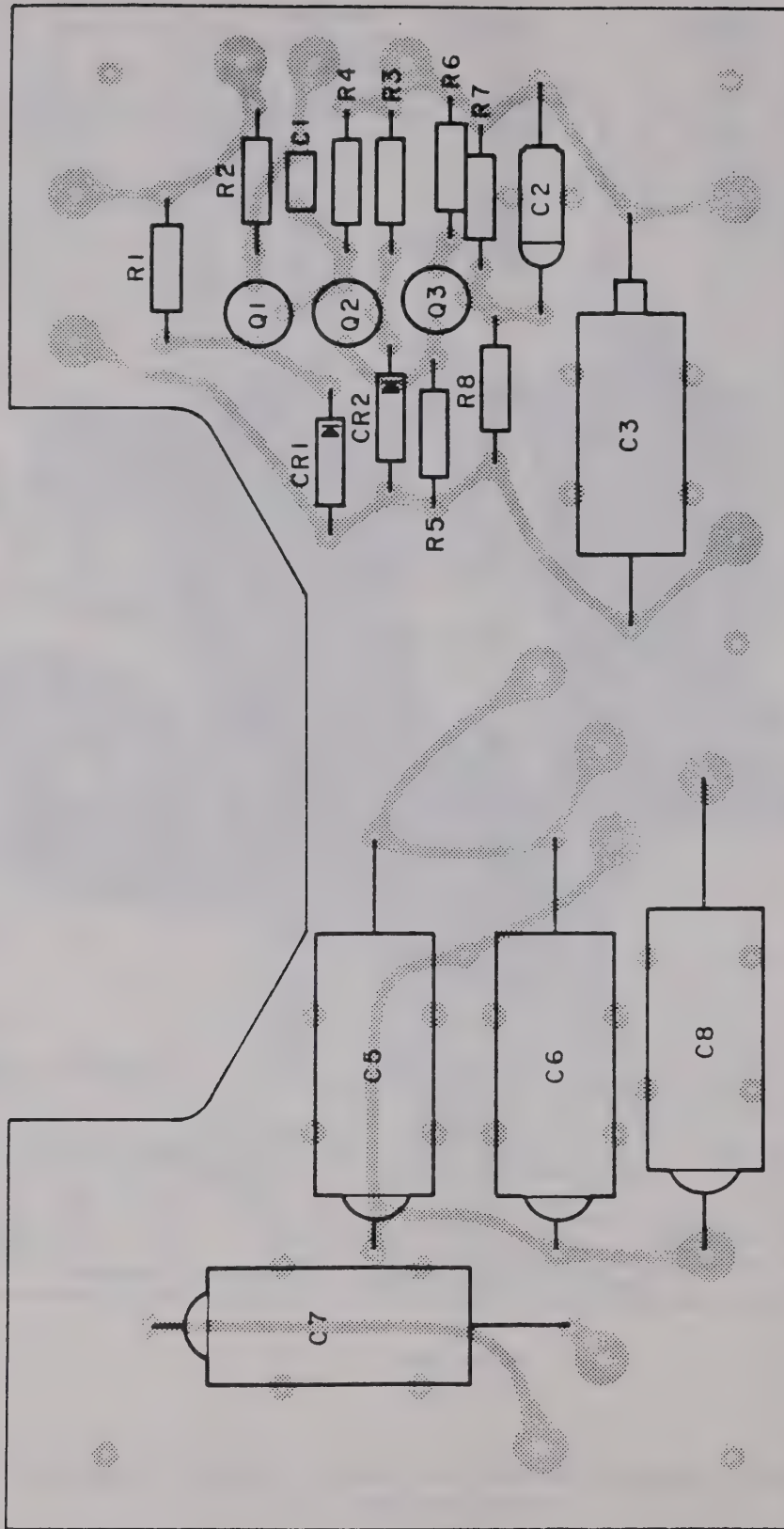


Figure 5-50. Power Supply A1A3PS1; +15 Volt Regulator (A3A2), Parts Location

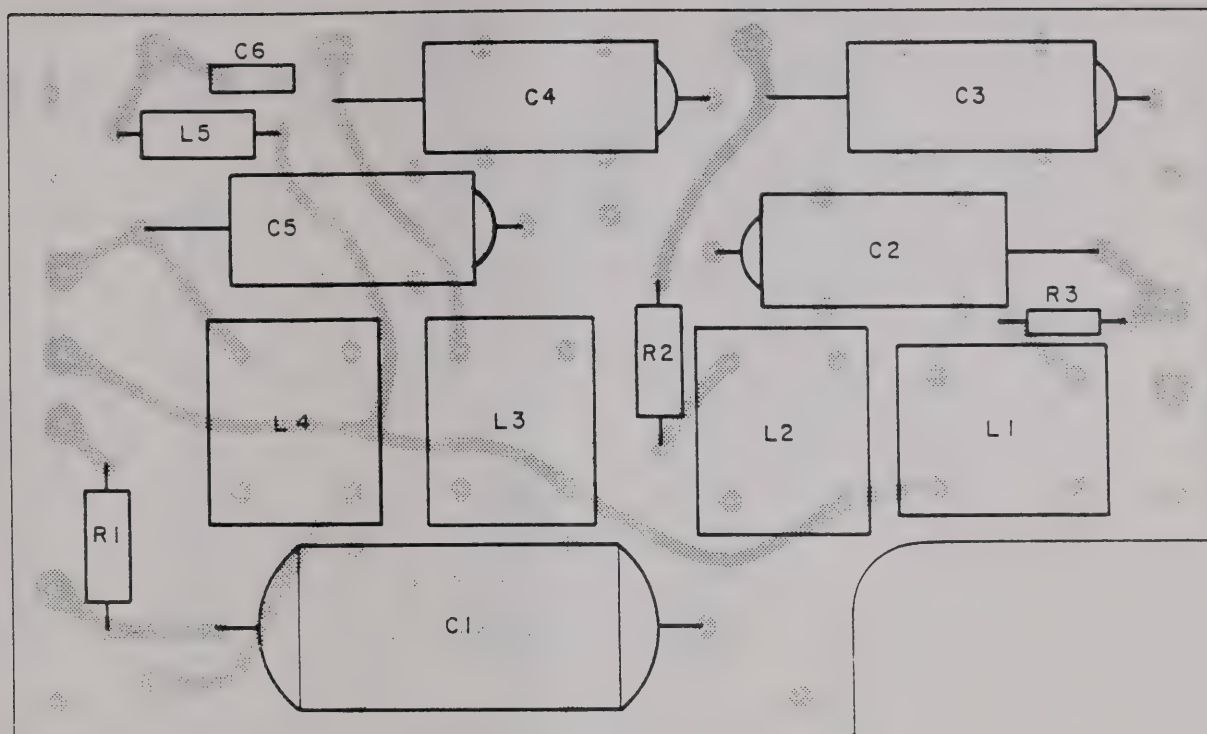


Figure 5-51. Rear-Deck Supply Decoupling Board A1A3A3, Parts Location

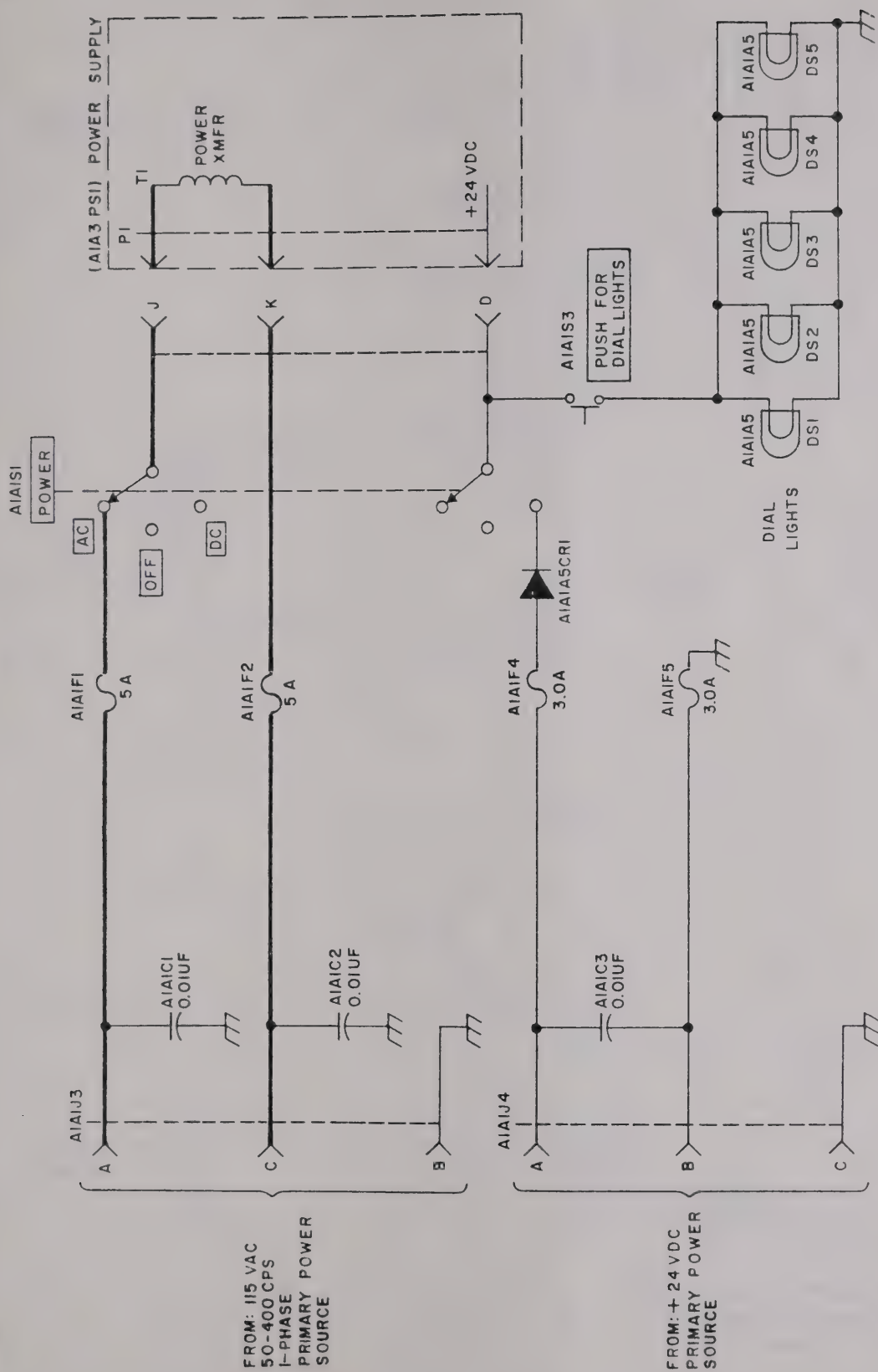


Figure 5-52. Primary Power Distribution, Schematic Diagram

FRONT DECK A1A2: SEE FIG. 5-54
REAR DECK A1A3: SEE FIG. 5-55

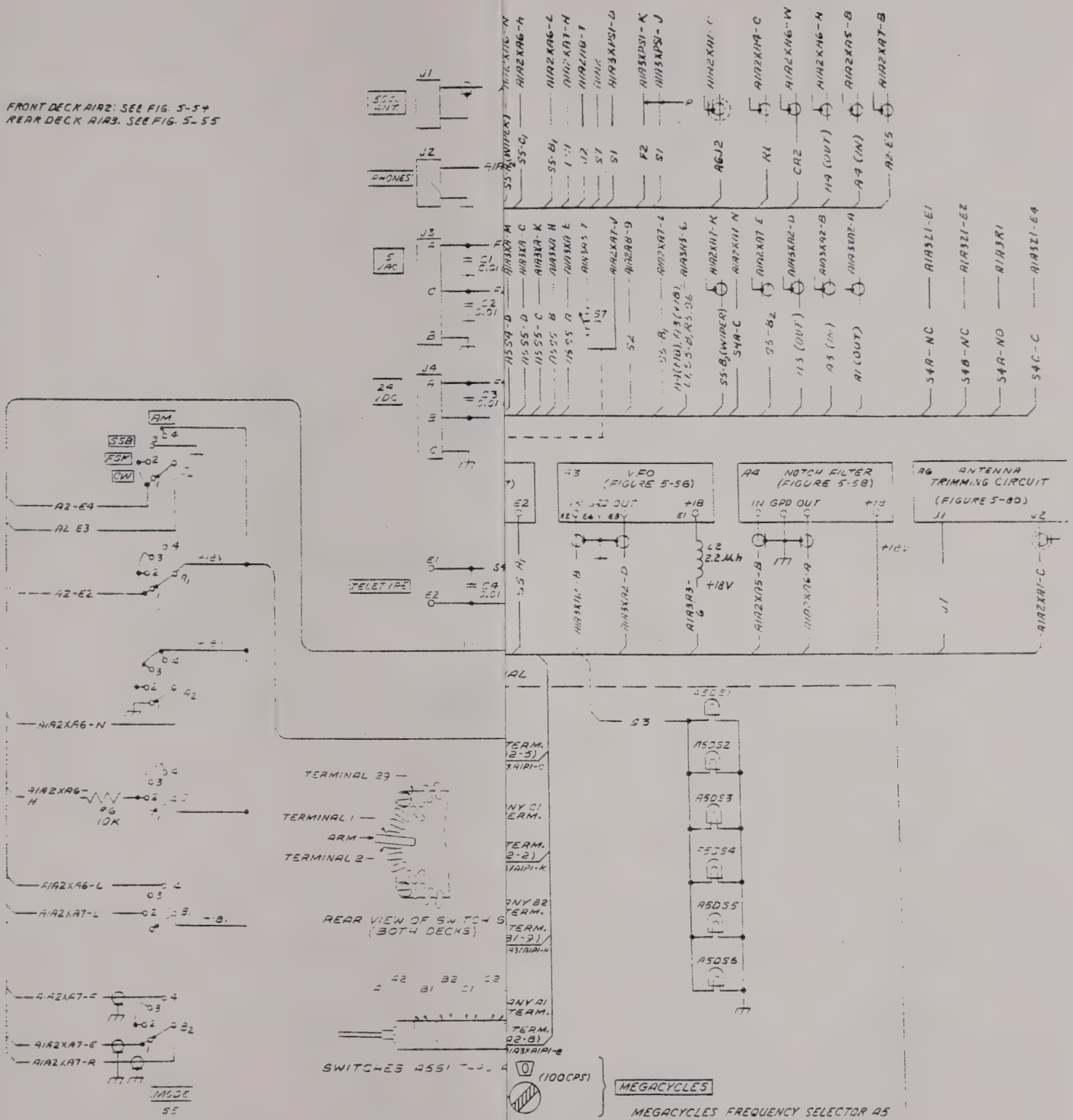


Figure 5-53. Receiver, Radio R-1490/GRR-17
Module Interconnection Diagram
(Sheet 1, Front Panel A1A1)

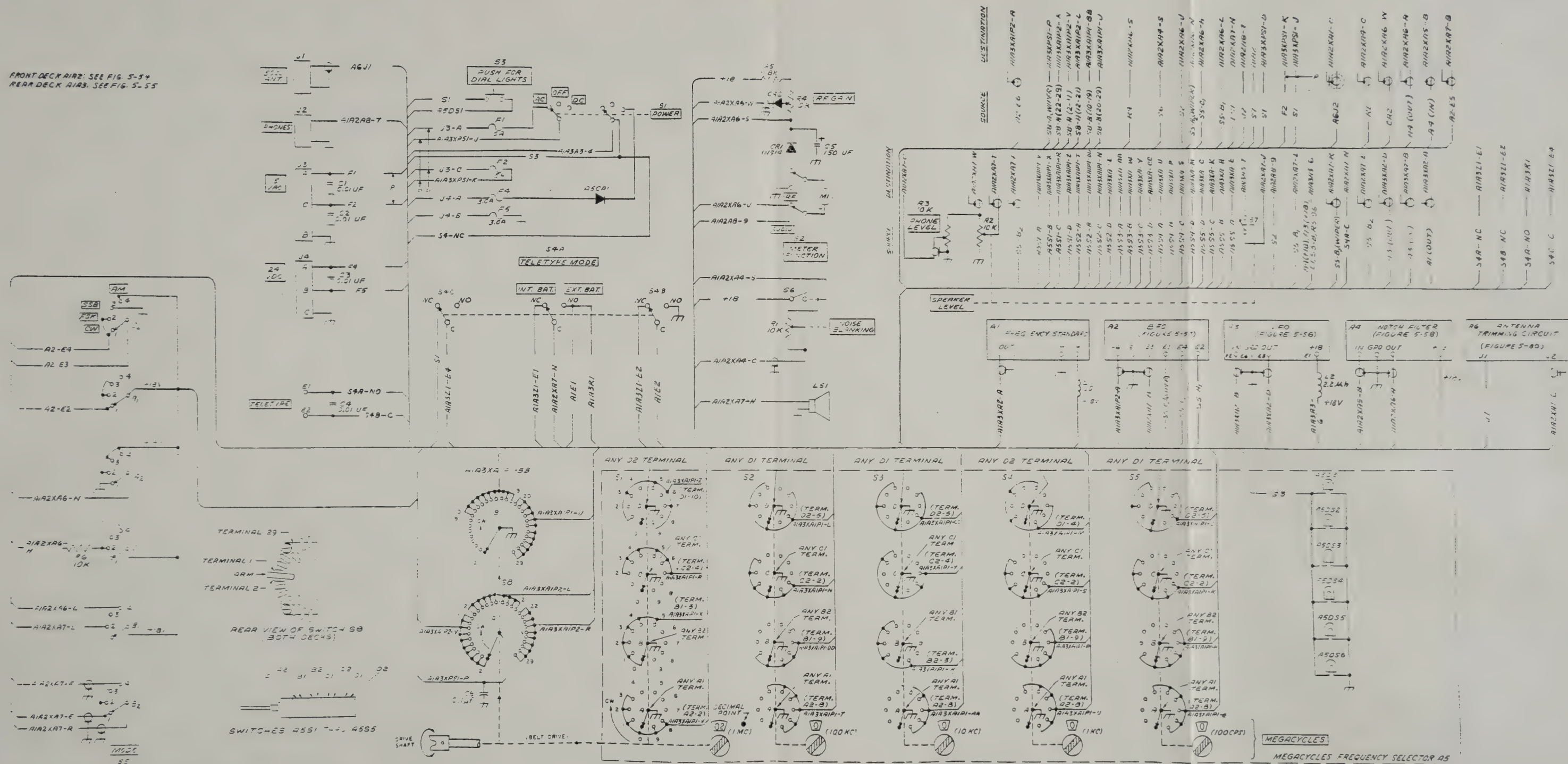
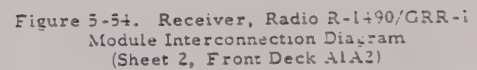
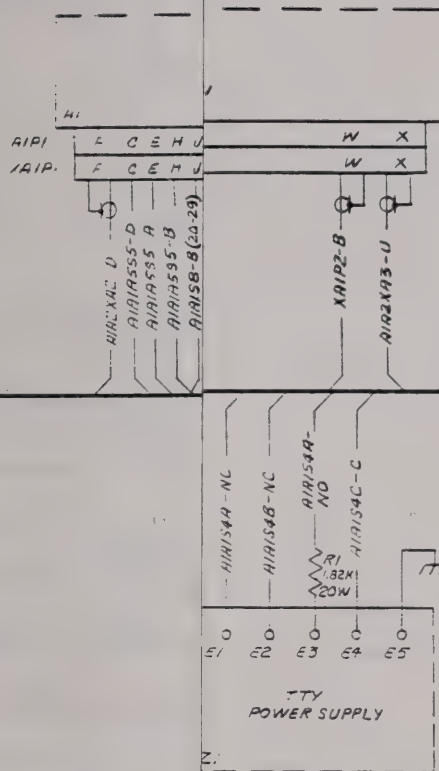
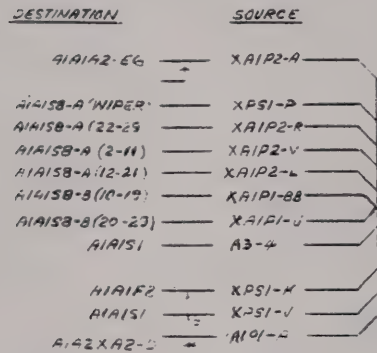


Figure 5-53. Receiver, Radio R-1490/GRR-17
Module Interconnection Diagram
(Sheet 1, Front Panel A1A1)





FRONT PANEL AIA1: SEE FIG. 5-53
FRONT DECK AIA2: SEE FIG. 5-54



FIX AIA3

FRONT PANEL AIA1: SEE FIG. 5-53
FRONT DECK AIA2: SEE FIG. 5-54

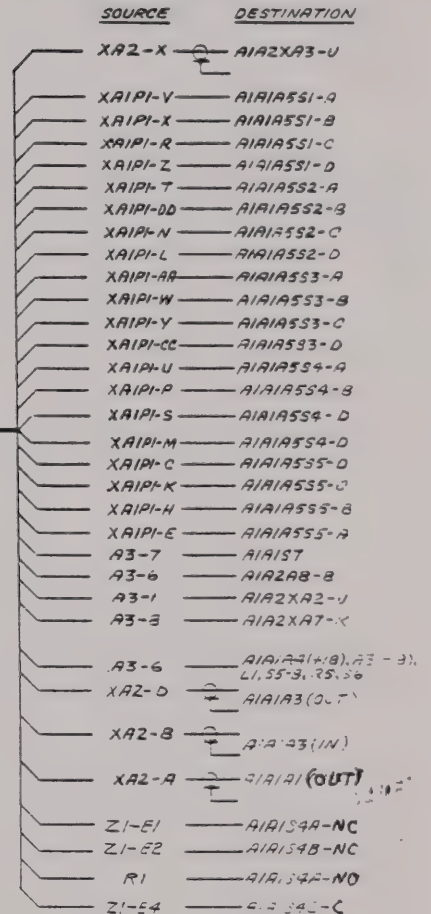


Figure 5-55. Receiver, Radio R-1490/GRR-17
Module Interconnection Diagram
(Sheet 3, Rear Deck AIA3)

FRONT PANEL AIA1: SEE FIG. 5-53
FRONT DECK AIA2: SEE FIG. 5-54

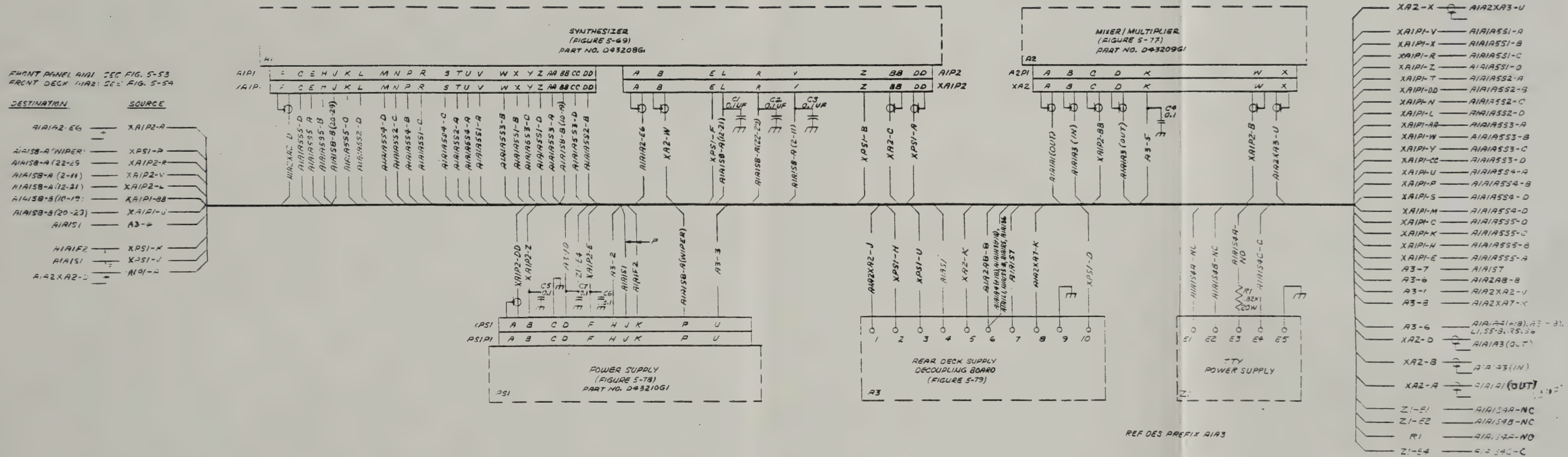


Figure 5-55. Receiver Radio R-1490/GRR-17
Module Interconnection Diagram
(Sheet 3, Rear Deck AIA3)

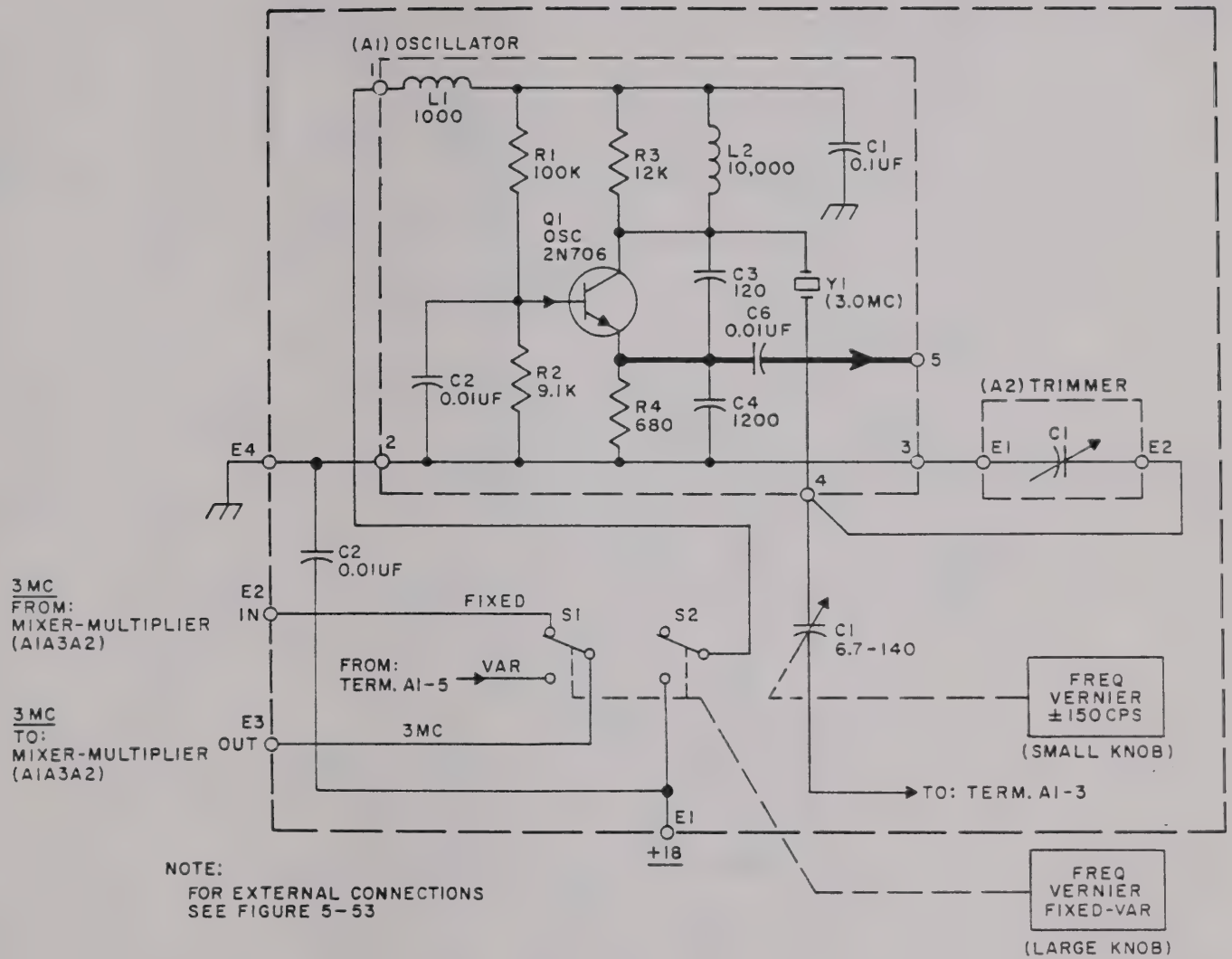


Figure 5-56. VFO A1A1A3,
Schematic Diagram

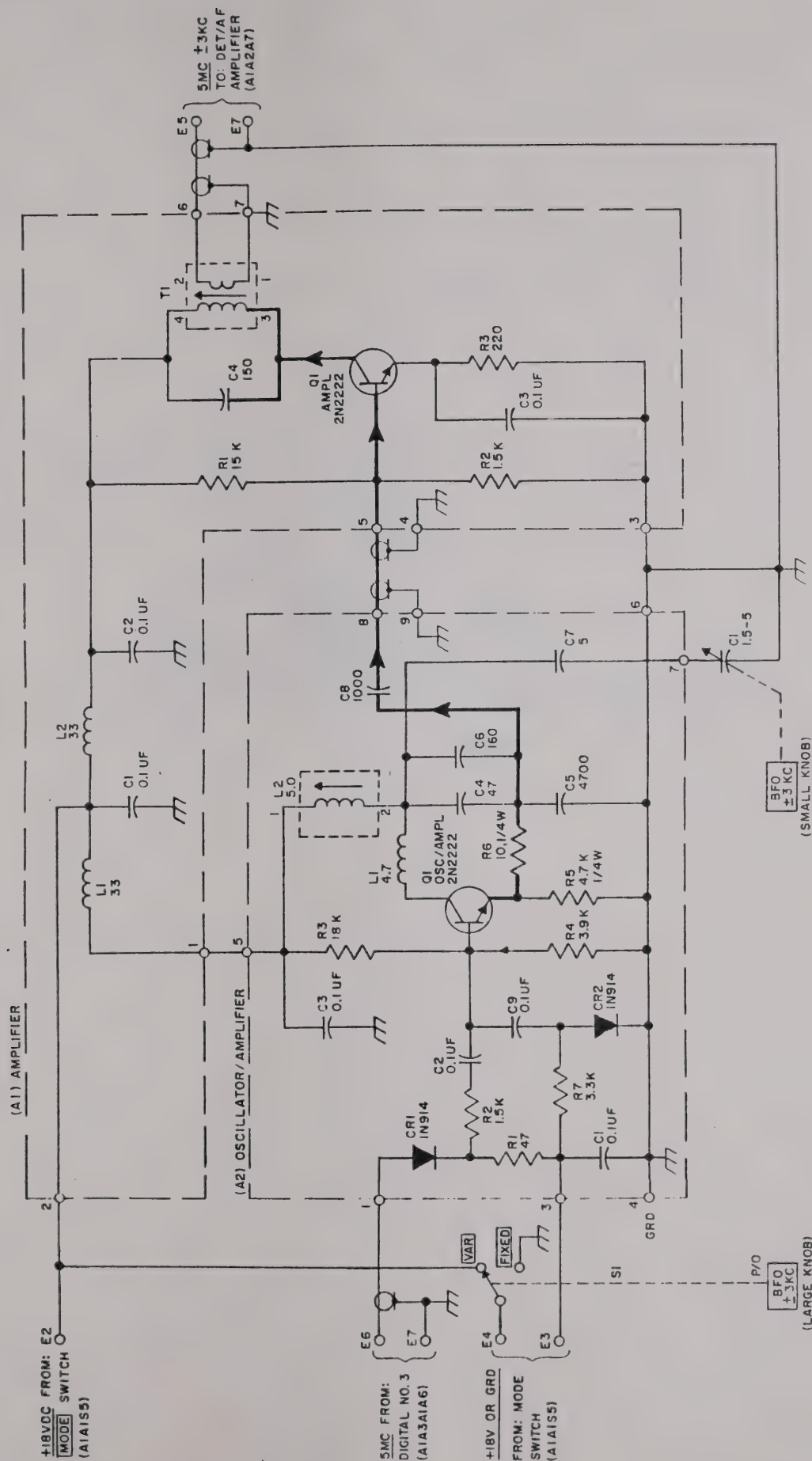


Figure 5-57. BFO A1A1A2,
Schematic Diagram

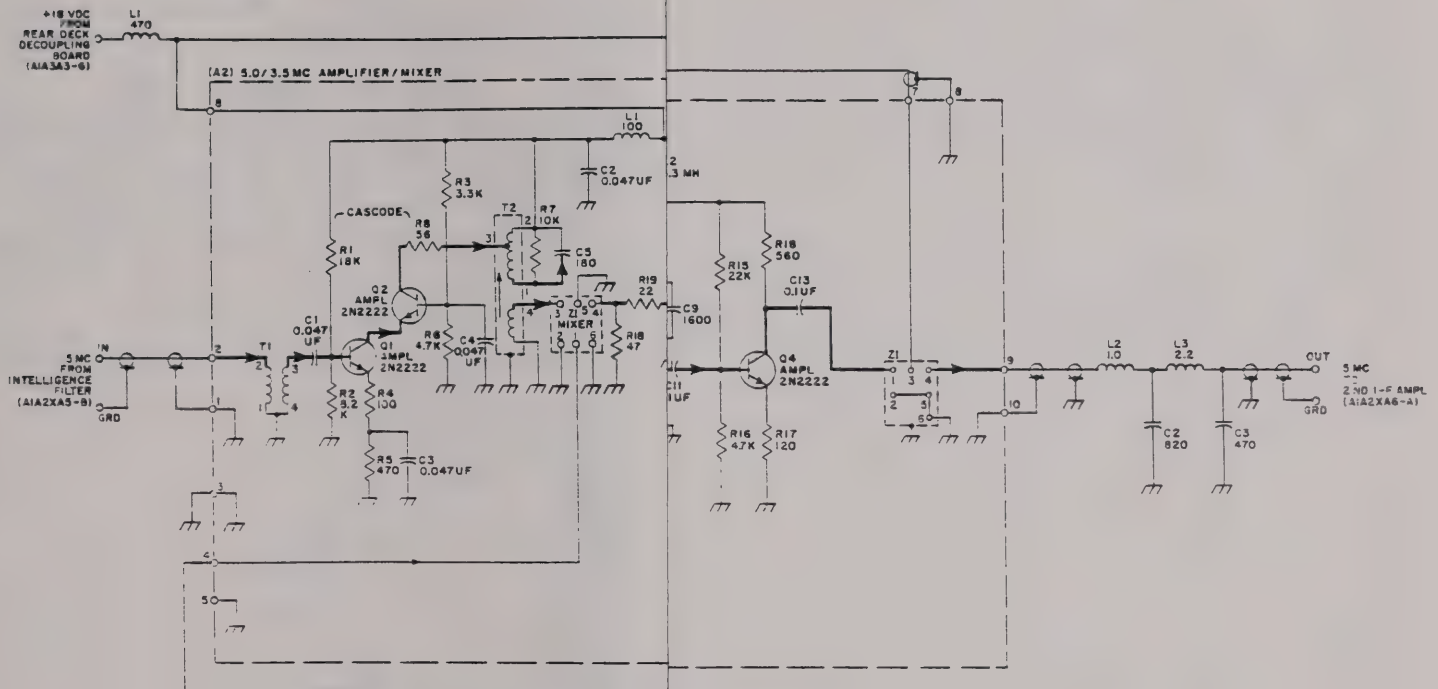


Figure 5-58. Notch Filter A1A4,
Schematic Diagram

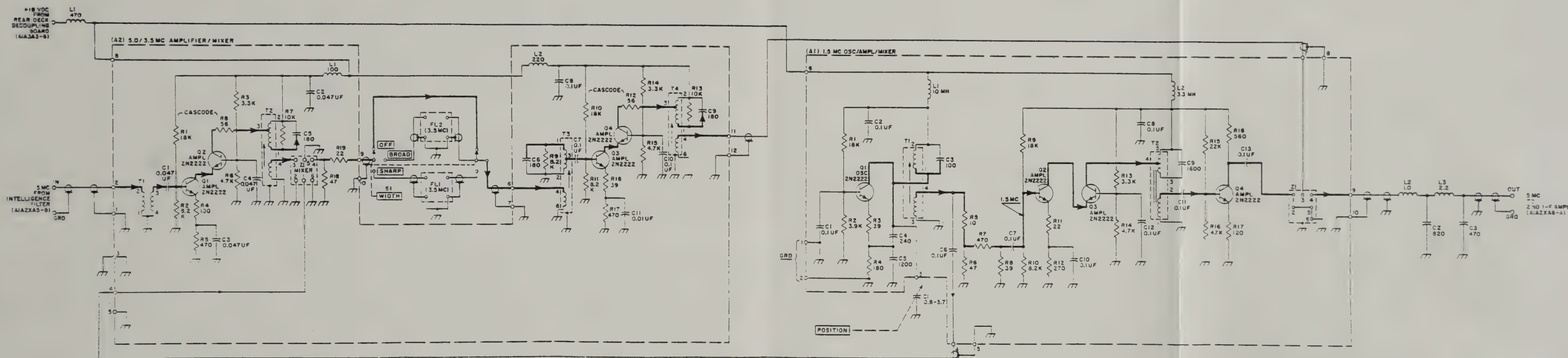


Figure 5-58. Notch Filter AlA1A4.
Schematic Diagram

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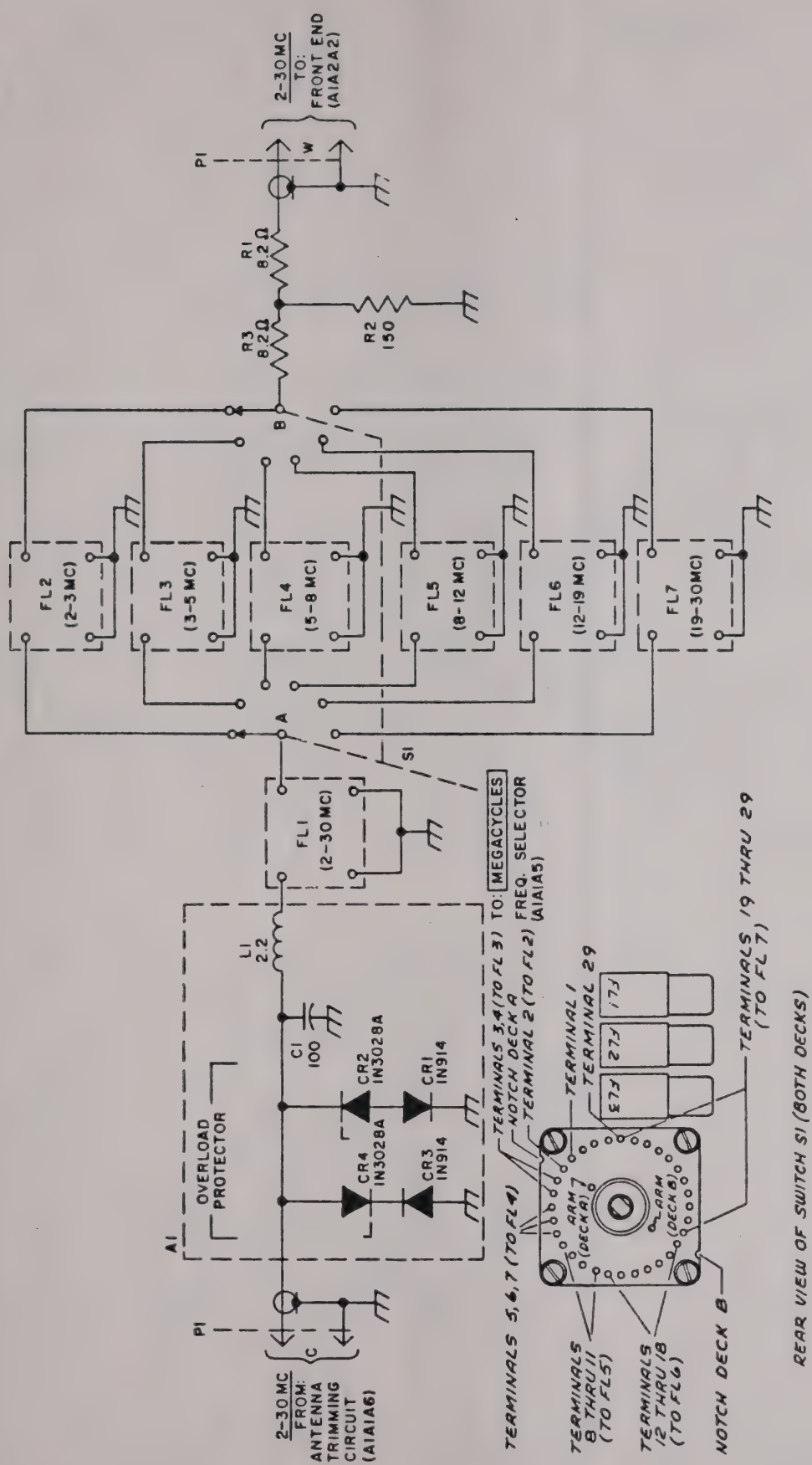


Figure 5-59. Input Filter ALA2A1, Schematic Diagram

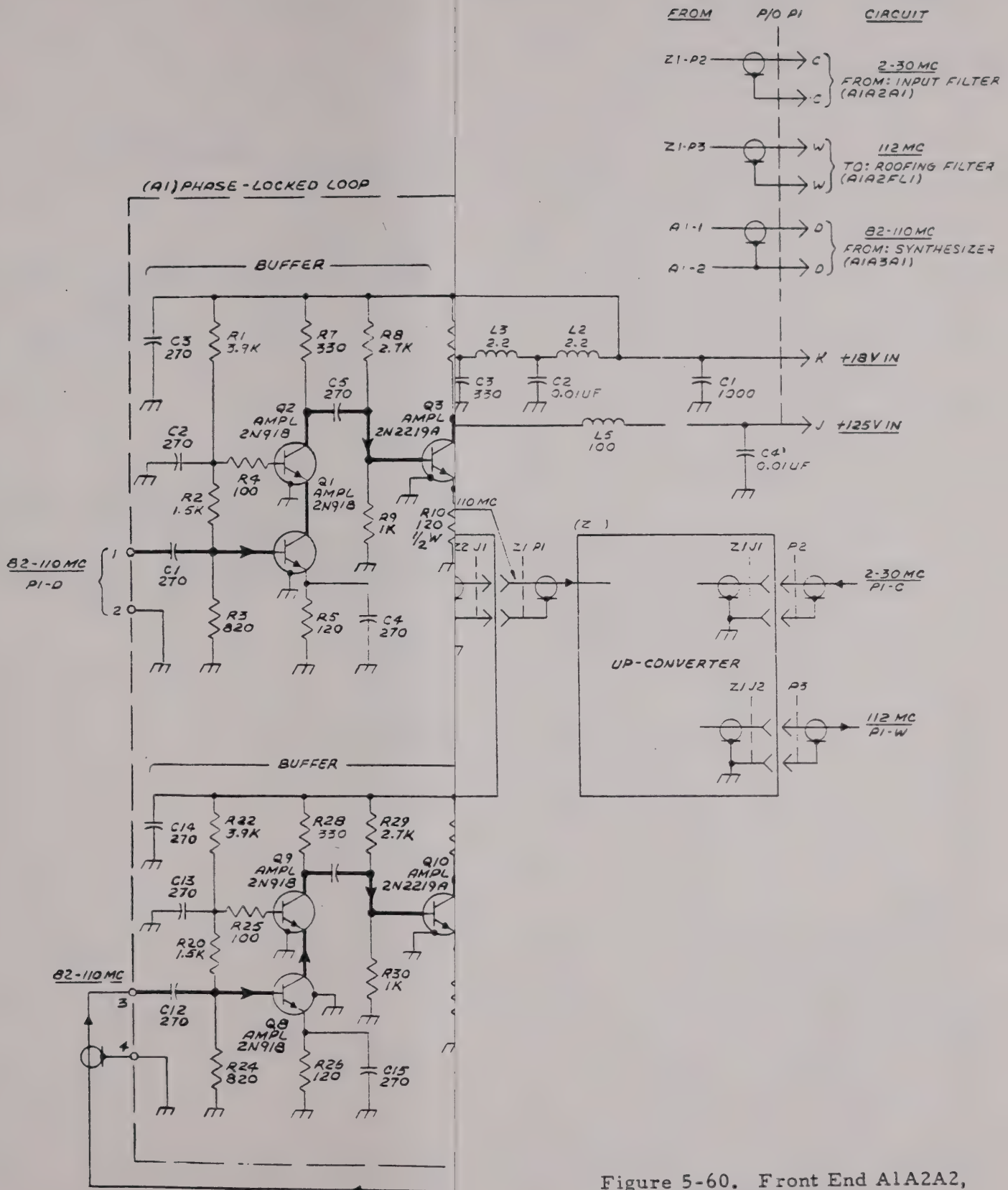


Figure 5-60. Front End A1A2A2,
Schematic Diagram

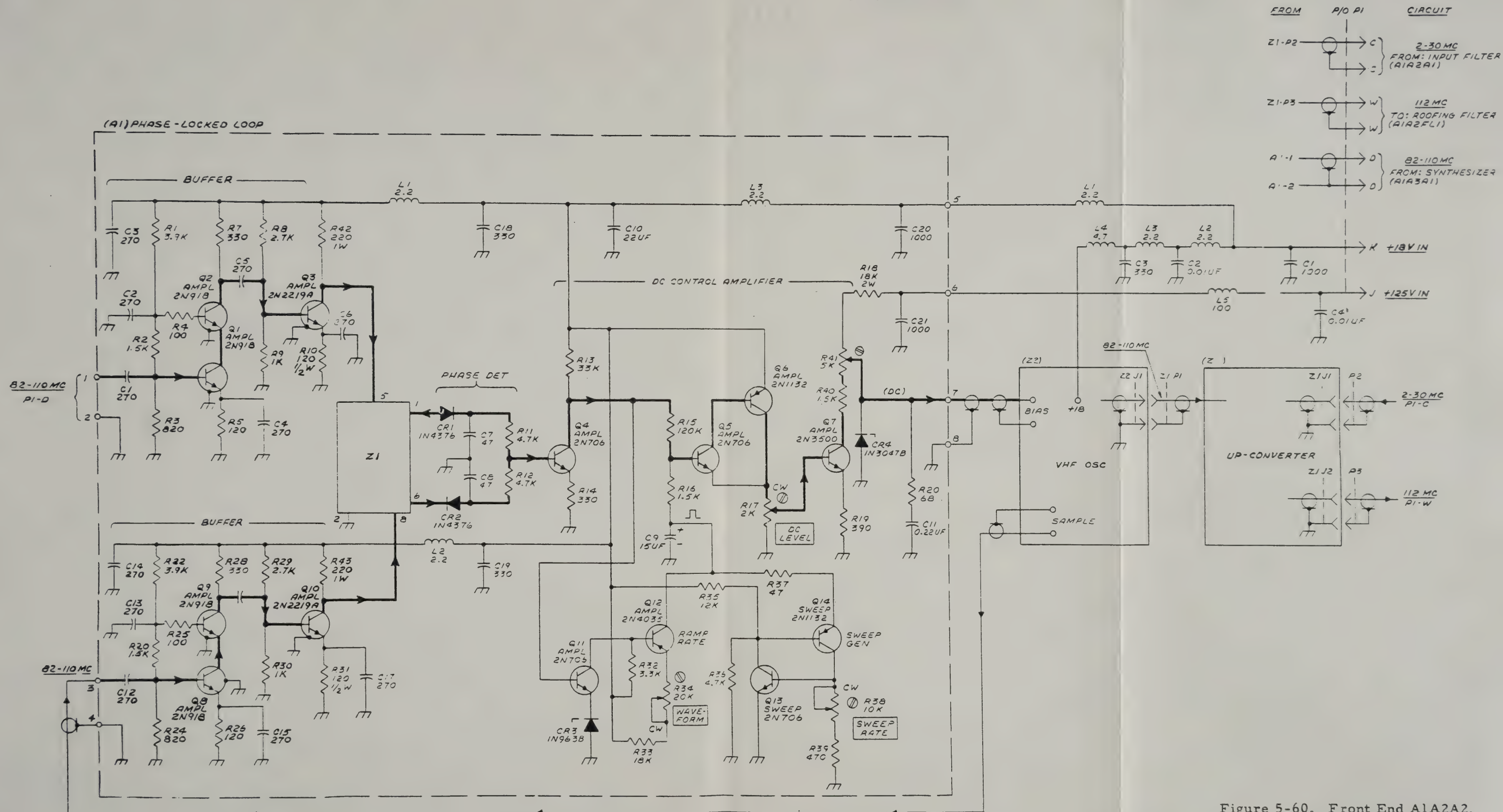


Figure 5-60. Front End A1A2A2,
Schematic Diagram

(A3) 117 MC BUFFER-AMPLIFIER

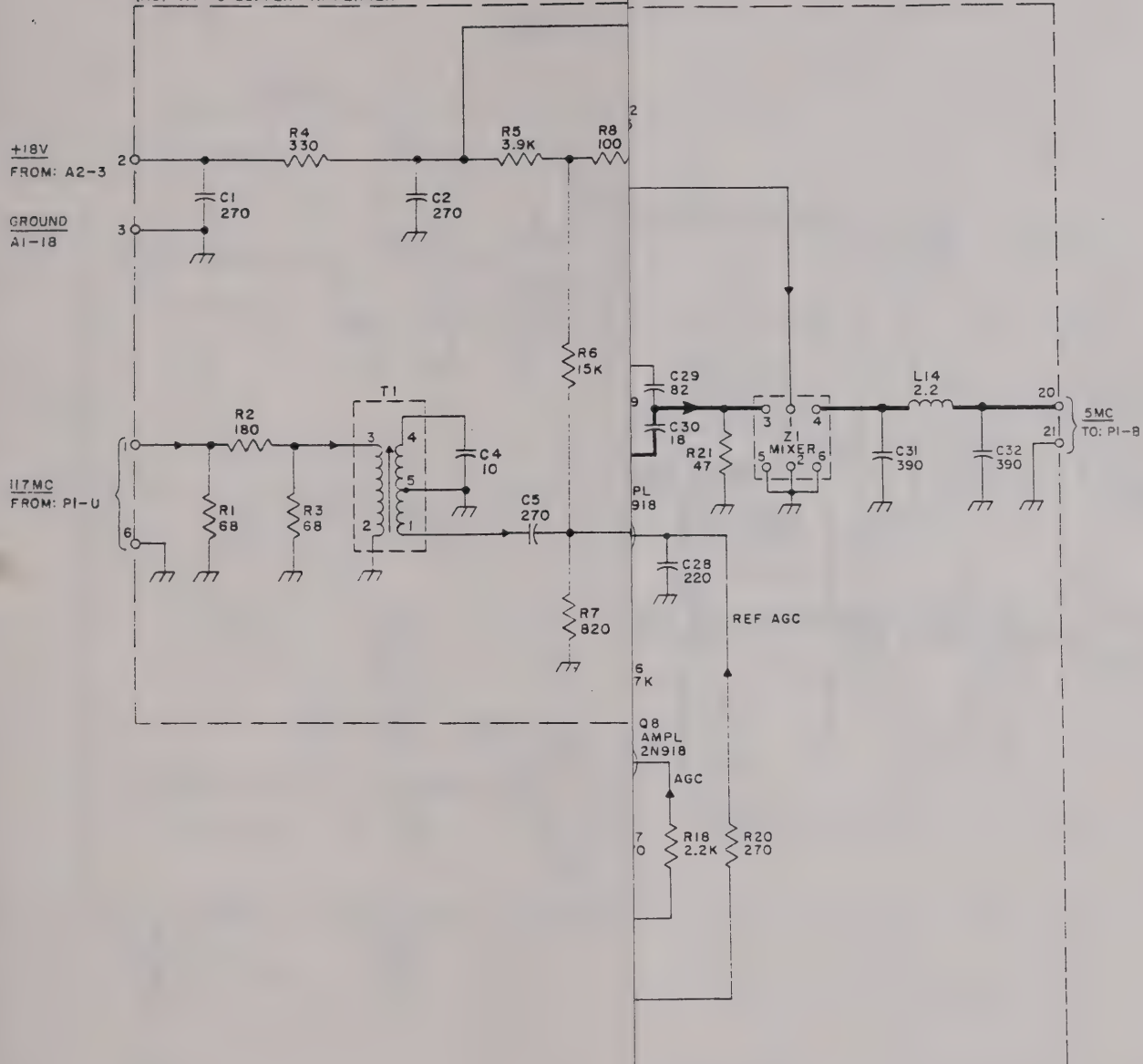


Figure 5-61. First I-F Amplifier A1A2A3, Schematic Diagram

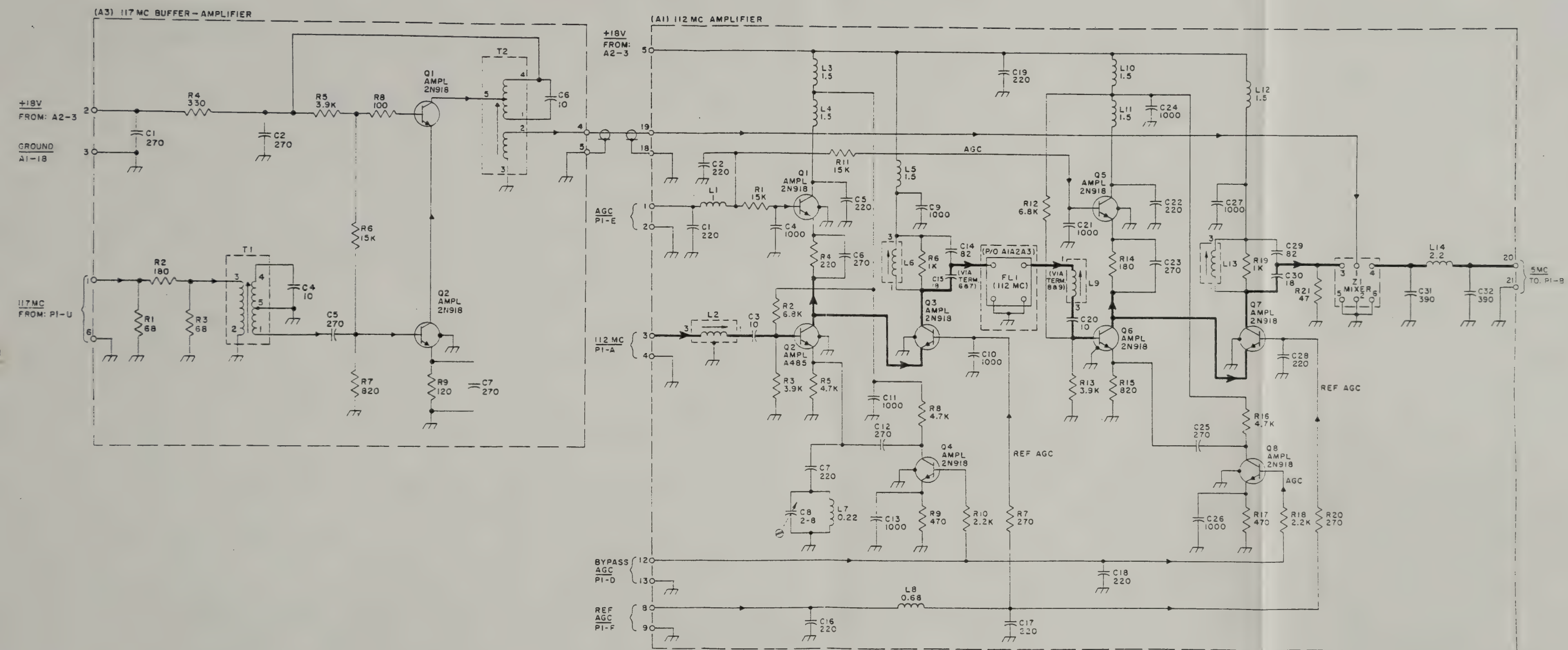
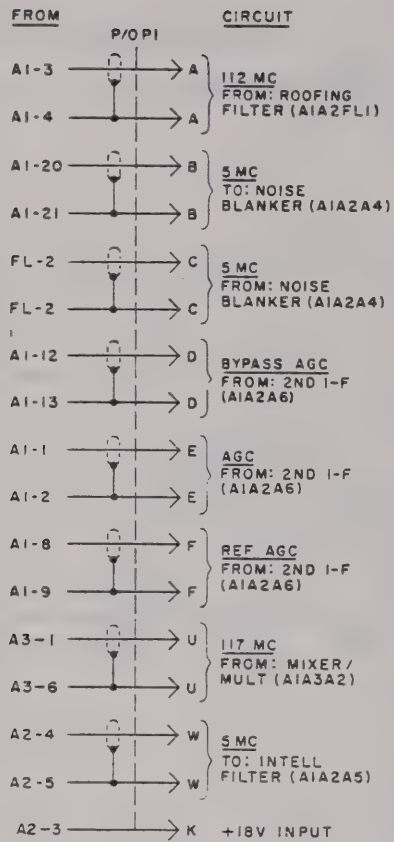


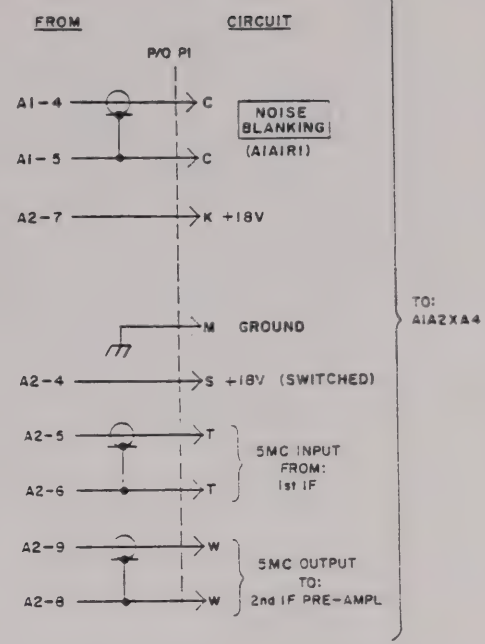
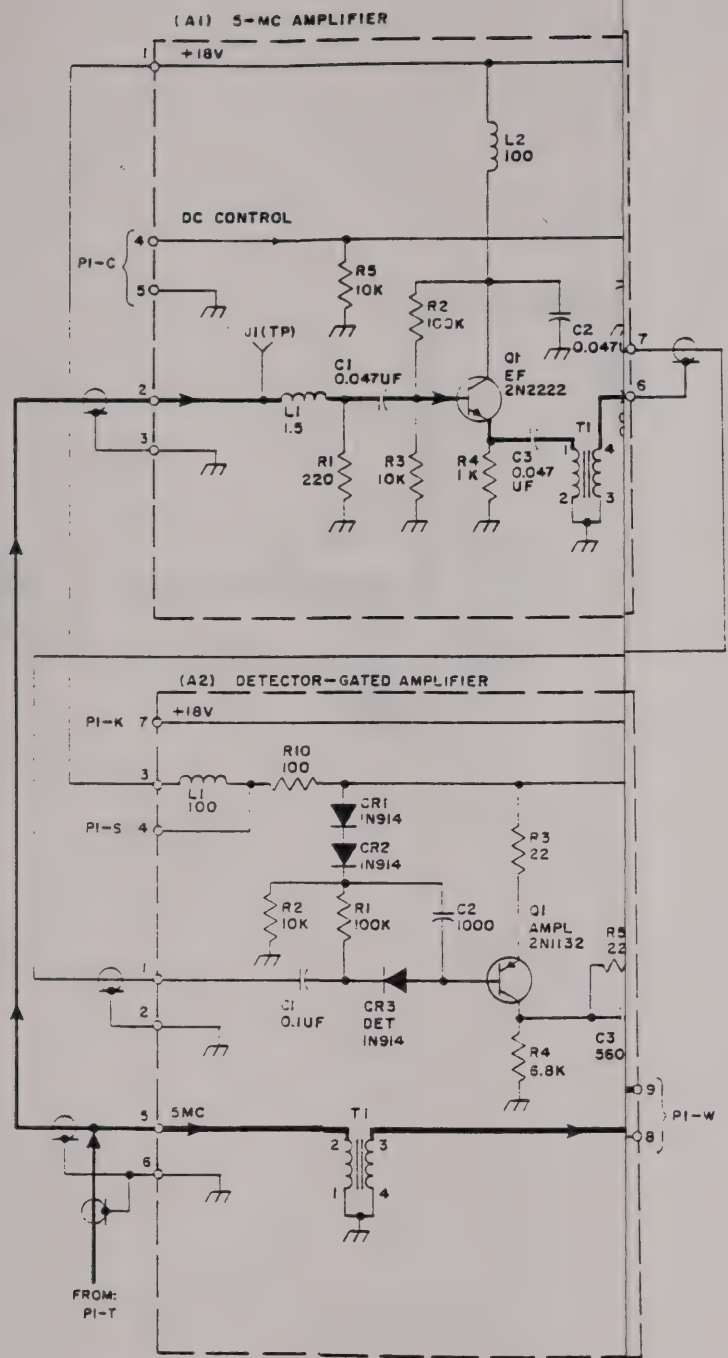
Figure 5-61. First I-F Amplifier A1A2A3, Schematic Diagram

ORIGINAL

Figure
5-61



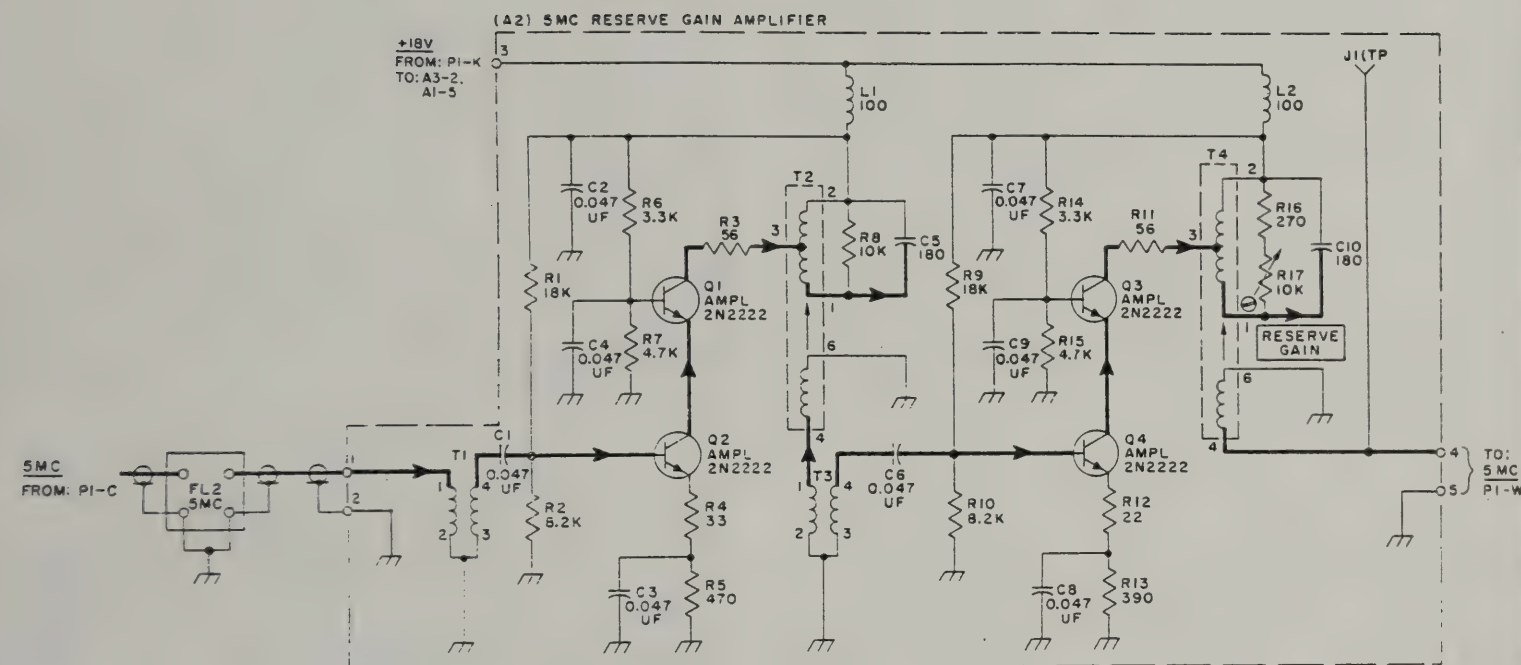
61. First I-F Amplifier A1A2A3,
Schematic Diagram



NOTES:
1. FOR EXTERNAL CONNECTIONS SEE FIGURE 5-54

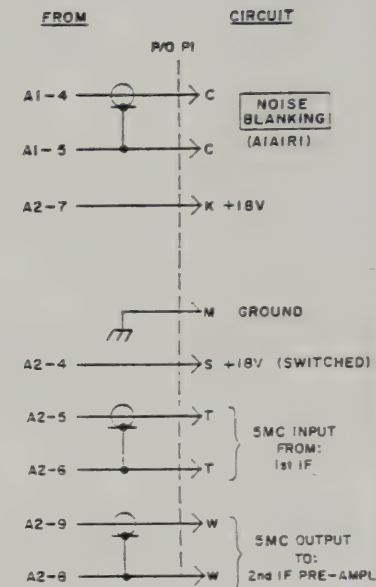
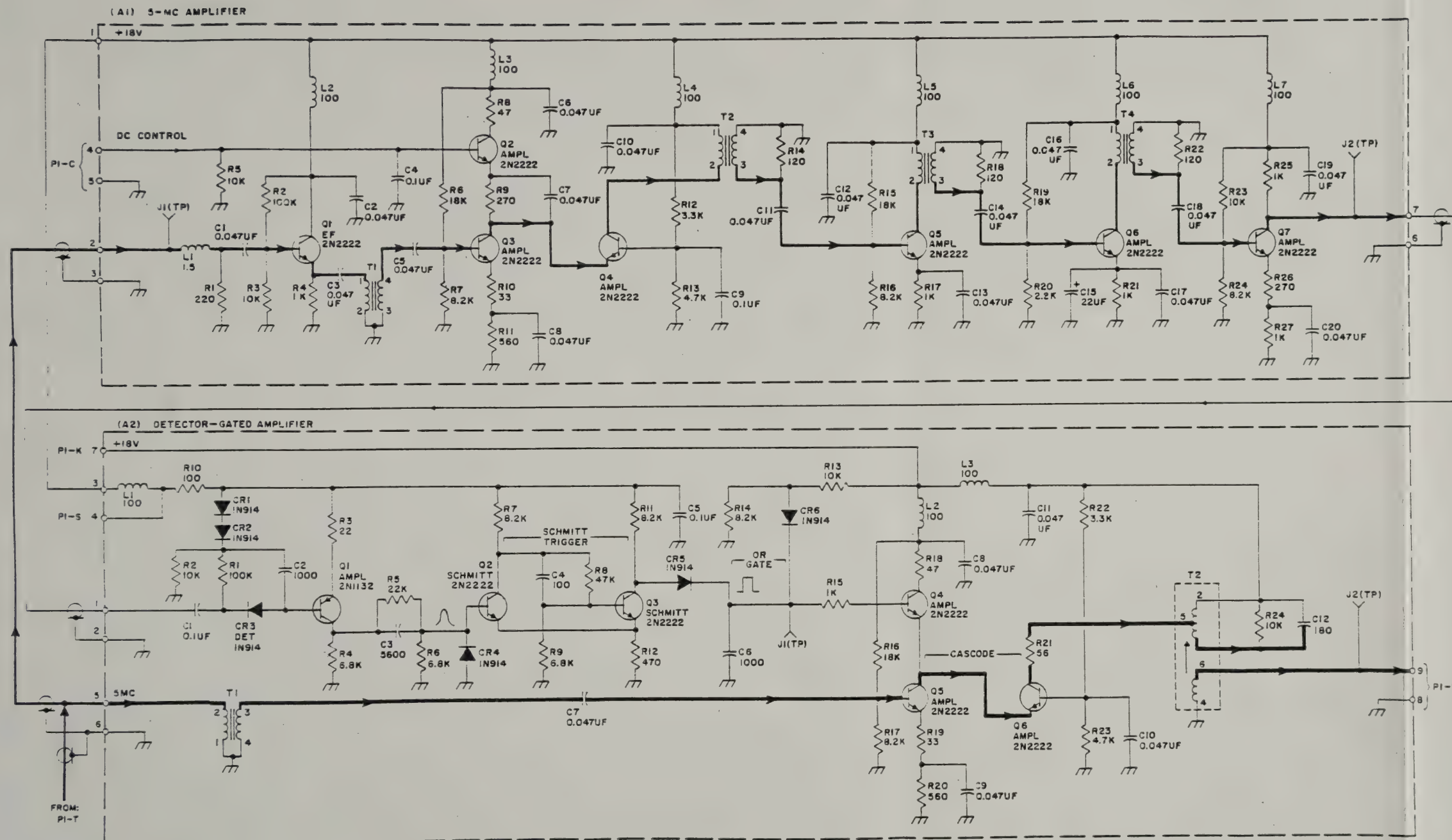
SIGNAL	NOISE PULSE	SCHMITT PULSE
NO BLANKING (T2 OUTPUT)	 FROM: NOISE DETECTOR A2CR3	 FROM: SCHMITT TRIGGER A2CR3
BLANKED (T2 OUTPUT)		

Figure 5-62. Noise Blanker A1A2A4,
Schematic Diagram



FROM	P/OPI	CIRCUIT
A1-3	A	112 MC FROM: ROOFING FILTER (A1A2FL1)
A1-4	A	
A1-20	B	5 MC TO: NOISE BLANKER (A1A2A4)
A1-21	B	
FL-2	C	5 MC FROM: NOISE BLANKER (A1A2A4)
FL-2	C	
A1-12	D	BYPASS AGC FROM: 2ND I-F (A1A2A6)
A1-13	D	
A1-1	E	AGC FROM: 2ND I-F (A1A2A6)
A1-2	E	
A1-8	F	REF AGC FROM: 2ND I-F (A1A2A6)
A1-9	F	
A3-1	U	117 MC FROM: MIXER/ MULT (A1A3A2)
A3-6	U	
A2-4	W	5 MC TO: INTELL FILTER (A1A2A5)
A2-5	W	
A2-3	K	+18V INPUT

Figure 5-61. First I-F Amplifier A1A2A3,
Schematic Diagram



NOTES:
1. FOR EXTERNAL CONNECTIONS SEE FIGURE 5-54

SIGNAL	NOISE PULSE	SCHMITT PULSE
NO BLANKING (T2 OUTPUT)	FROM: NOISE DETECTOR A2CR3	FROM: SCHMITT TRIGGER A2Q3
BLANKED (T2 OUTPUT)		

Figure 5-62. Noise Blanker A1A2A4,
Schematic Diagram

ORIGINAL

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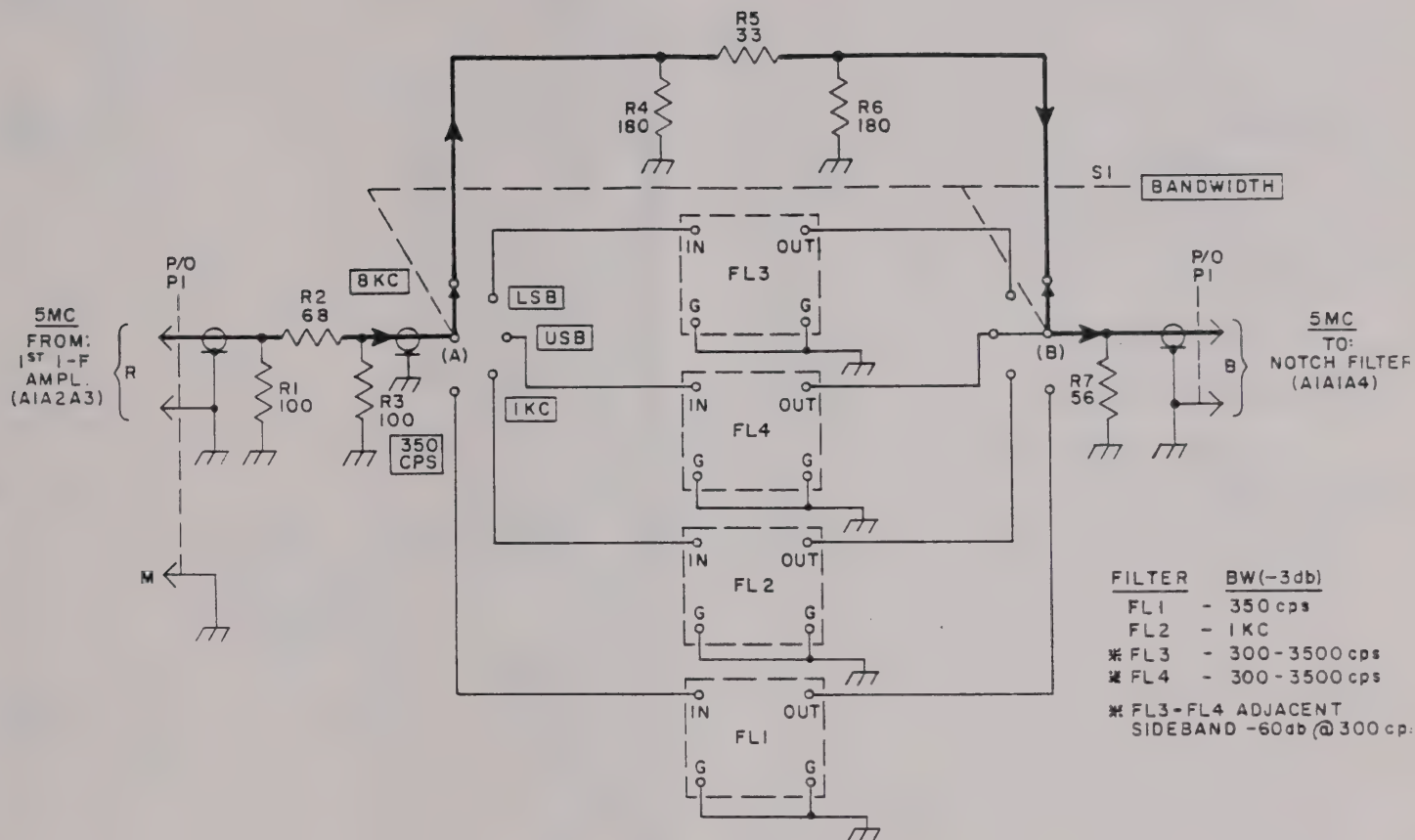


Figure 5-63. Intelligence Filter A1A2A5,
Schematic Diagram

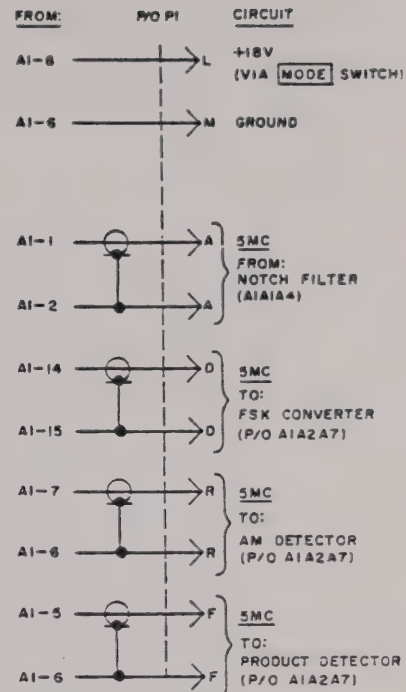
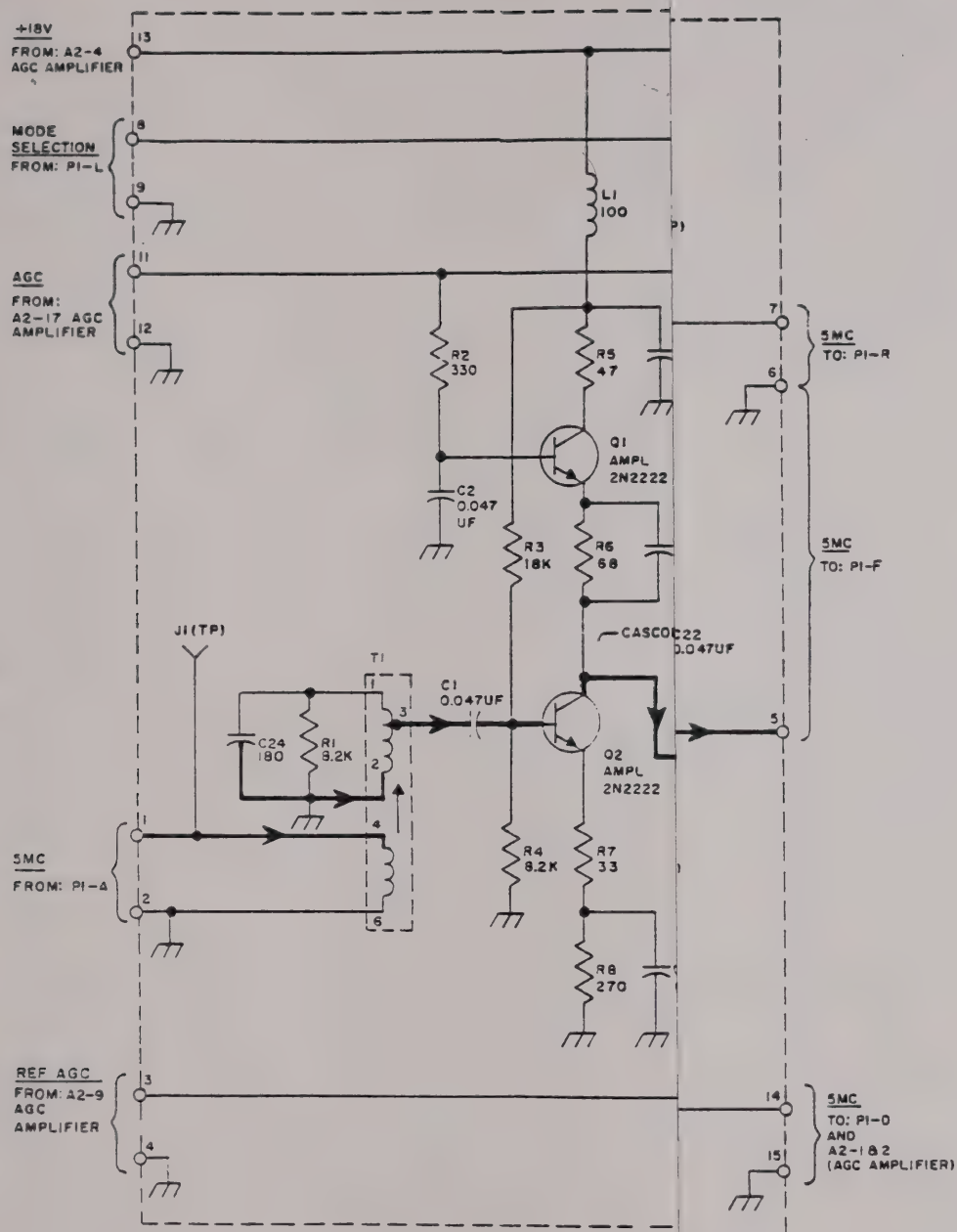
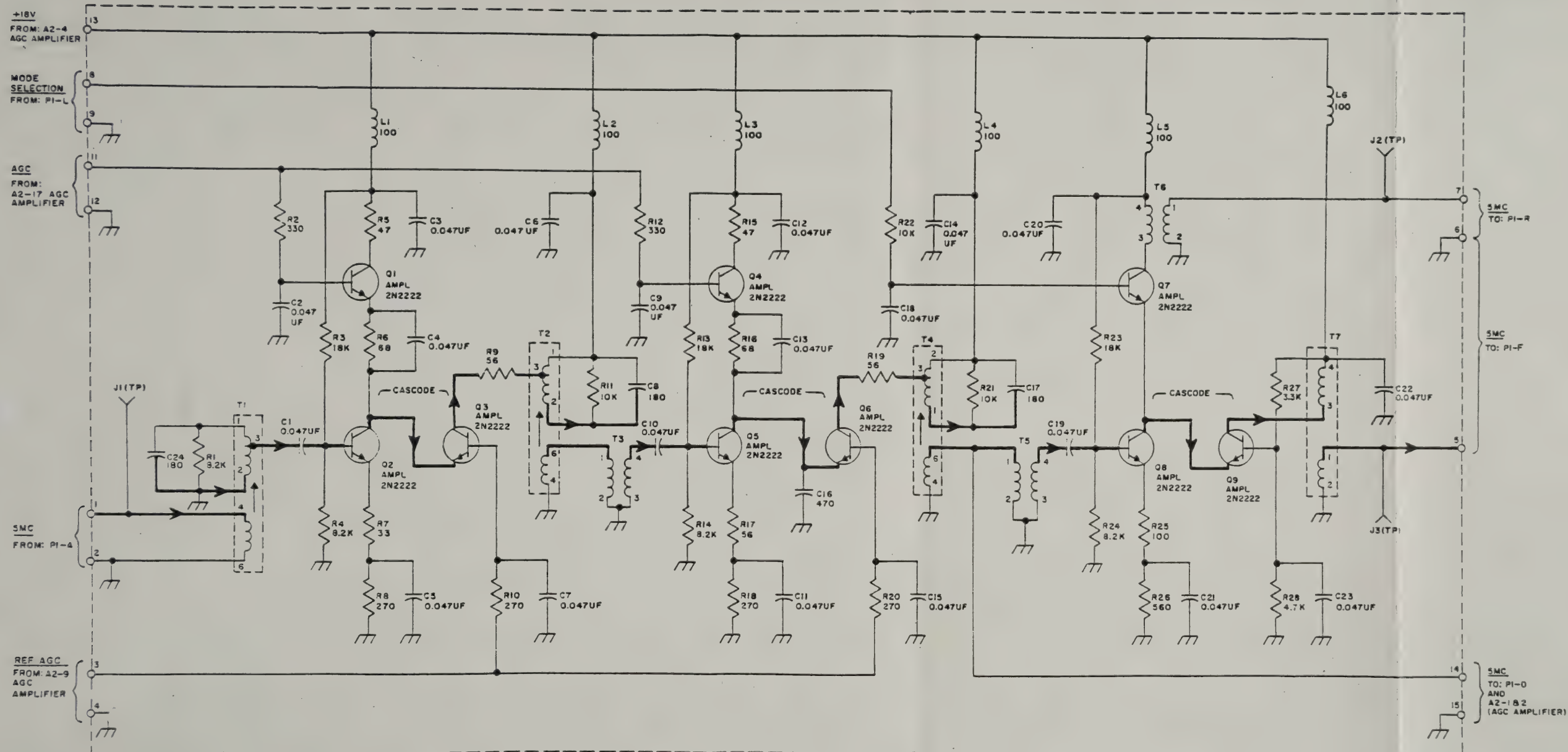


Figure 5-64. Second I-F/AGC Amplifier
A1A2A6, Schematic Diagram (Sheet 1)



FROM:	PRO PI	CIRCUIT
AI-8	L	+18V (VIA MODE SWITCH)
AI-6	M	GROUND
AI-1	A	SMC FROM: NOTCH FILTER (A1A1A4)
AI-2	A	
AI-14	D	SMC TO: FSK CONVERTER (P/O A1A2A7)
AI-15	D	
AI-7	R	SMC TO: AM DETECTOR (P/O A1A2A7)
AI-6	R	
AI-5	F	SMC TO: PRODUCT DETECTOR (P/O A1A2A7)
AI-6	F	

Figure 5-64. Second I-F/AGC Amplifier
AlA2A6, Schematic Diagram (Sheet 1)

ORIGINAL

5-115/5-116

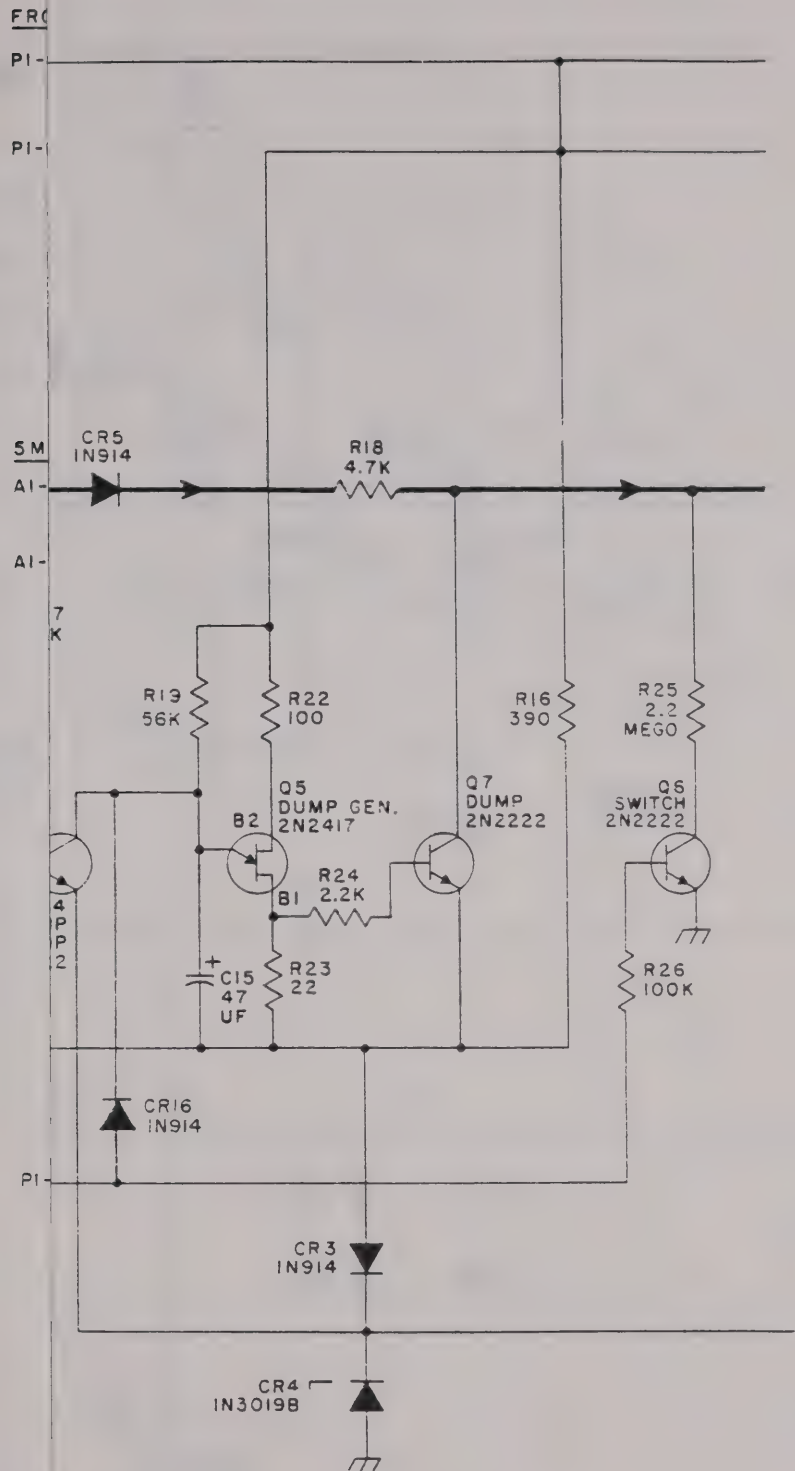


Figure 5-65. Second I-F/AGC Amplifier
AlA2A6, Schematic Diagram (Sheet 2)

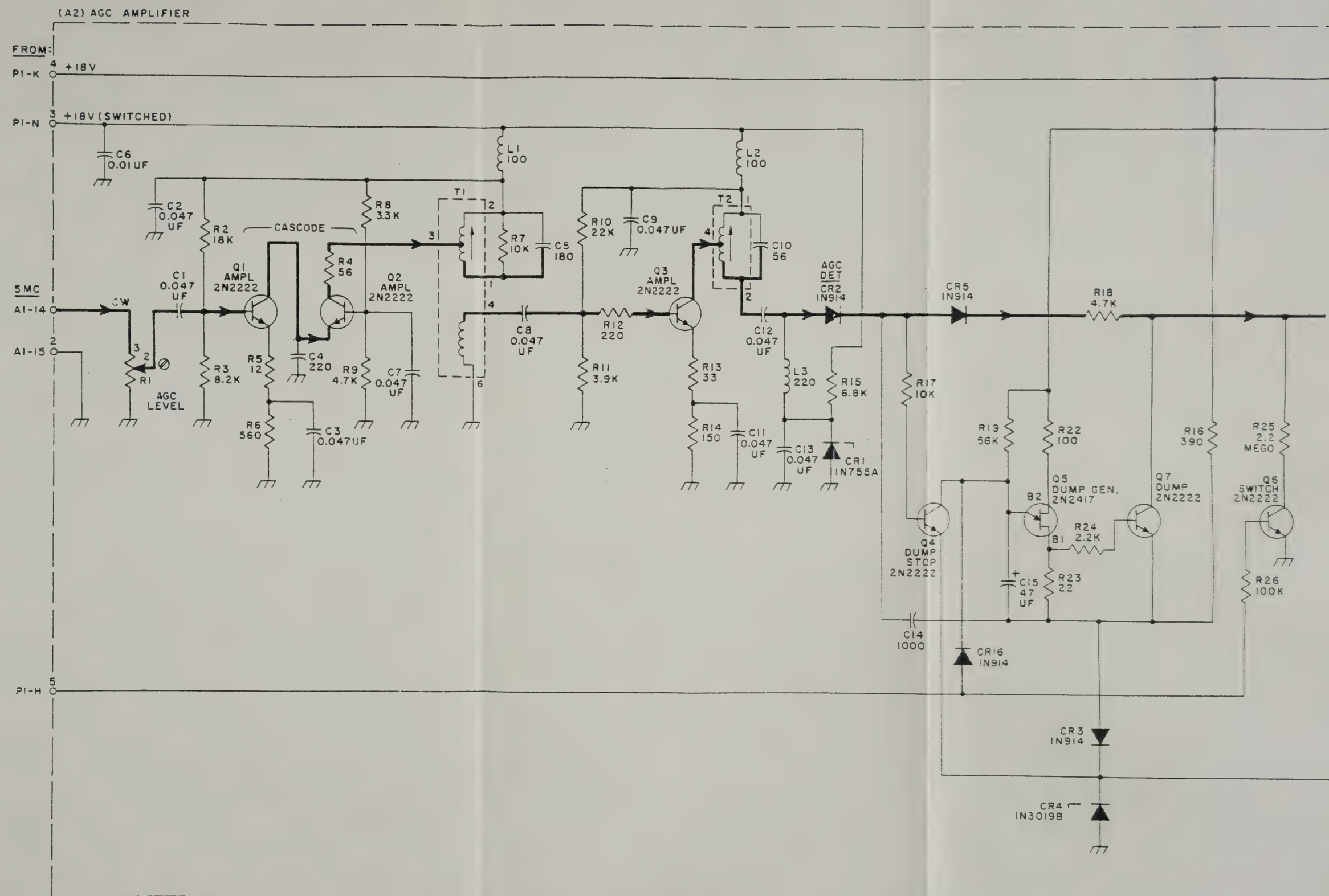


Figure 5-65. Second I-F/AGC Amplifier
A1A2A6, Schematic Diagram (Sheet 2)

ORIGINAL

5-117/5-118

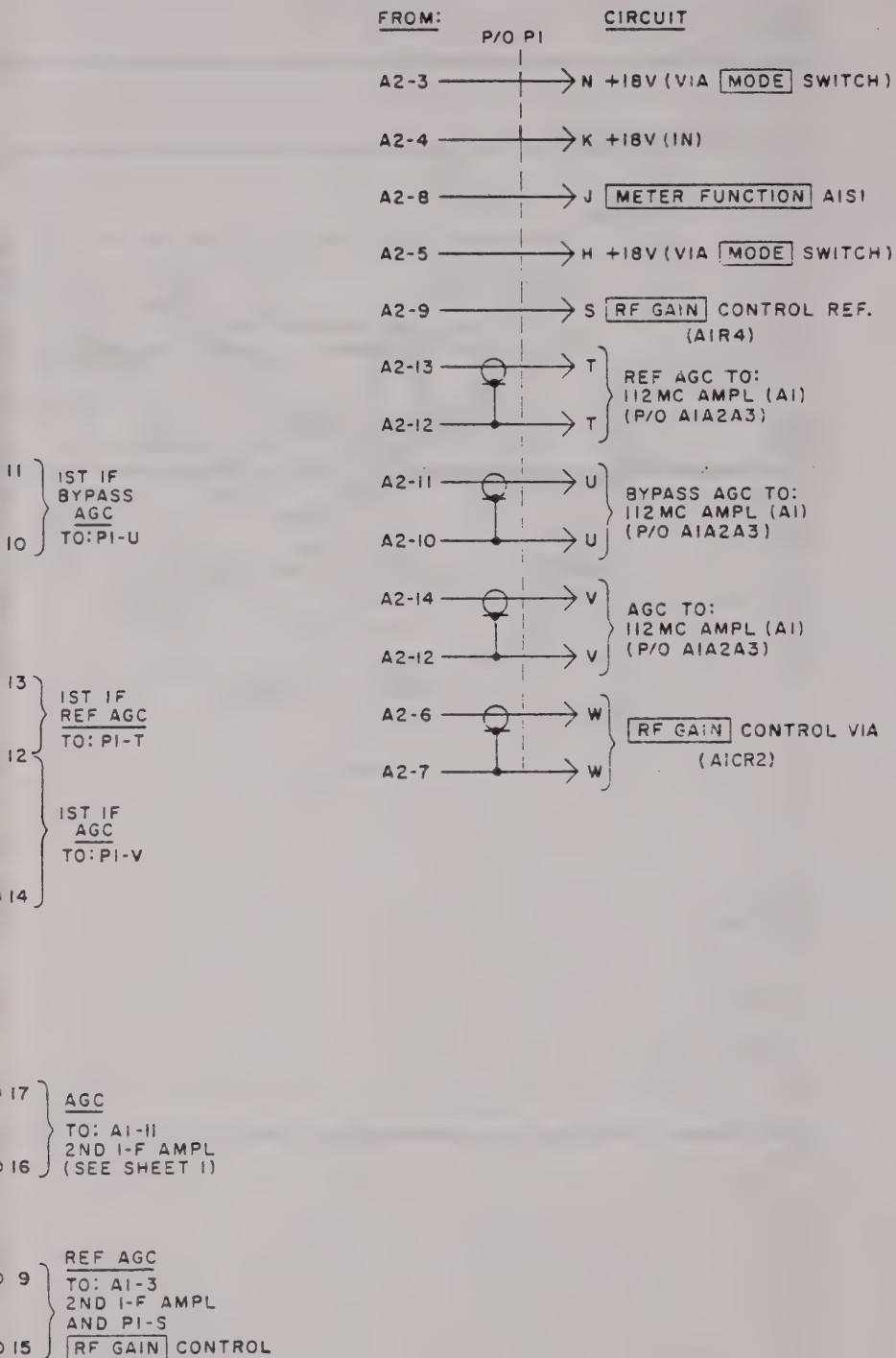


Figure 5-65. Second I-F/AGC Amplifier
A1A2A6, Schematic Diagram (Sheet 2)

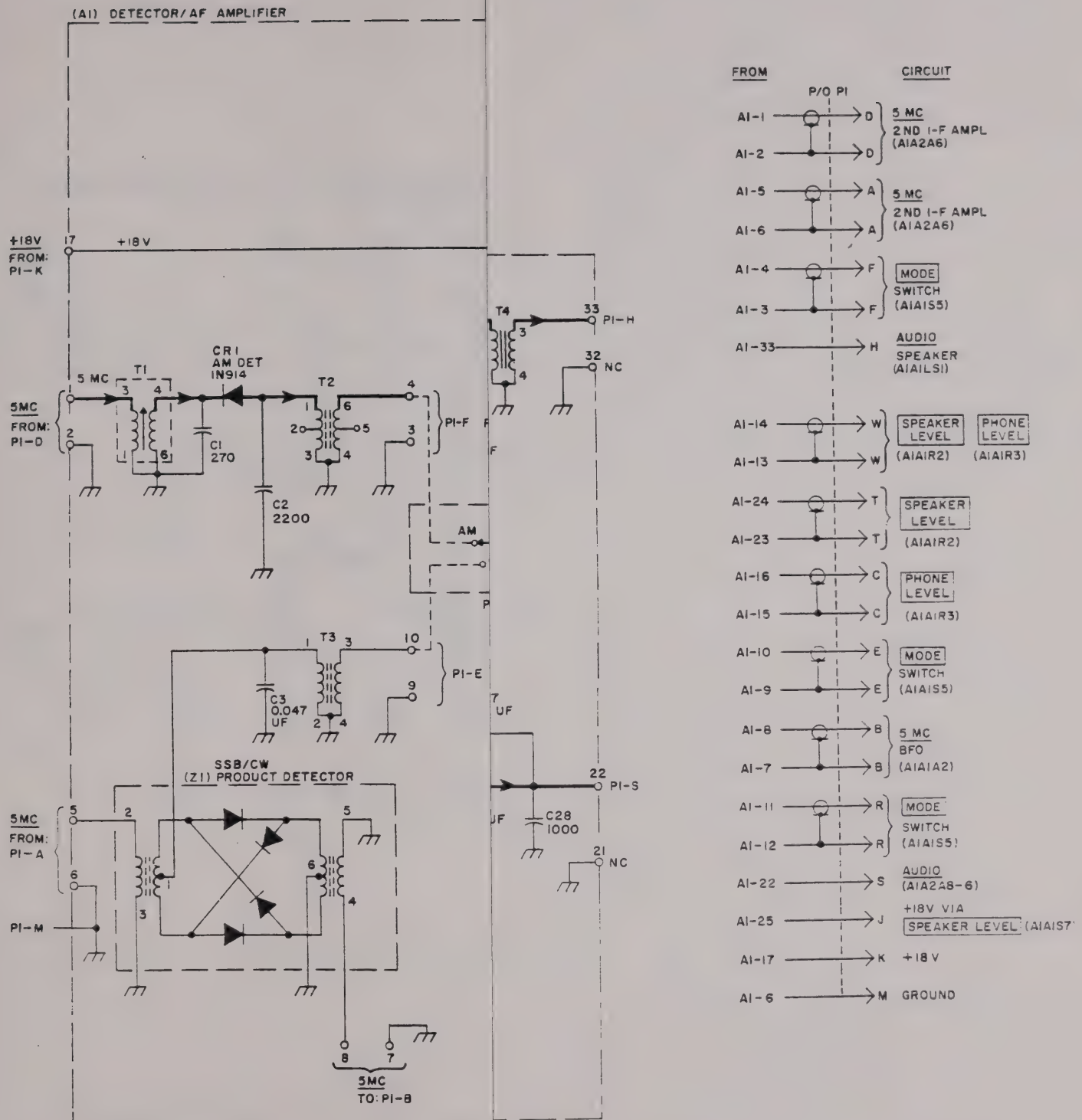
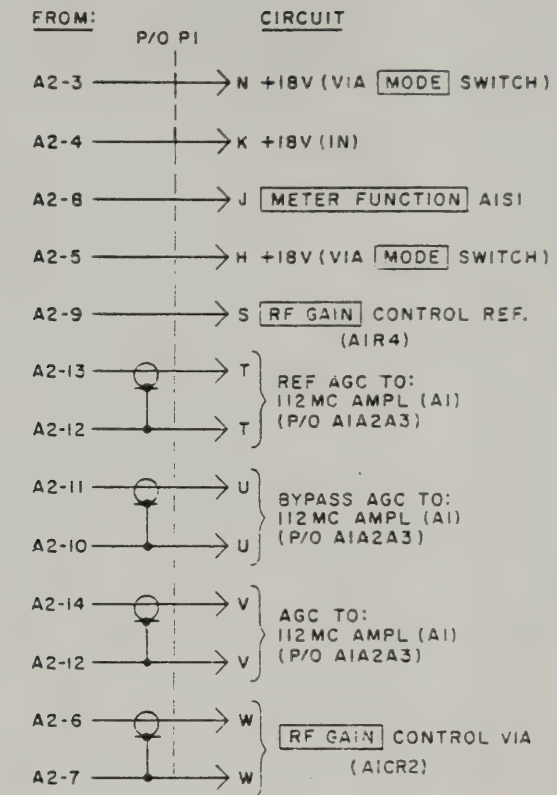
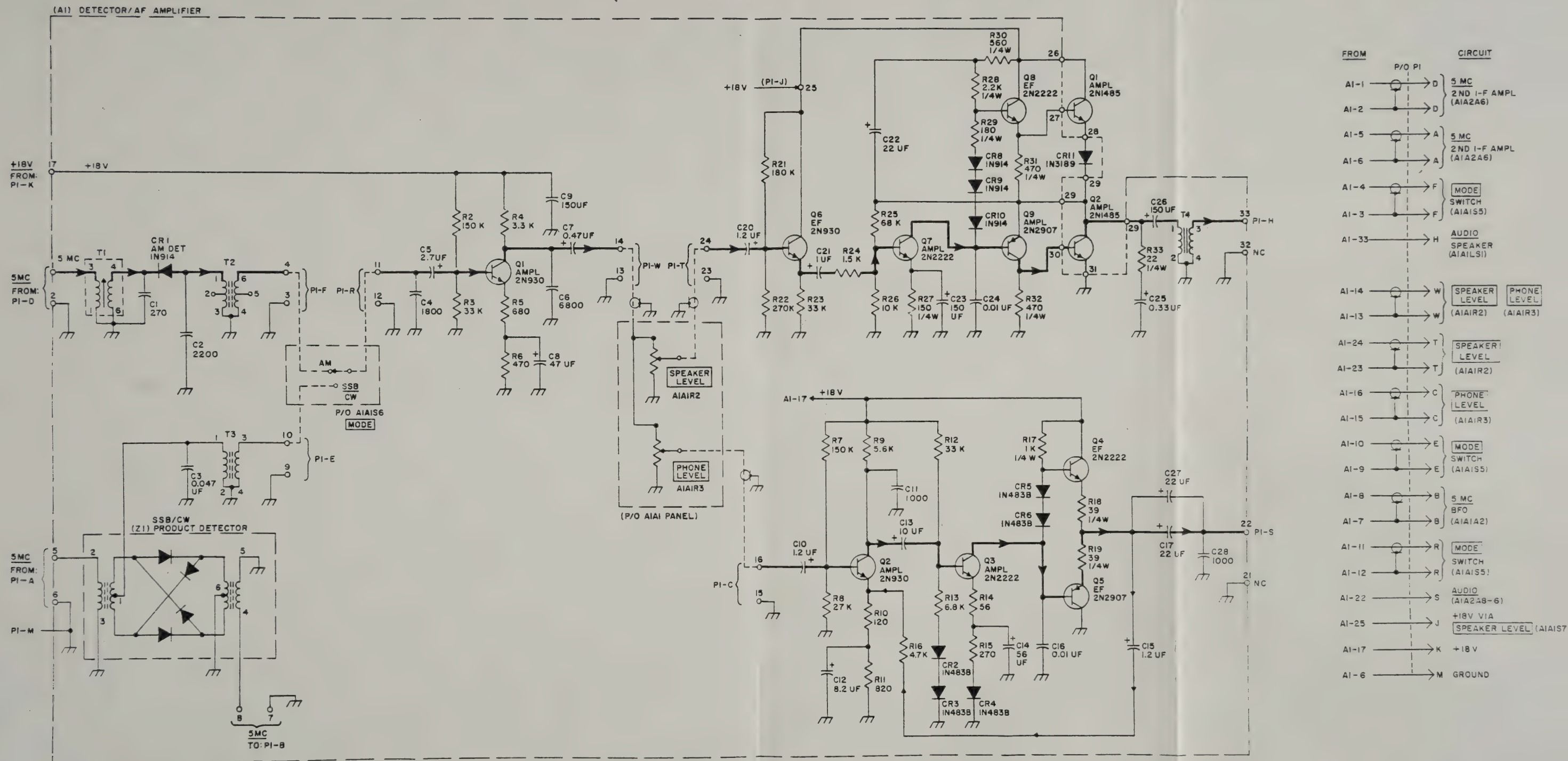


Figure 5-66. Detector/AF Amplifier AlA2A7,
Schematic Diagram (Sheet 1)

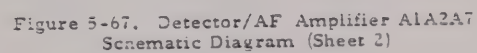


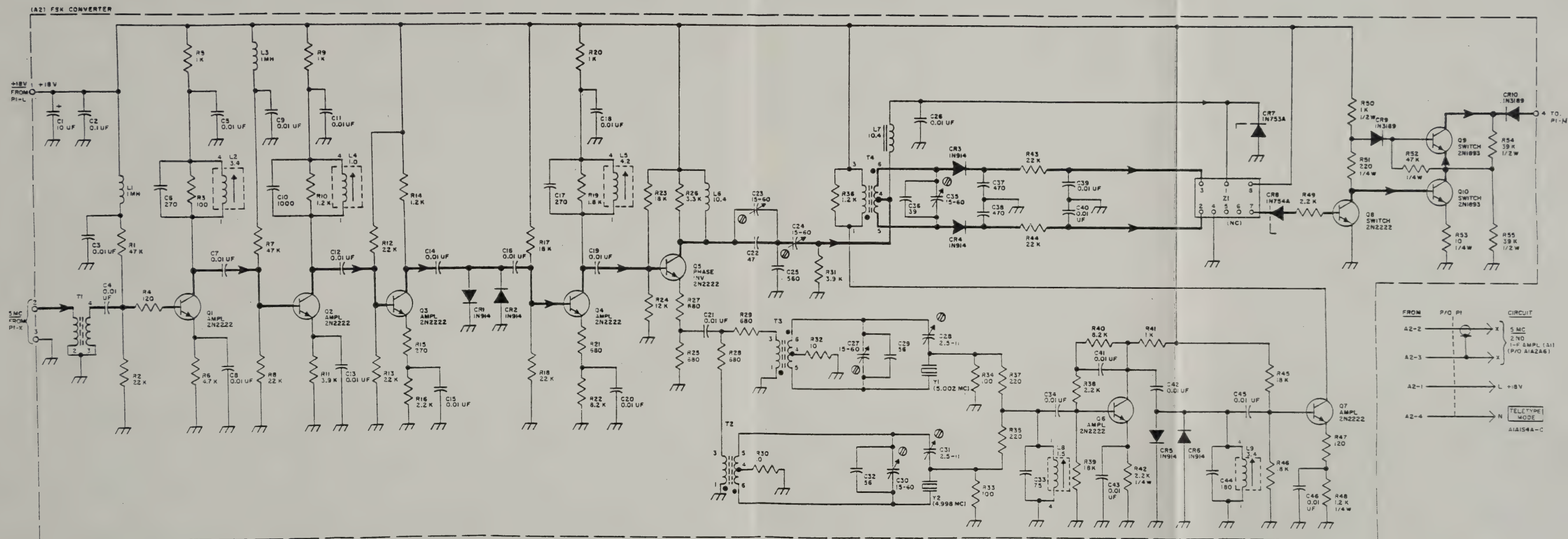
5-117 5-118

Figure 5-66. Detector/AF Amplifier A1A2A7,
Schematic Diagram (Sheet 1)

ORIGINAL

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Figure 5-67. Detector/AF Amplifier A1A2A7
Schematic Diagram (Sheet 2)

ORIGINAL

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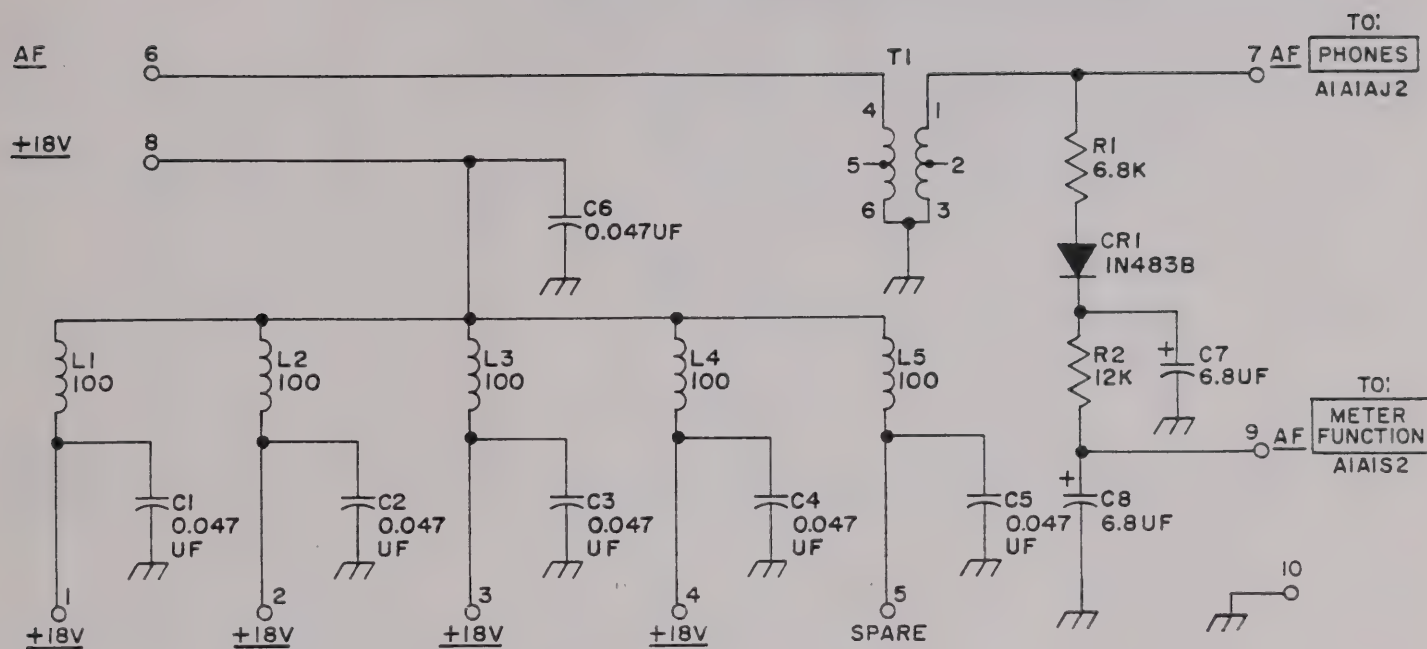


Figure 5-68. Front Deck Supply Decoupling
Board A1A2A8, Schematic Diagram

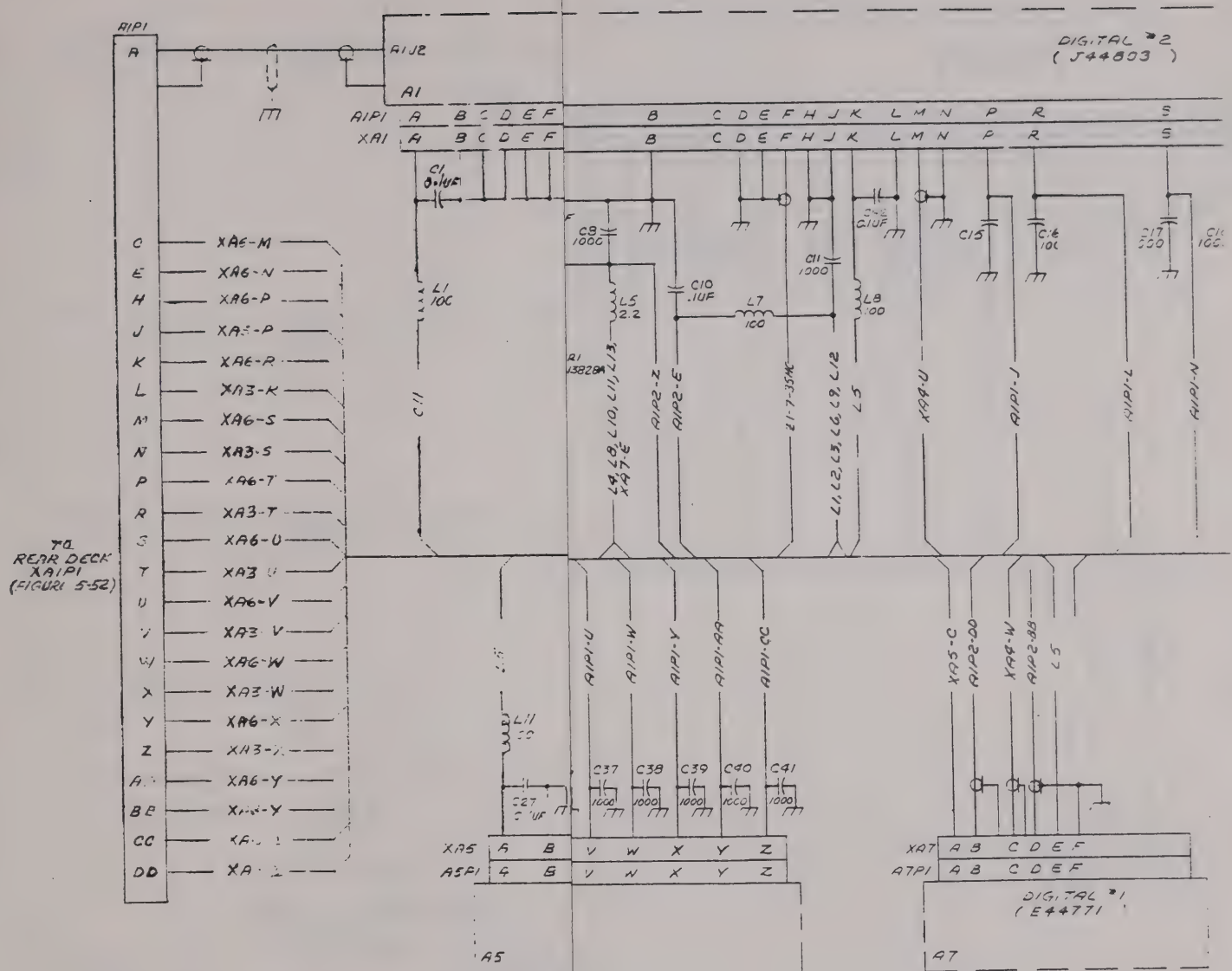


Figure 5-69. Synthesizer A1A3A1,
Interconnection Diagram

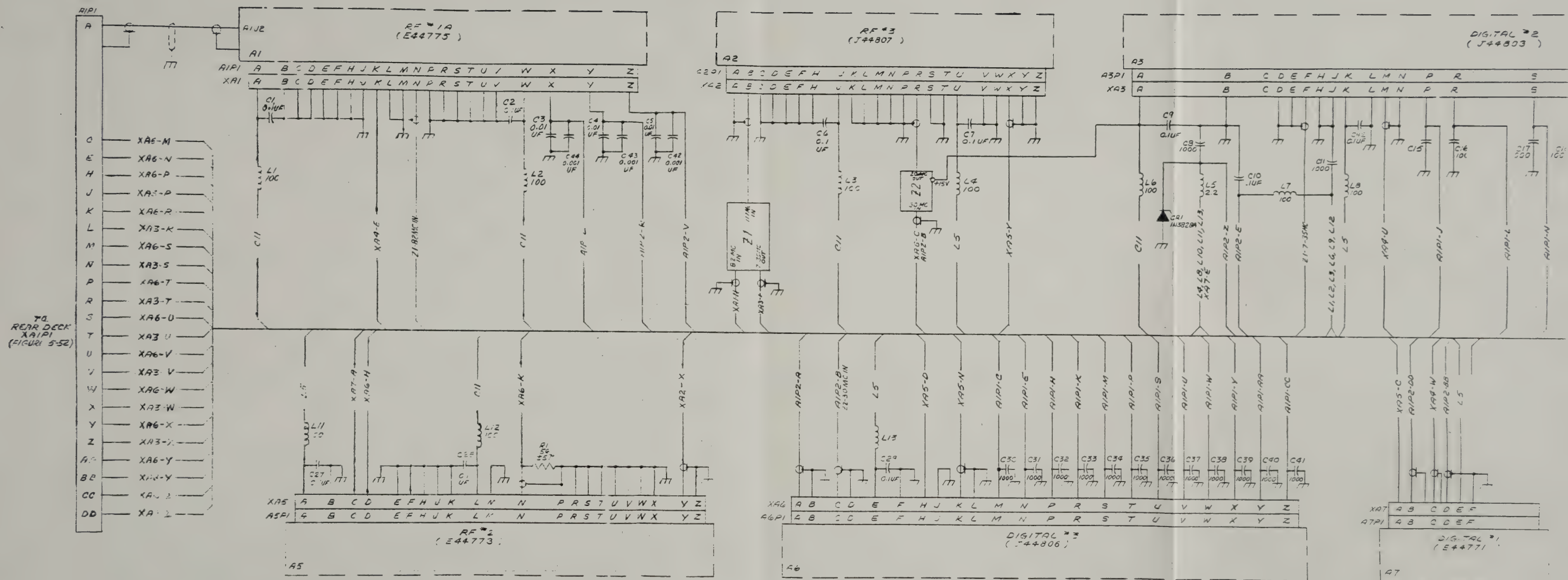


Figure 5-69. Synthesizer AlA3A1,
Interconnection Diagram

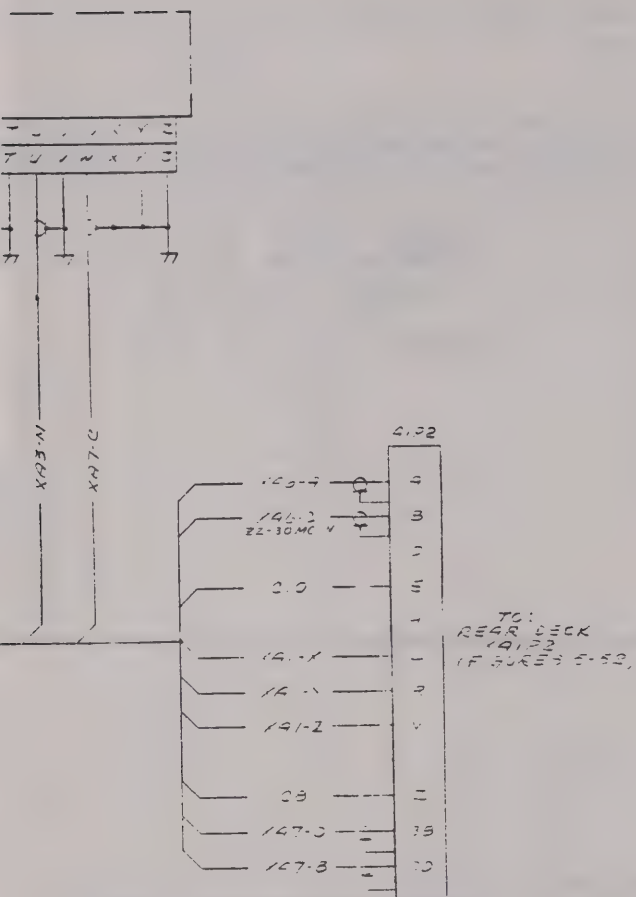


Figure 5-69. Synthesizer AlA3A1,
Interconnection Diagram

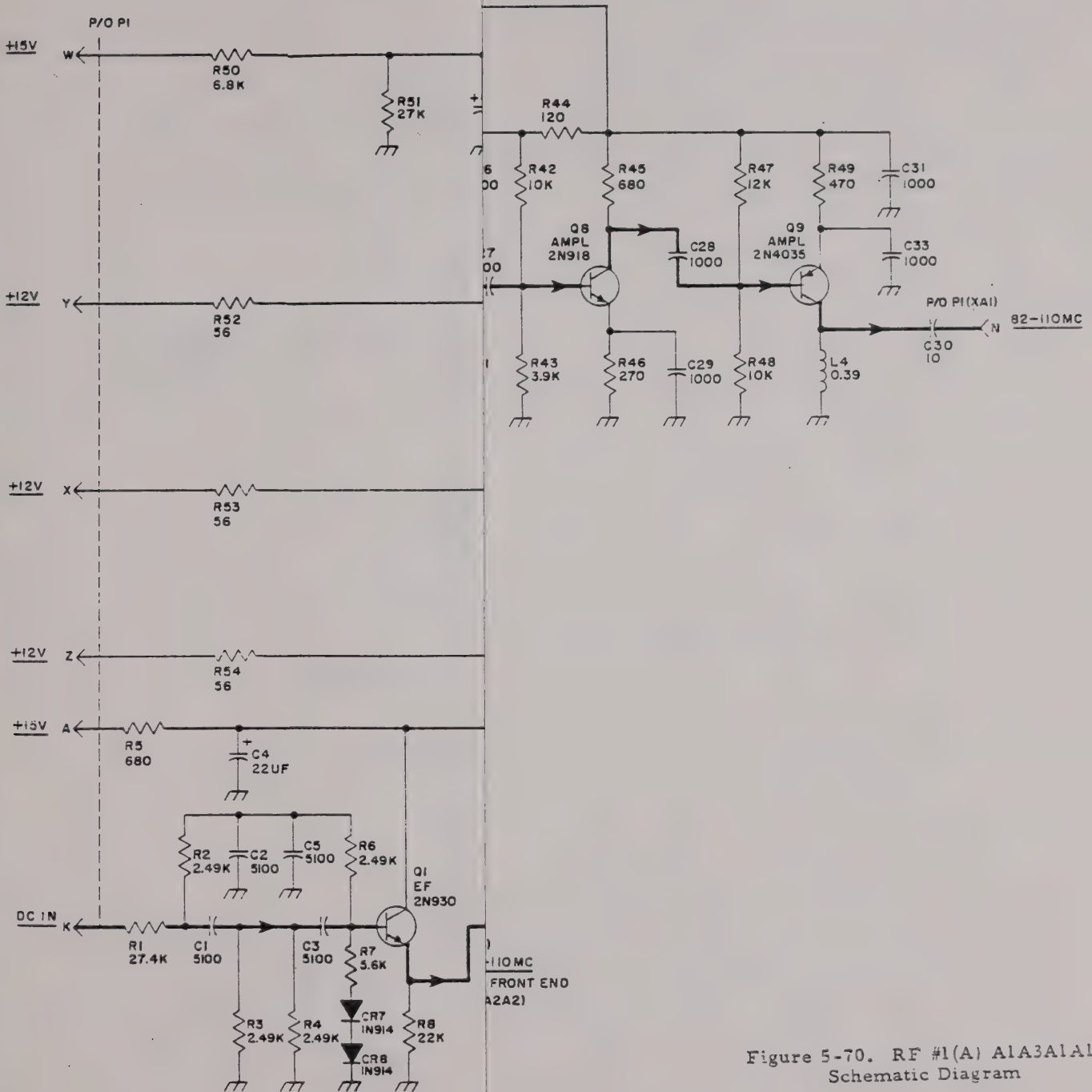


Figure 5-70. RF #1(A) A1A3A1A1,
Schematic Diagram

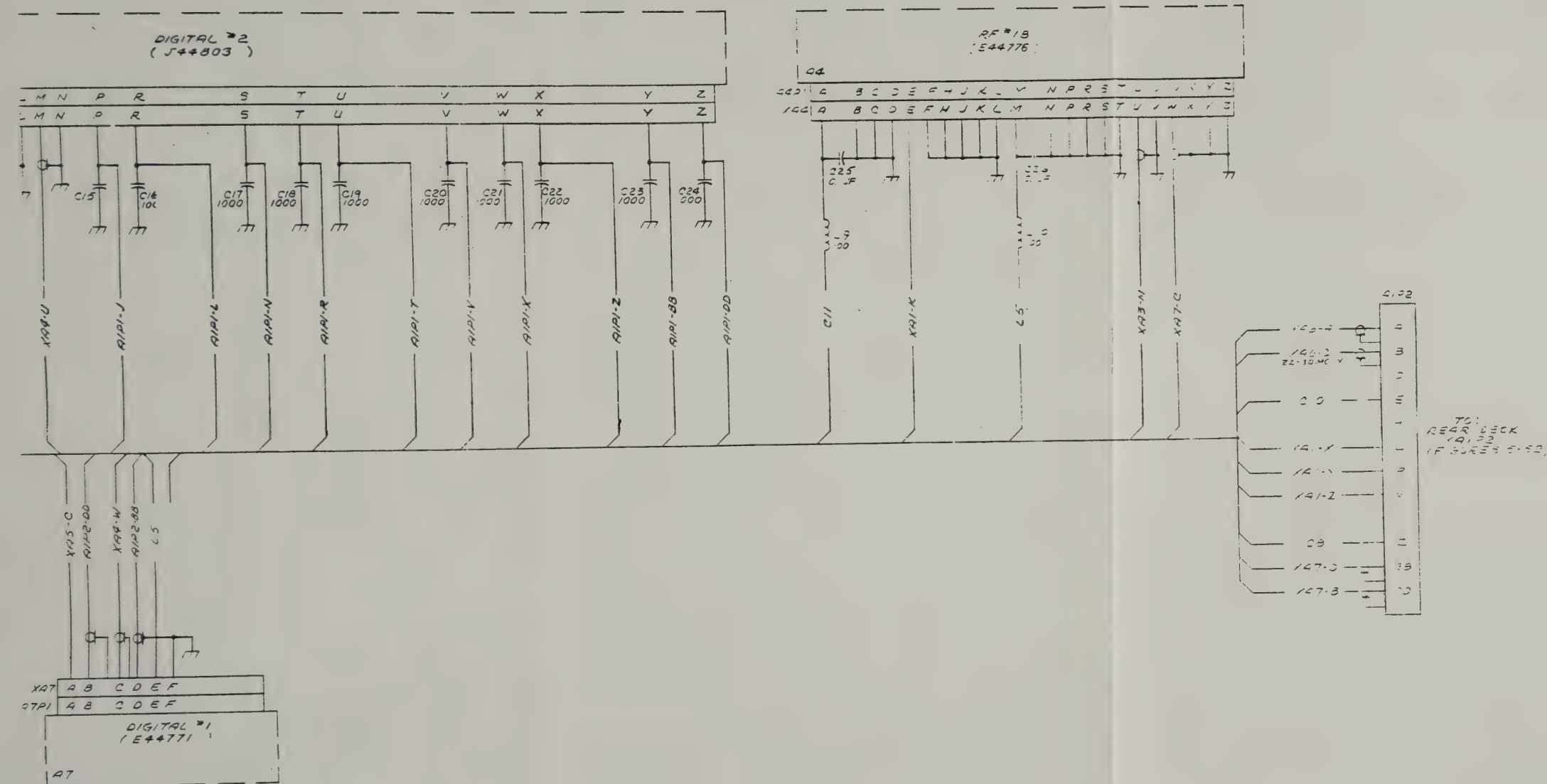
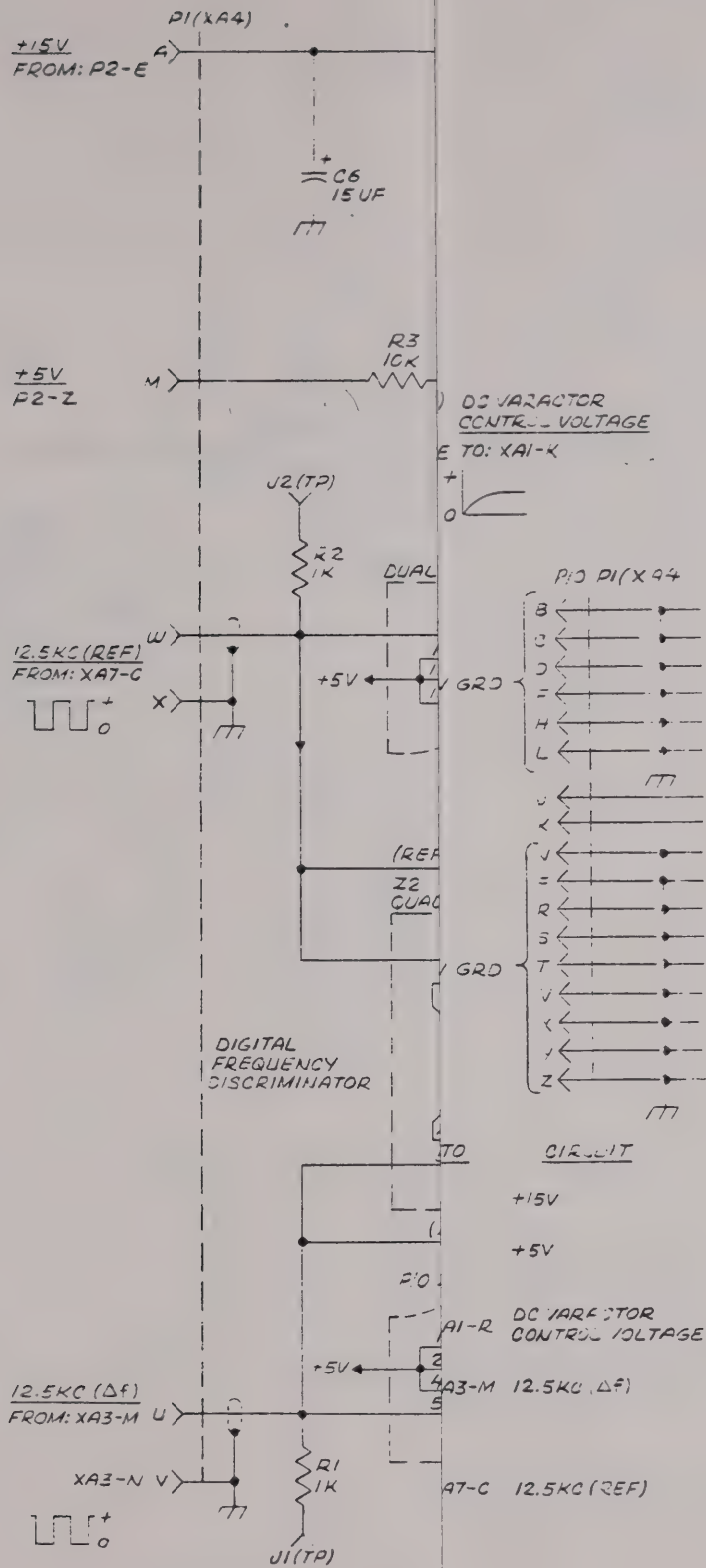


Figure 5-69. Synthesizer AlA3A1,
Interconnection Diagram



Figure 5-70. RF #1(A) AlA3AlAl,
Schematic Diagram

Figure
5-71



#1(B) A1A3A1A4,
Diagram

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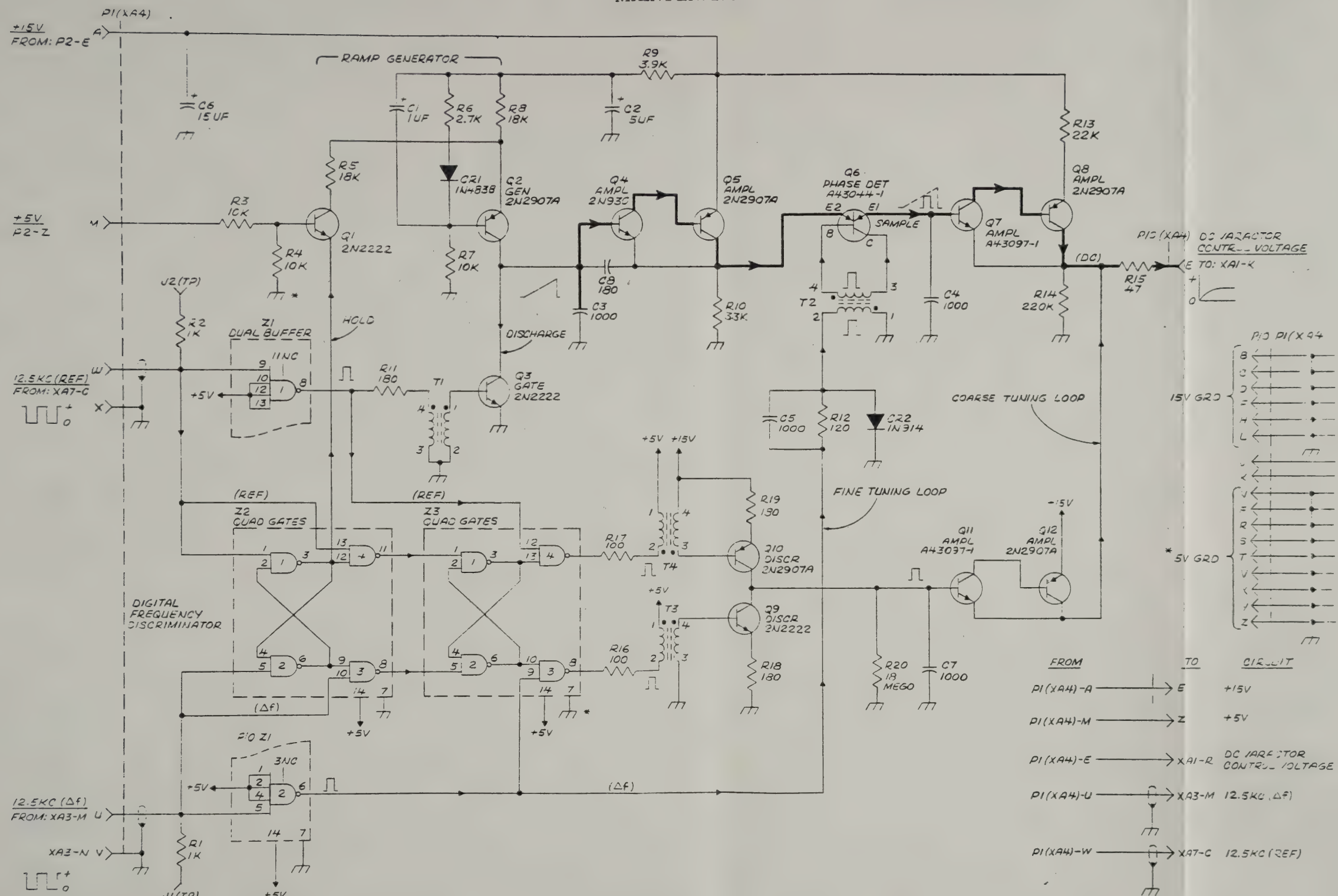


Figure 5-71. RF #1(B) A1A3A1A4,
Schematic Diagram

TM-05866A-15

Figure 5-72

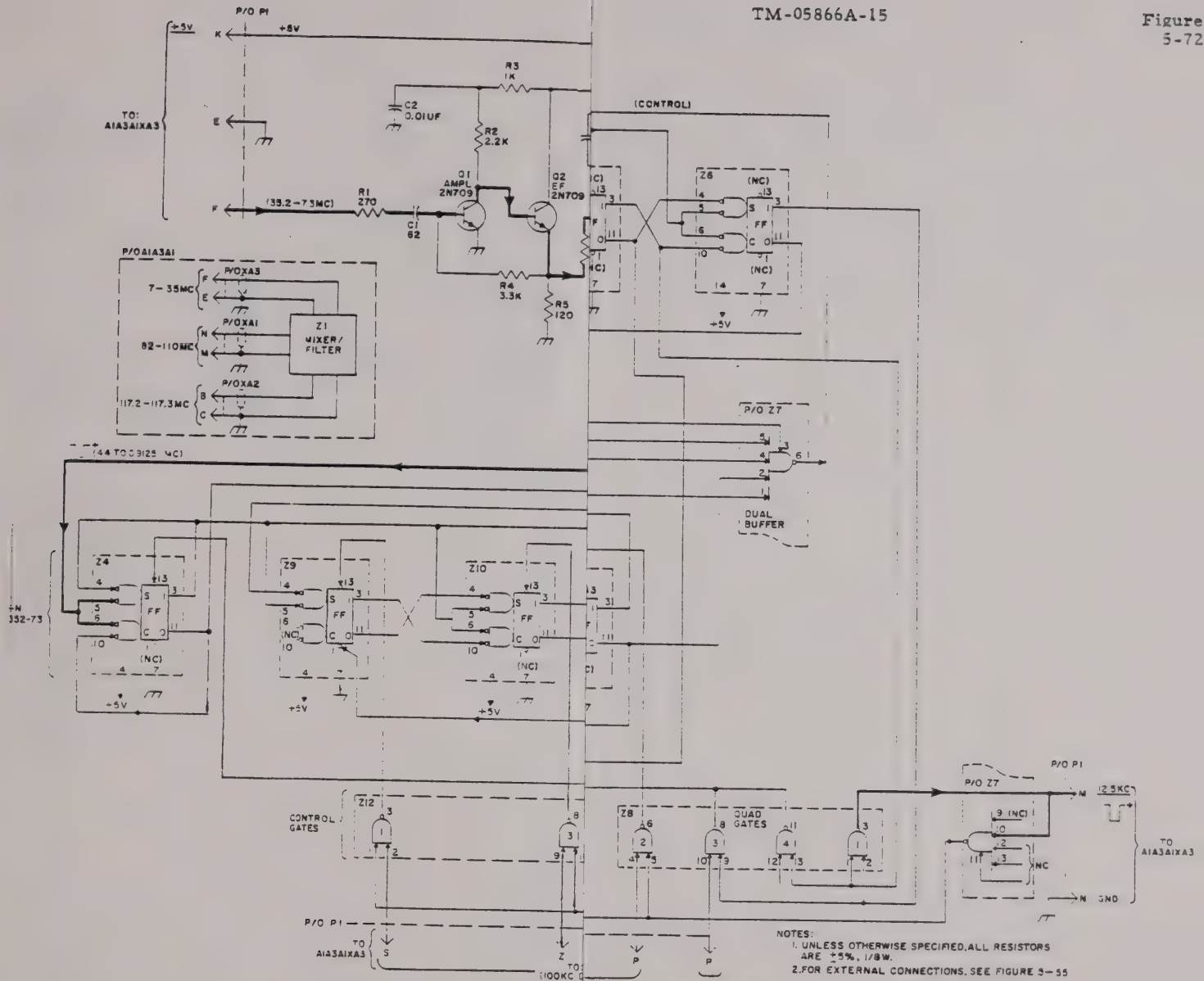
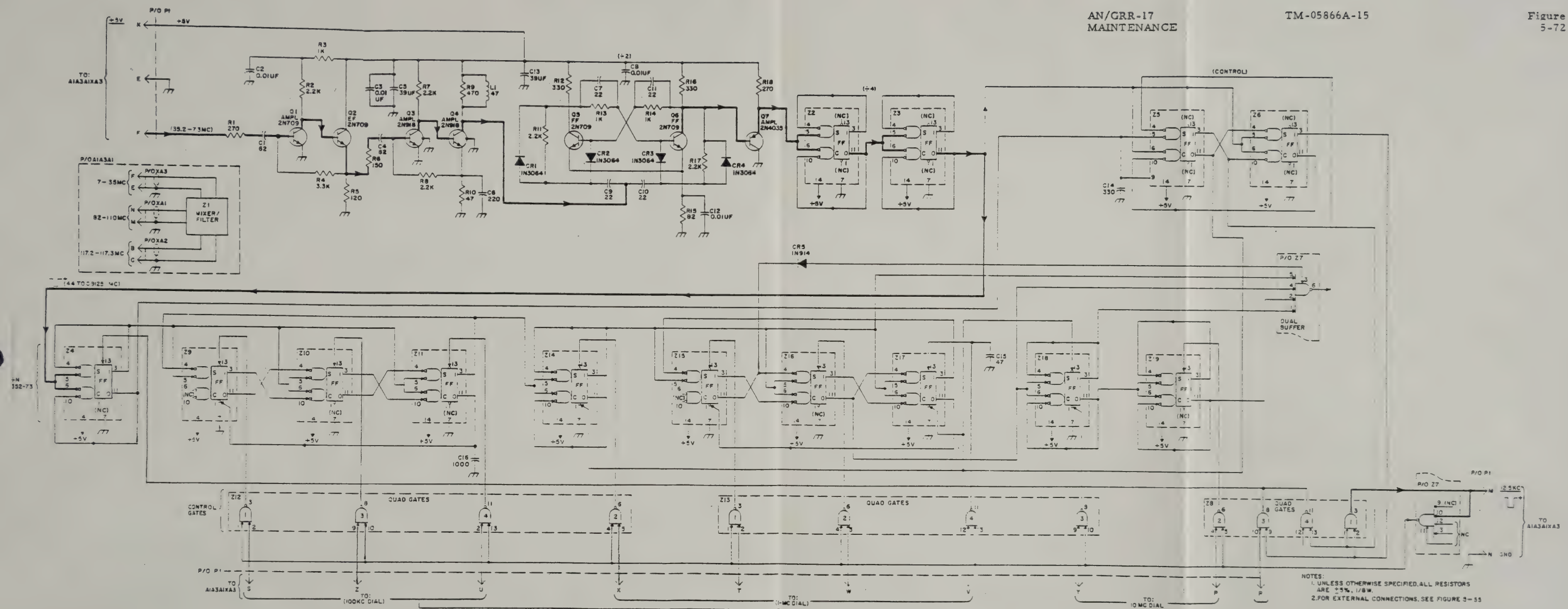


Figure 5-72. Digital #2 A1A3A1A3, Schematic Diagram

5-131/5-132



ORIGINAL

Figure 5-72. Digital #2 A1A3A1A3,
Schematic Diagram

TM-05866A-15

Figure 5-73

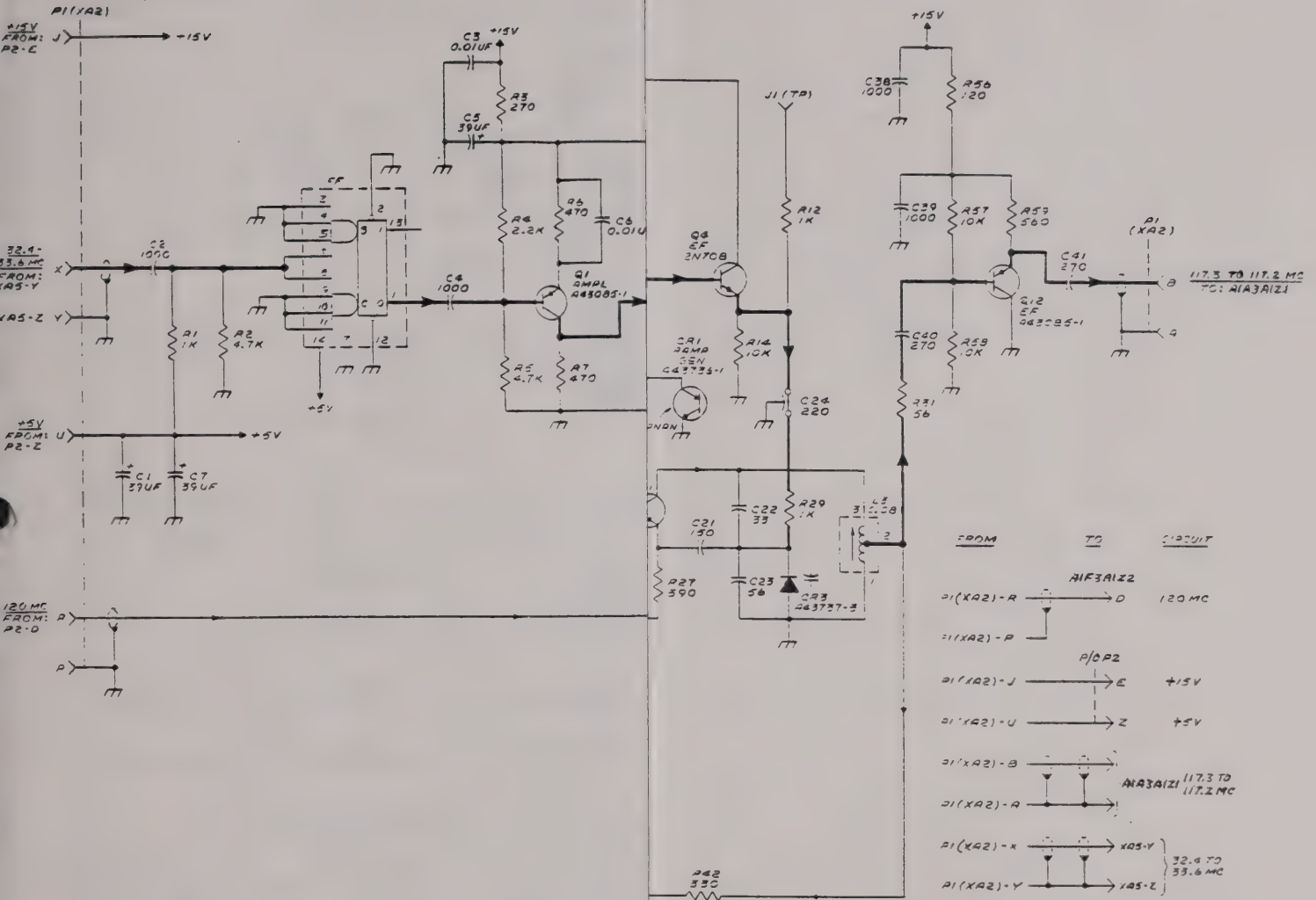


Figure 5-73. RF #3 A1A3A1A2, Schematic Diagram

5-133/5-134



5-133/5-134

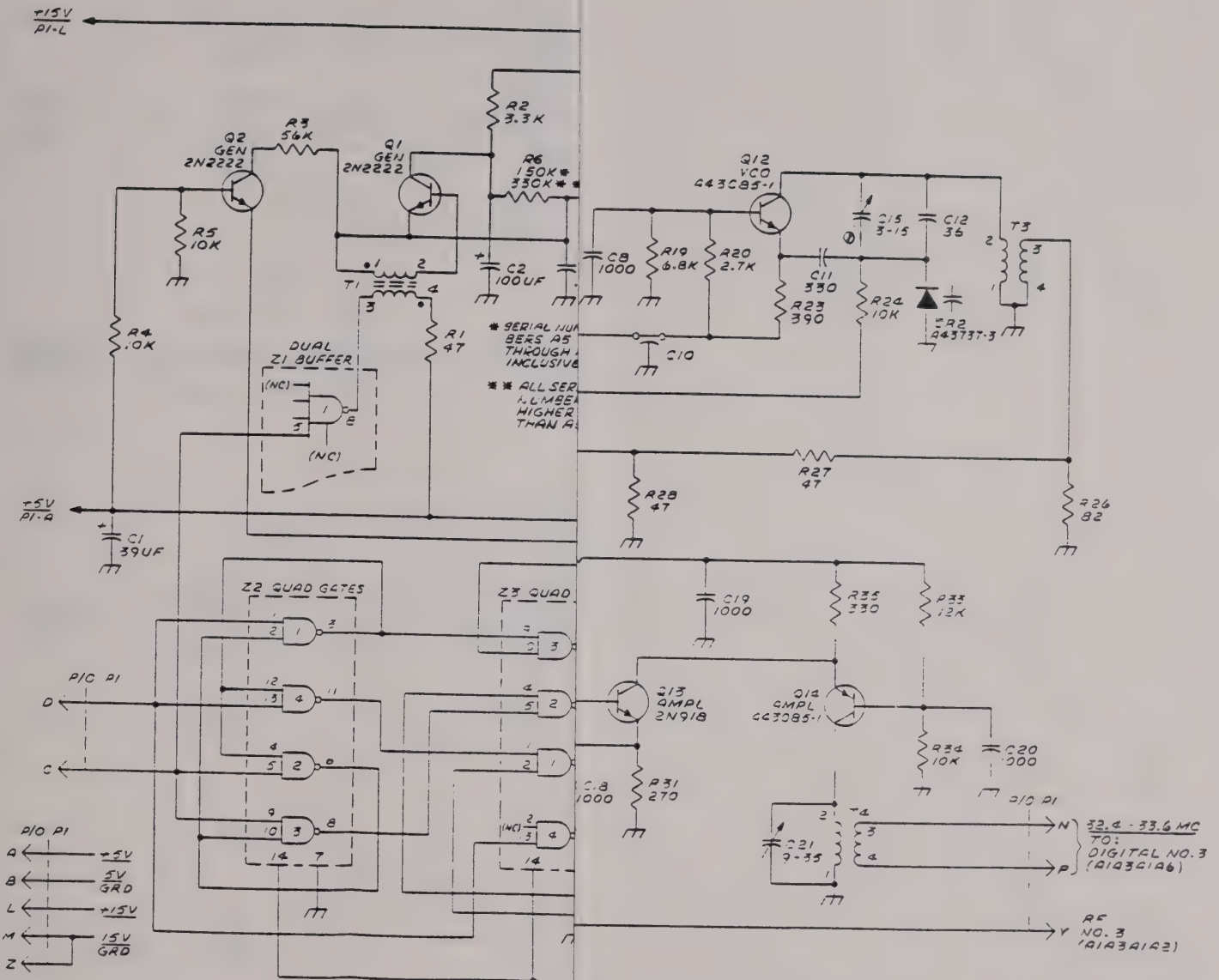
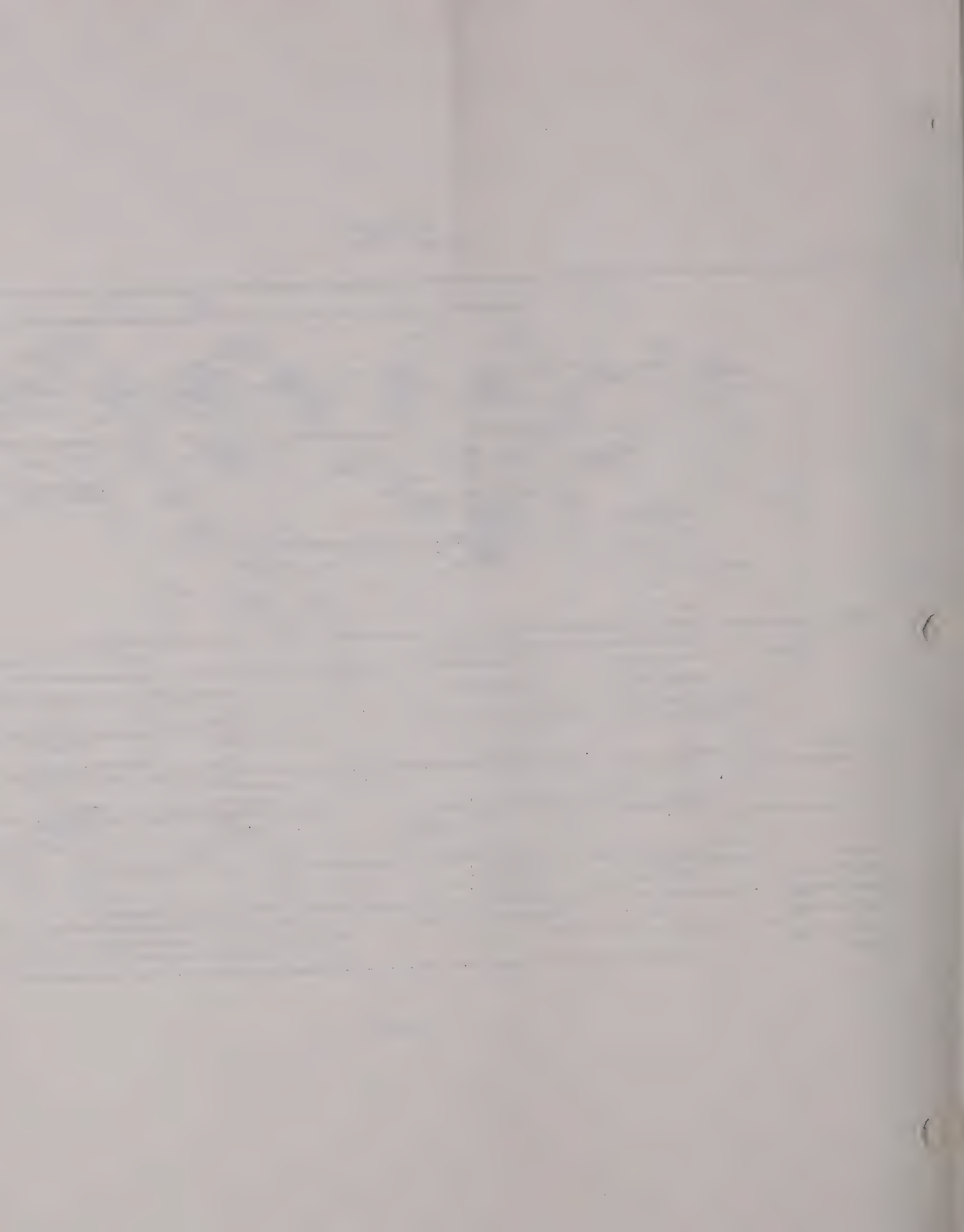


Figure 5-74. RF #2 A1A3A1A5,
Schematic Diagram



5-135/5-136



TM-05866A-15

Figure 5-75

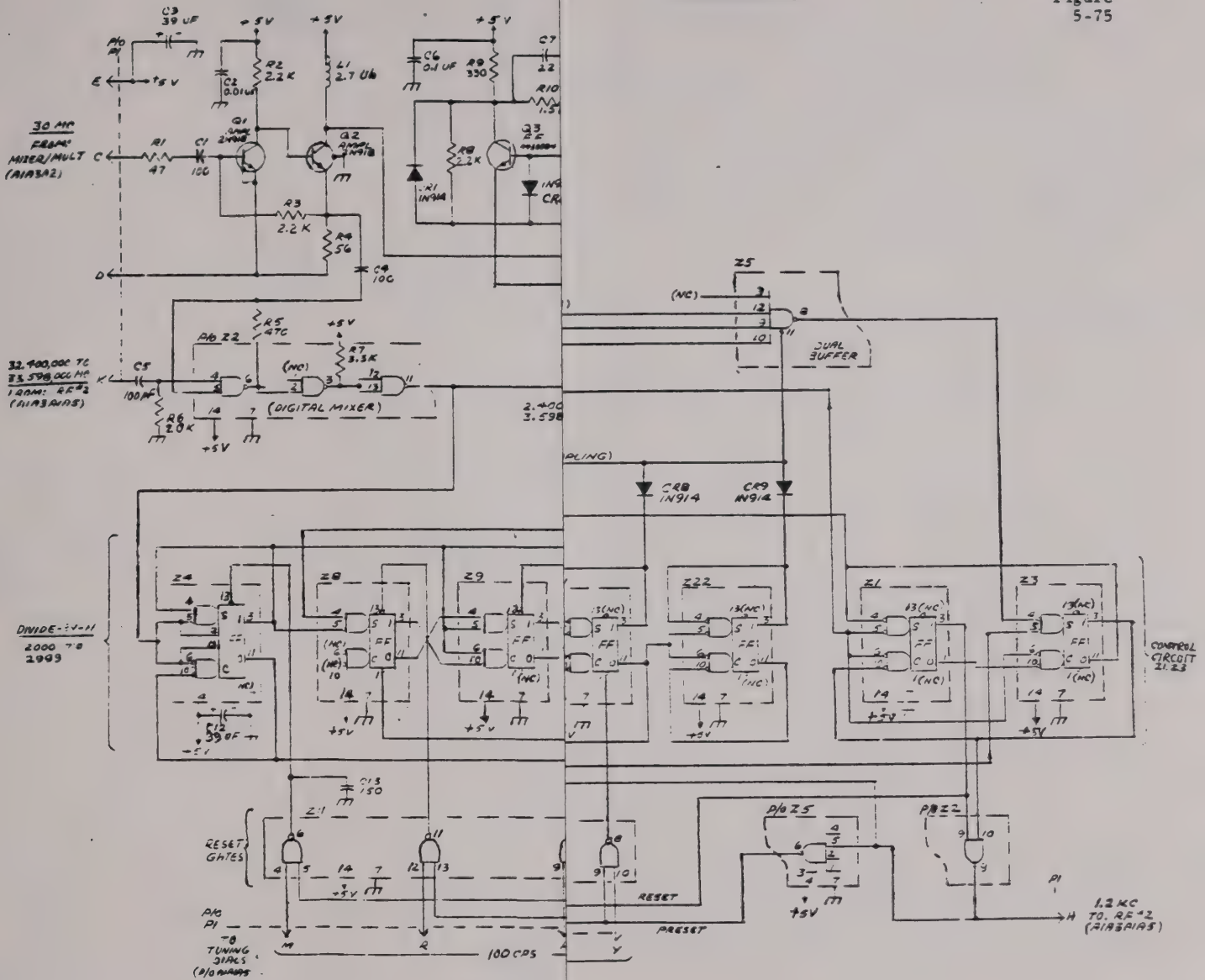


Figure 5-75. Digital #3 A1A3A1A6, Schematic Diagram

5-137/5-138

AN/GRR-17
MAINTENANCE

TM-05866A-15

Figure
5-75

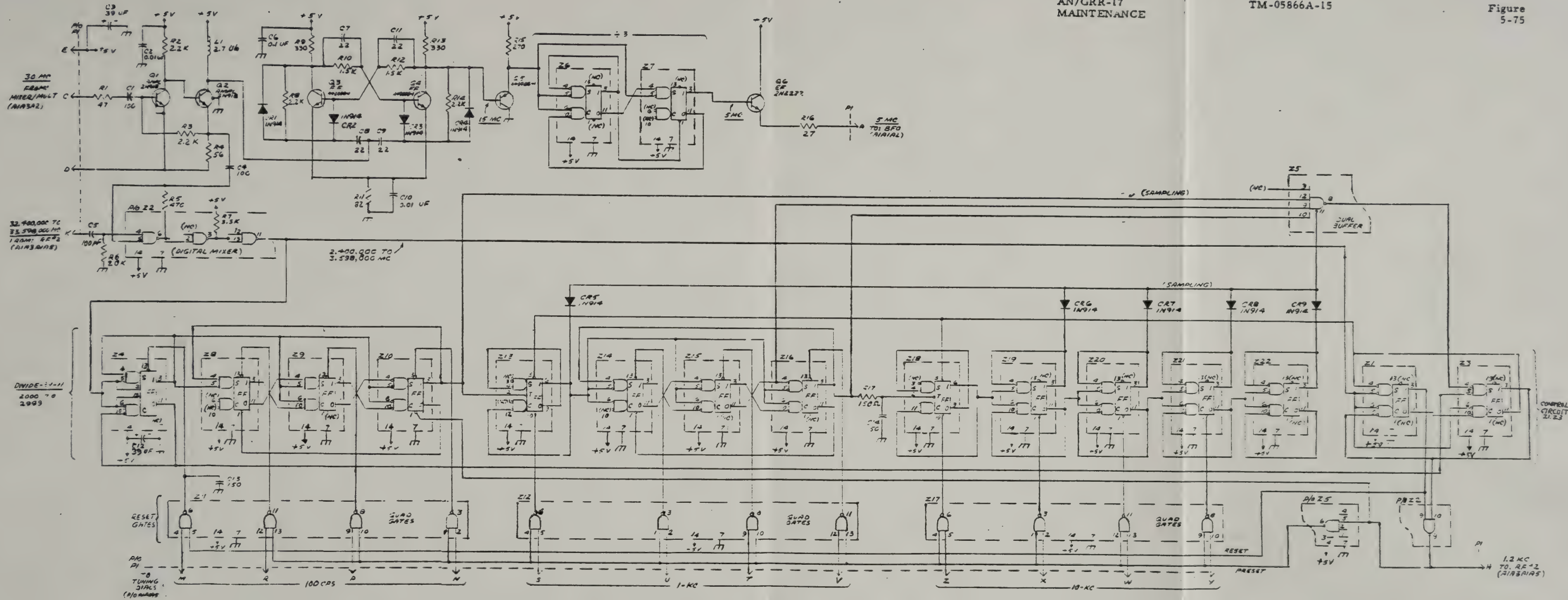


Figure 5-75. Digital #3 A1A3A1A6,
Schematic Diagram

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5-137/5-138



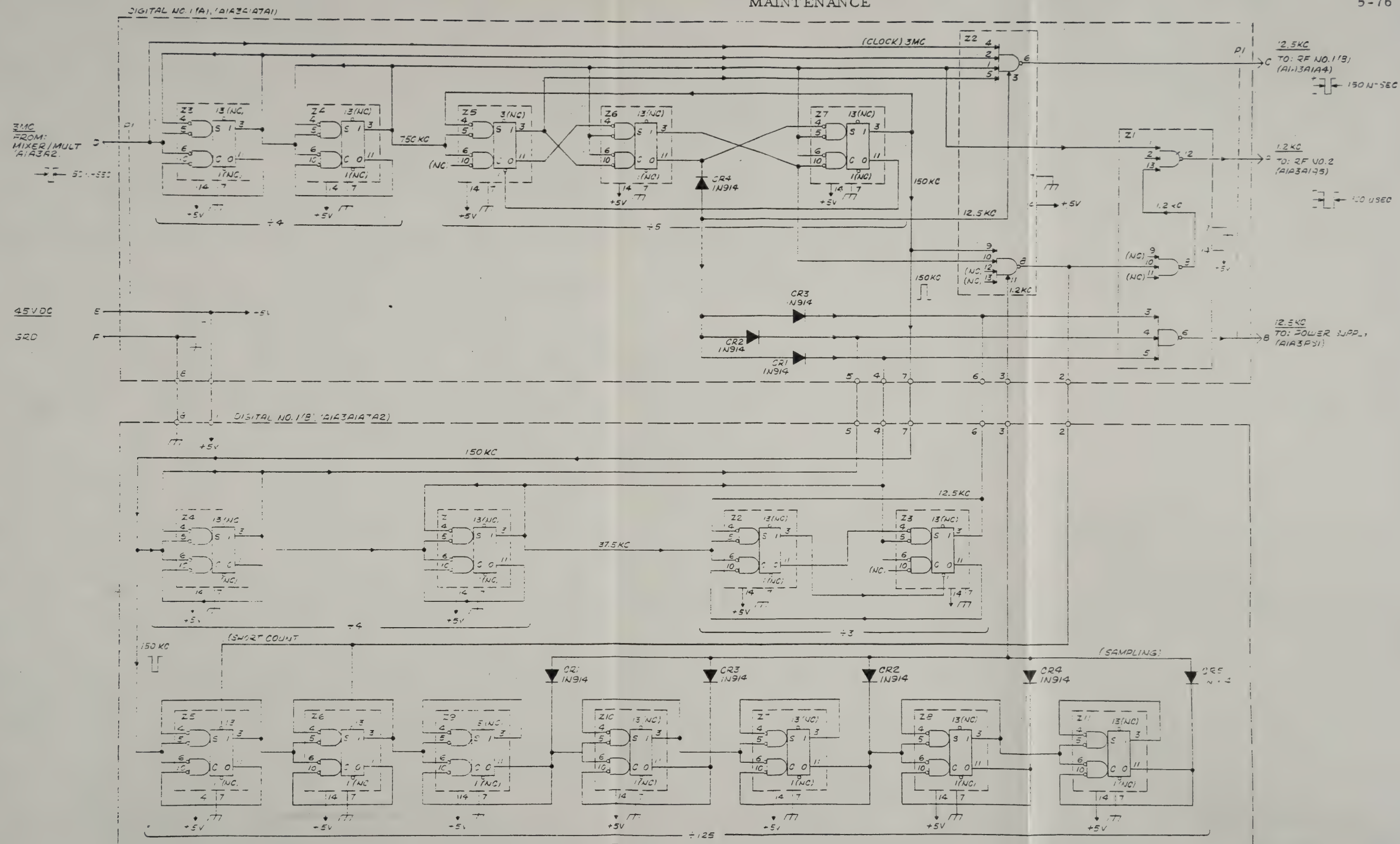
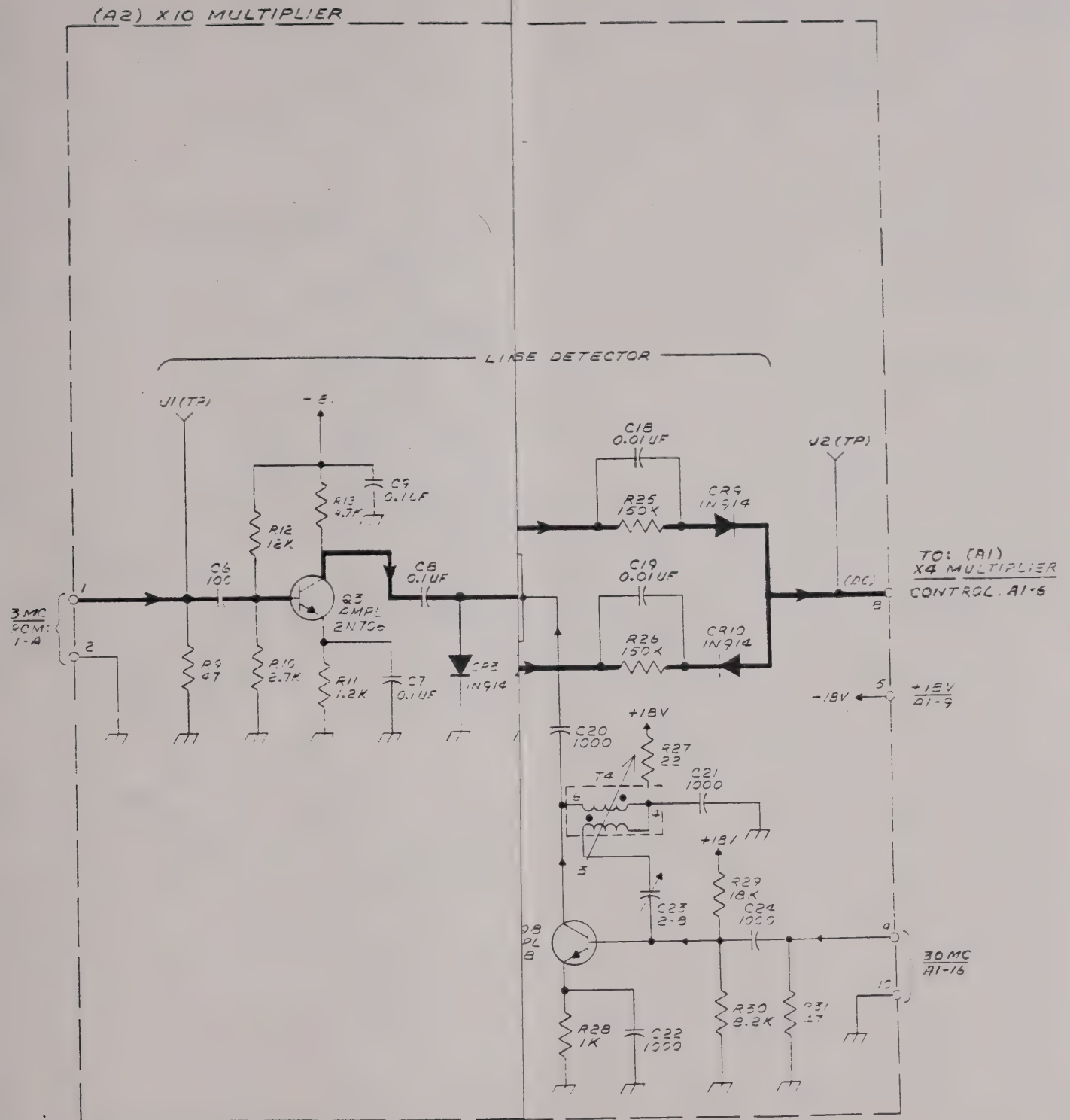
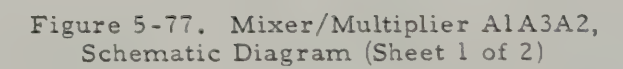


Figure 5-76. Digital #1 A1A3A1A7,
Schematic Diagram





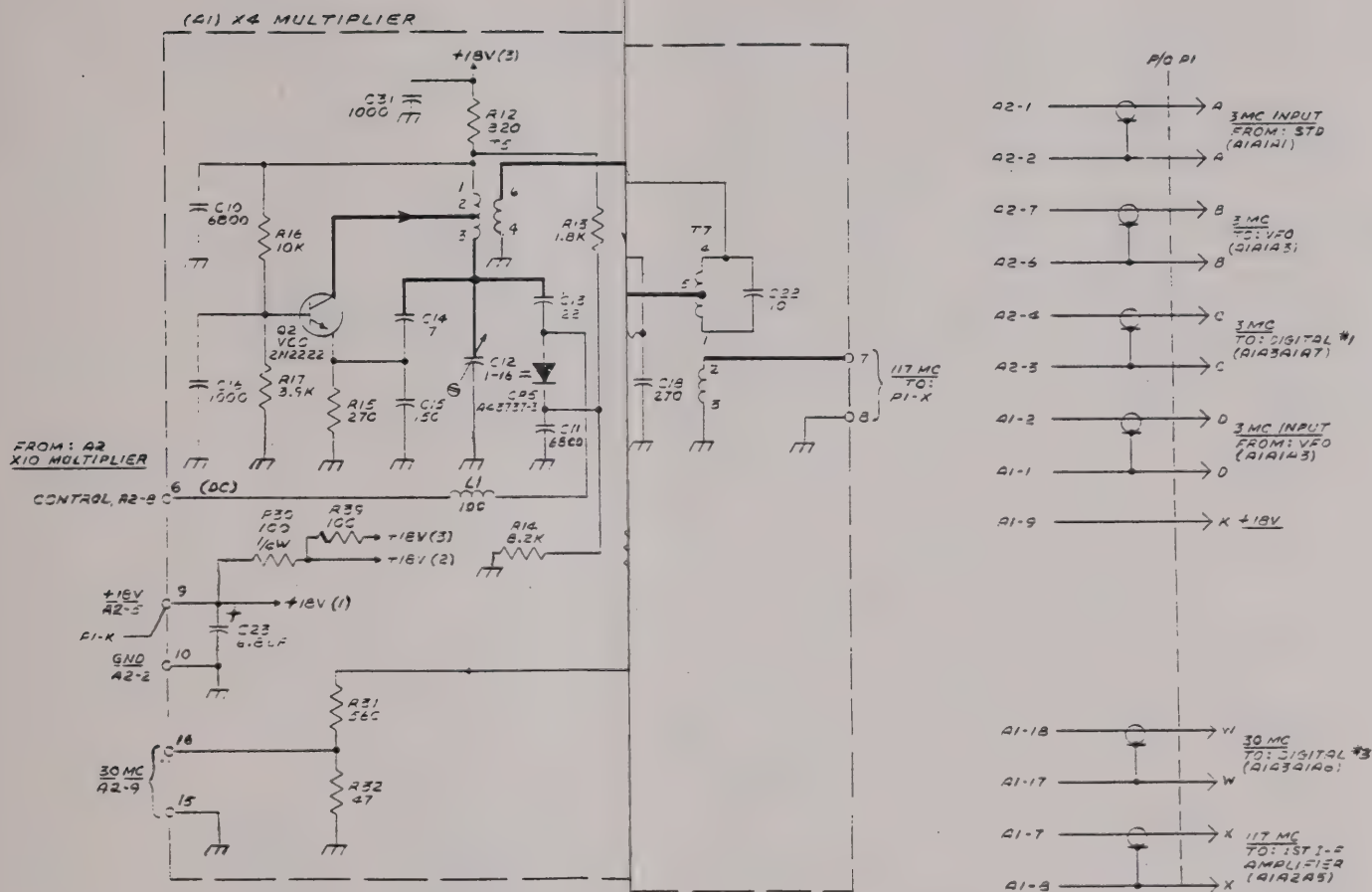


Figure 5-77. Mixer/Multiplier A1A3A2,
Schematic Diagram (Sheet 2 of 2)

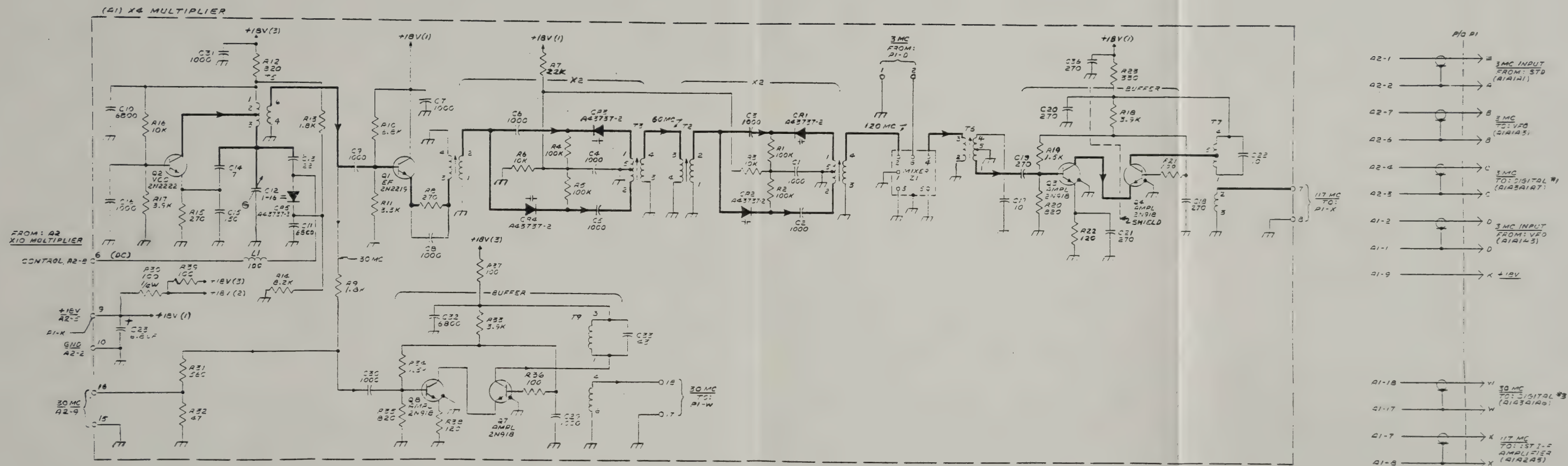


Figure 5-77. Mixer/Multiplier A1A3A2,
Schematic Diagram (Sheet 2 of 2)

ORIGINAL

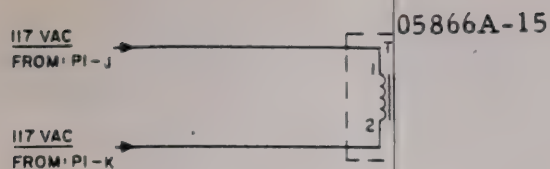


Figure
5-78

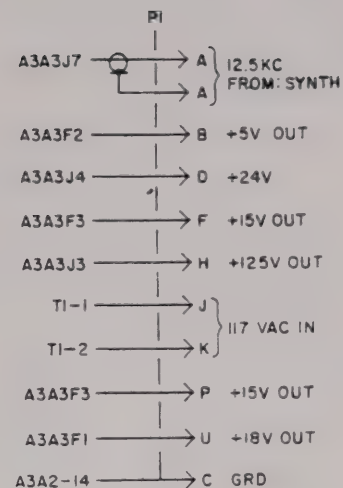
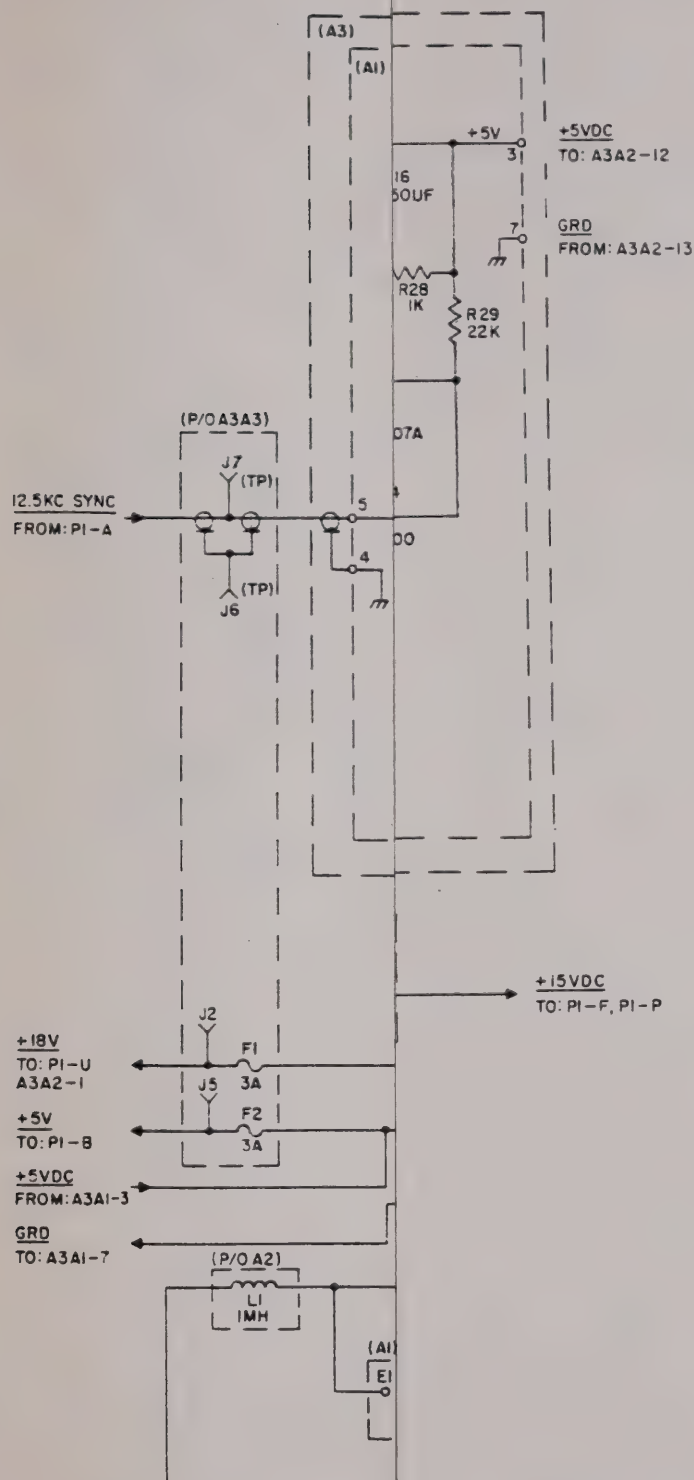
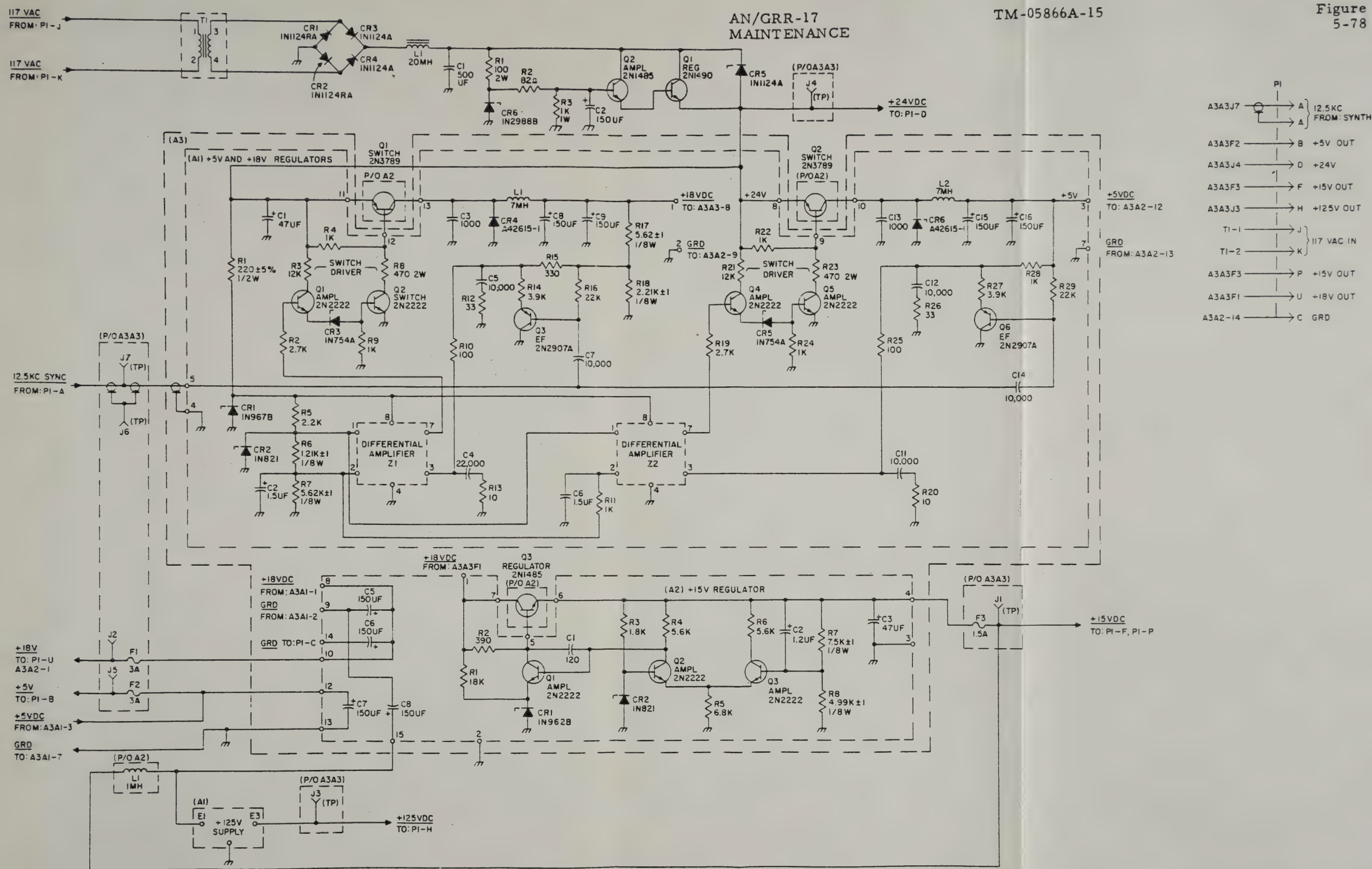
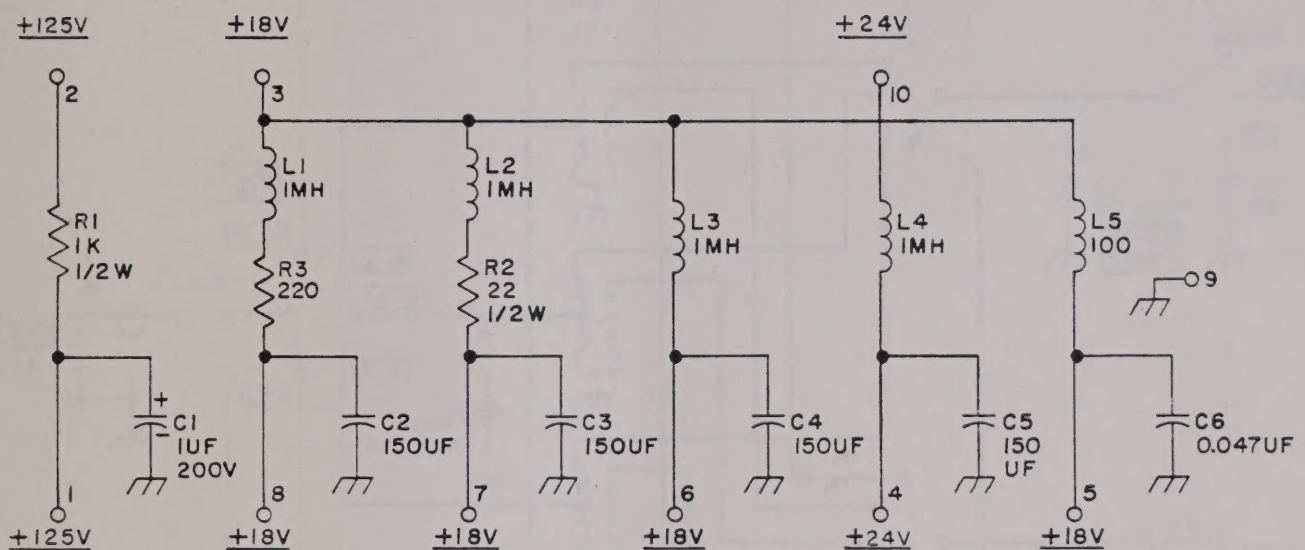


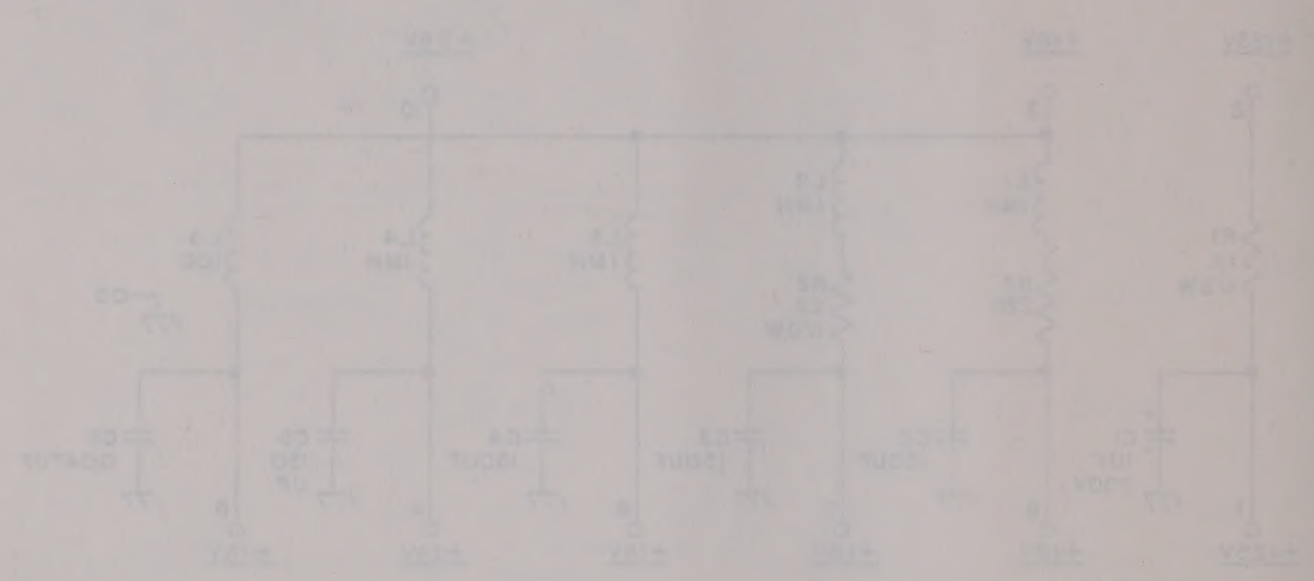
Figure 5-78. Power Supply A1A3PS1,
Schematic Diagram

Figure 5-78. Power Supply A1A3PS1,
Schematic Diagram



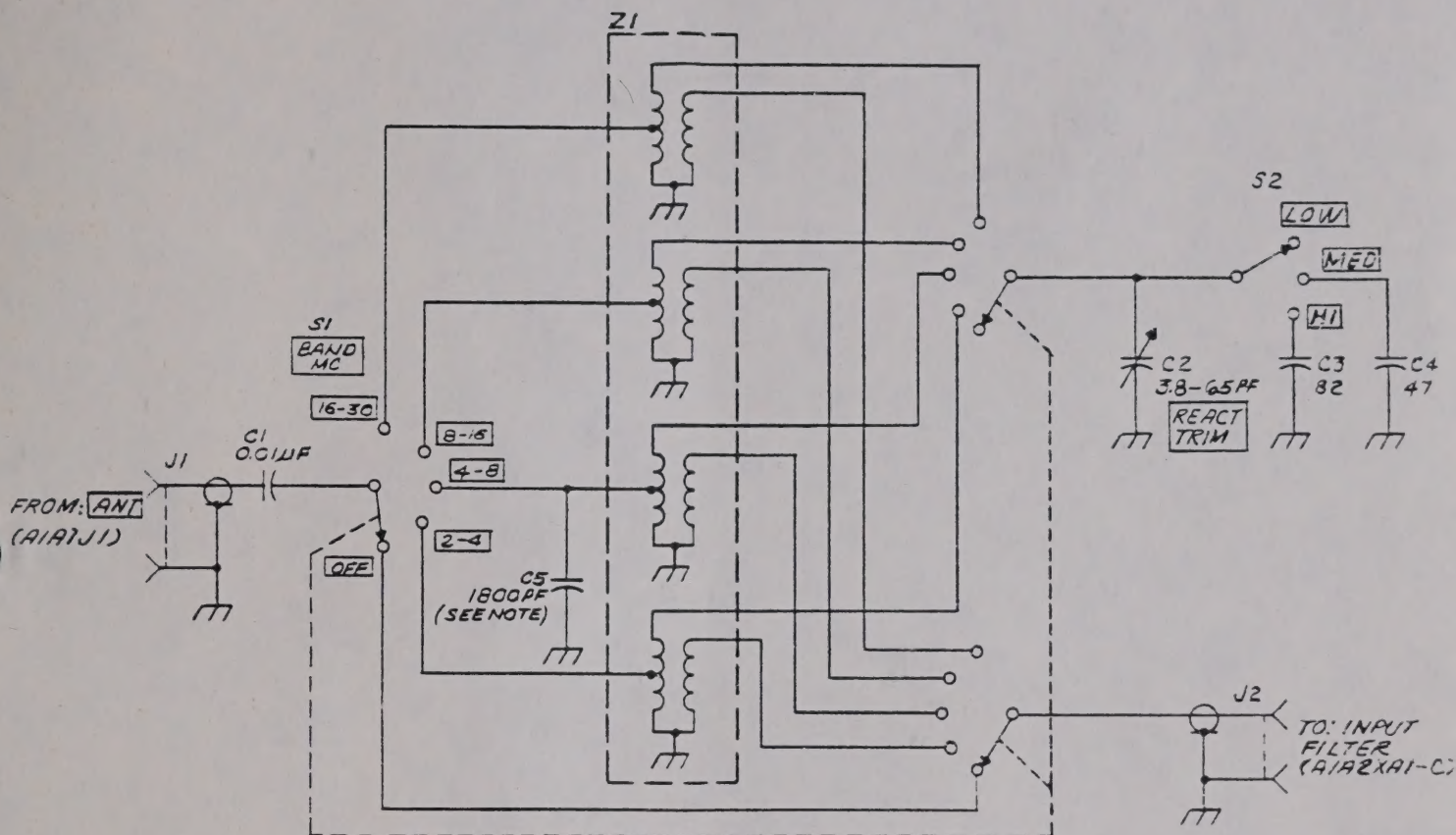
NOTES: 1. FOR EXTERNAL CONNECTIONS
SEE FIGURE 5-55

Figure 5-79. Rear Deck Supply Decoupling
Board AlA3A3, Schematic Diagram



NOTE: FOR EXTERNAL CONNECTIONS
SEE FIGURE 2-11

Figure 2-10. Power Supply Diagram
Board A1A1, Subsystem Diagram



NOTE:

CAPACITOR C5 IS USED ONLY ON SERIAL NOS. A5 THROUGH A29; THIS CAPACITOR IS NOT USED ON SERIAL NO. A30 OR ON SERIAL NOS. HIGHER THAN NO. A30.

Figure 5-80. Antenna Trimming Circuit A1A1A6, Schematic Diagram

